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VOLUME 3 DIAGRAMS

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The diagrams in this manual are printed only on odd-numbered pages. With two exceptions, the reverse sides of the diagrams are blank.

PREFACE

This manual contains information to assist trained Engineering Services personnel during maintenance of the CDC® CYBERPLUS Parallel Processor, with or without the direct memory access unit (DMAU). A supplement to this manual is planned that will document the DMAU and floating point unit (FPU) options.

OVERVIEW

This manual first provides an overview of the CYBERPLUS Parallel Processor and of the base processor in high-level block diagram form (level 1 diagrams). Block diagram overviews (level 2 diagrams) with descriptive text and the corresponding detailed logic diagrams (level 4 diagrams) are then provided for each of the functional units of the base processor and the DMAU.

RELATED PUBLICATIONS

Following is a list of other manuals applicable to the maintenance of the CYBERPLUS Parallel Processor:

Manual Title	Publication Number
CYBERPLUS Parallel Processor, Hardware Maintenance Manual, Volume 1, Installation and Checkout	60461740
CYBERPLUS Parallel Processor, Hardware Maintenance Manual, Volume 2, Maintenance and Parts Data	60461850
CYBERPLUS Parallel Processor, Hardware Maintenance Manual, Volume 4, Troubleshooting	60462390
CYBERPLUS Parallel Processor System, Hardware Reference Manual	77960981

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I. OVERVIEW

1. CYBERPLUS PARALLEL PROCESSOR SYSTEM

SYSTEM FUNCTION

The CYBERPLUS Parallel Processor is capable of processing scientific and business applications at a very high computational rate. The system can be tailored to the performance requirements of the application by utilizing the ring architecture of the system to provide parallel computational routes for portions of the processing.

GENERAL DESCRIPTION

The CYBERPLUS Parallel Processor consists of the 16-bit base processor, the CYBER channel ring port (CRP), the high performance memory (HPM), and the two optional features, floating point unit (FPU) and the direct memory access unit (DMAU). A block diagram of the CYBERPLUS system is shown in figure I-1-1.

The CYBER channel ring port connects the system ring to the host computer, allowing communication between the host computer and one or more (up to 16) base processors.

The base processor is made up of a crossbar switch and 15 functional units. Three of the functional units allow the base processor to communicate on two of the four communication rings and to the external memory. Ring port 0 connects the base processor to the system ring; ring port 1 connects the base processor to the application ring, and the external memory unit connects the base processor to the high performance memory.

The floating point unit, which is optional, provides CYBERPLUS with the capability to perform floating point arithmetic. The floating point unit can add, subtract, compare, multiply, divide, and calculate square roots using floating point formatted numbers.

The DMAU, which is also optional, consists of the system ring interface (SRI), the memory ring interface (MRI), the processor memory interface (PMI), and the central memory interface (CMI), and provides the common link between three of the four communication rings. The DMAU is connected to the system ring via the SRI; to the memory ring via the MRI; and to the central memory ring via the PMI. The central memory interface provides the link between the central memory ring and memory of the host computer.

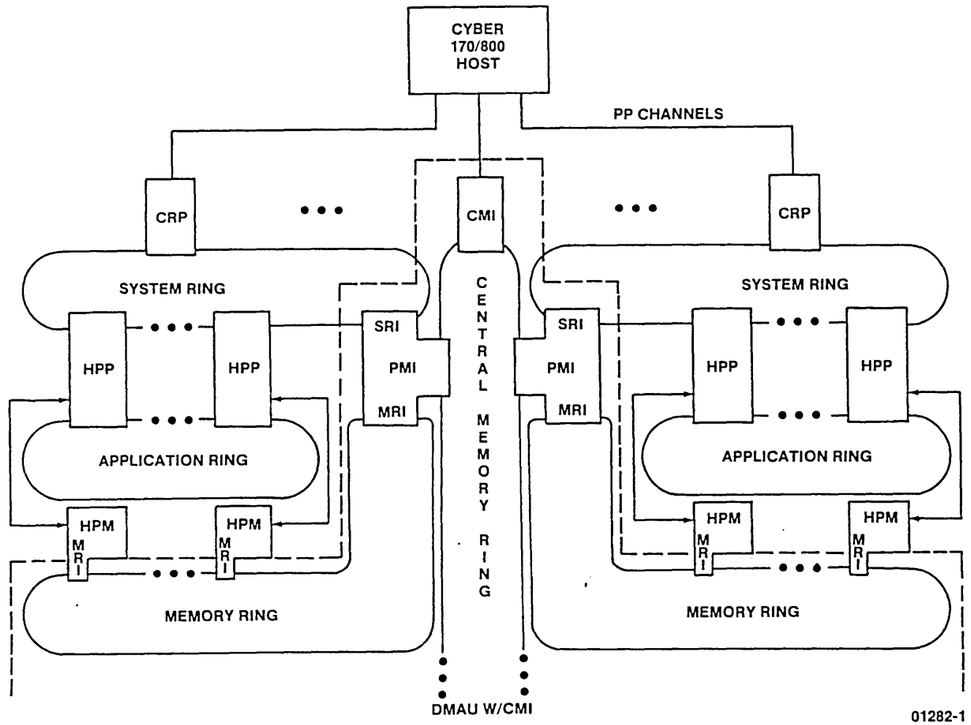


Figure I-1-1. CYBERPLUS Parallel Processor

HØST CENTRAL MEMØRY

CENTRAL MEMØRY RING

PRØCESSØR MEMØRY INTERFACE PMI 2.0

3

CENTRAL MEMØRY INTERFACE CMI 2.0

4

CENTRAL MEMØRY RING

MEMØRY RING

MEMØRY RING INTERFACE MRI 2.0

SYSTEM RING INTERFACE SRI 2.0

2

SYSTEM RING

BANK 0 | BANK 1 | BANK 2 | BANK 3 | BANK 4 | BANK 5 | BANK 6 | BANK 7

HIGH PERFØRMANCE MEMØRY HPM 2.0

MULTIPLE MEMØRY INTERFACE MMI 2.0

MEMØRY RING INTERFACE MRI 2.0

MEMØRY RING 5

APPLICATIØN RING

RING PØRT 0 RPU 4.0

CRØSS BAR

CØNTRØL CØN 2.0

EXTERNAL MEMØRY ACCESS 0 XMA 2.0

EXTERNAL MEMØRY ACCESS 1 XMA 2.0

DATA MEMØRY 0 DMU 2.0

DATA MEMØRY 1 DMU 2.0

DATA MEMØRY 2 DMU 2.0

DATA MEMØRY 3 DMU 2.0

MULTIPLIER MUL 2.0

ADDER 0 ADD 2.0

ADDER 1 ADD 2.0

DATA FILES F G FGU 2.0

SHIFT/ BØØLEAN 0 SBU 2.0

SHIFT/ BØØLEAN 1 SBU 2.1

RING PØRT 1 RPU 2.1

APPLICATIØN RING

SYSTEM RING

CYBER CHANNEL RING PØRT CRP 2.0

1

HØST CYBER DEDICATED PP CHANNEL

FLØATING PØINT CØNTRØL UNIT FPC 2.0

FLØATING PØINT CRØSS BAR FPC 2.0

MULTIPLY FPM 2.0

DIVIDE SQUARE RØØT FPD 2.0

ADD FPA 2.0

FILE FPC 2.0

NØTES:

1. ØNE CRP CAN HANDLE A MAXIMUM ØF 16 BASE PRØCESSØRS.
2. ØNLY ØNE SRI PER SYSTEM RING.
3. ØNLY ØNE PMI PER SRI. ØNLY FØUR PMI'S PER CENTRAL MEMØRY RING.
4. ØNE CMI CAN HANDLE A MAXIMUM ØF FØUR PMI'S.
5. THE MEMØRY RING CAN HAVE A MAXIMUM ØF 16 MRI'S.

CONTROL DATA CORPORATION

DEVELØPMENT DIVISIØN

LEVEL 1 DIAGRAM
CYBERPLUS SUBSYSTEM.
(INCLUDING ØPTIØNS)

CODE IDENT | DWG NO | REV
60461830 | A

SHEET CYP 1.1 | SIZE I-1-3

2. KEY-TO-SYMBOLS DIAGRAM

SYMBOL DESCRIPTIONS

The symbols used in the diagrams within this manual are shown in figure I-2-2 along with an explanation of their uses and meanings. The number of unfamiliar symbols on the diagrams has been kept to a minimum. However, some symbols have been adapted to the hardware design details of the CYBERPLUS and therefore have taken on some additional or special meanings not previously employed in other systems. Time should be spent getting familiar with these differences.

CABINET CONFIGURATION

The CYBERPLUS Parallel Processor is housed in a cabinet consisting of a two column unit and a single column unit. The two column unit is always on the left as one faces the logic panels. It houses the base processor, the high performance memories (HPMs), the CYBER channel ring port (CRP), and the optional direct memory access unit (DMAU). The single column unit houses the optional floating point unit (FPU). The CYBERPLUS cabinet configuration portion of the Key-to-Symbols diagram (figure I-2-1) shows the location of the functional unit logic panels within the CYBERPLUS cabinet.

Figure I-2-1 below shows the top view of a typical "plus" cabinet arrangement for four CYBERPLUS Parallel Processors. The arrows point to the logic-panel side of the four processors.

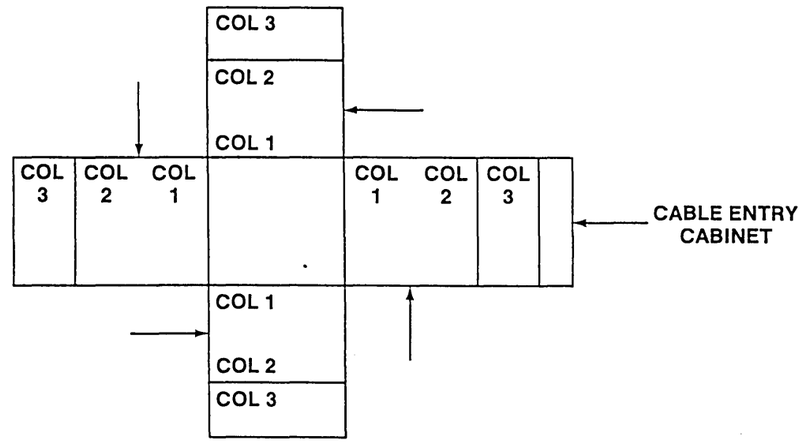
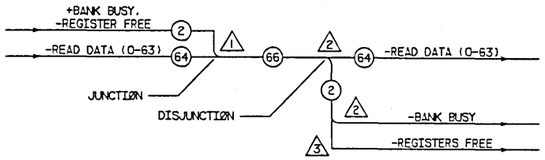
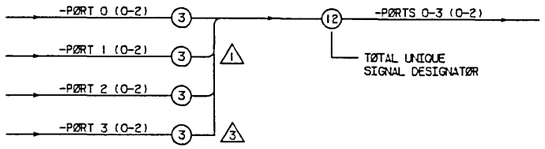


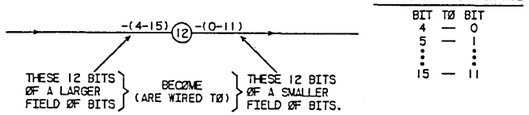
Figure I-2-1. Typical Cabinet Configuration

HIGHWAYING



1. CURVING THE LINE INTØ THE HIGHWAY INDICATES THE SIGNAL(S) JØINS THE HIGHWAY (JUNCTIØN).
2. CURVING THE LINE ØUT ØF THE HIGHWAY INDICATES THE SIGNAL(S) LEAVES THE HIGHWAY (DISJUNCTIØN).
3. ALL ØTHER LINE CØRNERS (WHERE LINES SIMPLY CHANGE DIRECTIØN) ARE SQUARE.

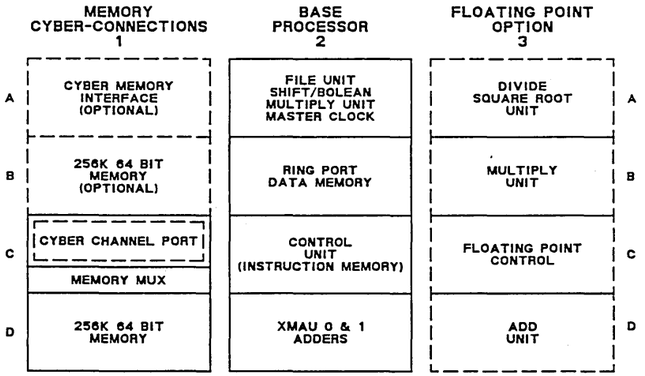




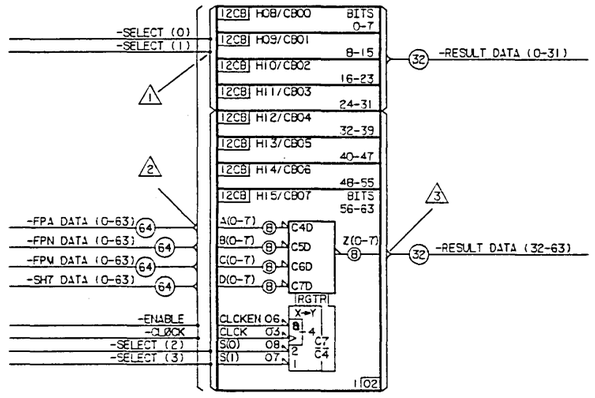
BIT DESIGNATIØN CHANGE

BIT	TØ	BIT
4	—	0
5	—	1
⋮		⋮
15	—	11

CYBERPLUS CABINET CØNFIGURATIØN

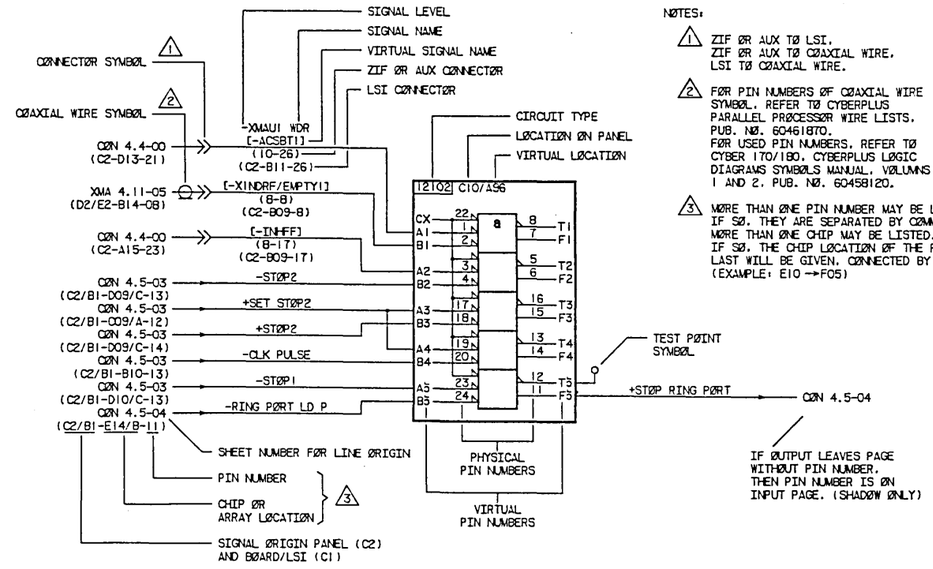


STACKING AND BRACKETING



1. A SØLDER PØINT ØN A BRACKET INDICATES THAT THE SIGNAL(S) GØ TØ THE SAME PIN(S) ØN EACH ARRAY/CHIP.
2. INDICATES DATA IS DISTRIBUTED AS DEFINED BY THE SIGNAL INFØRMATIØN INSIDE THE ARRAY/CHIP ENCLØSURE.
3. INDICATES DATA IS MERGED AS DEFINED BY THE SIGNAL INFØRMATIØN INSIDE THE ARRAY/CHIP ENCLØSURE.

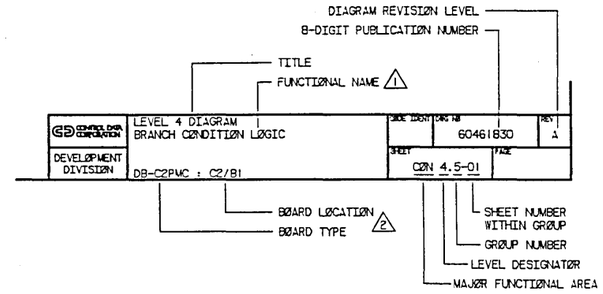
ENTRANCE AND EXIT LINE LABELING



NØTES:

1. ZIF ØR AUX TØ LSI, ZIF ØR AUX TØ CØAXIAL WIRE, LSI TØ CØAXIAL WIRE.
2. FØR PIN NUMBERS ØF CØAXIAL WIRE SYMBØL, REFER TØ CYBERPLUS PARALLEL PRØCESSØR WIRE LISTS, PUB. NØ. 60461870. FØR USED PIN NUMBERS, REFER TØ CYBER 170/180, CYBERPLUS LØGIC DIAGRAMS SYMBØLS MANUAL, VØLUMES 1 AND 2, PUB. NØ. 60458120.
3. MØRE THAN ØNE PIN NUMBER MAY BE LISTED. IF SØ, THEY ARE SEPARATED BY CØMMAS. MØRE THAN ØNE CHIP MAY BE LISTED. IF SØ, THE CHIP LØCATIØN ØF THE FIRST AND LAST WILL BE GIVEN, CØNNECTED BY AN ARRØW. (EXAMPLE: E10 → F05)

TITLE BLØCK LABELING

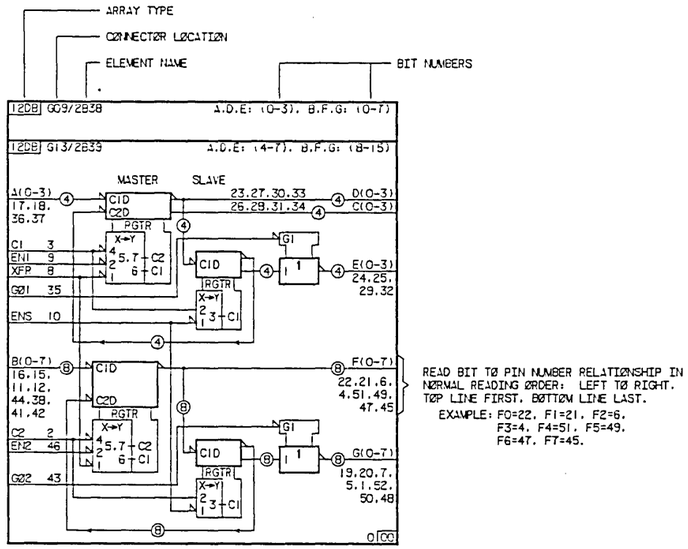


1. THE FUNCTIØNAL NAME IS A DESCRIPTIØN ØF THE LØGIC CØNTAINED ØN THAT PARTICULAR L4 DIAGRAM SHEET.
2. THE PANEL LØCATIØN CØNSISTS ØF THE RØW, LETTER, AND CØLUMN NUMBER ØF THE PANEL LØCATIØN.

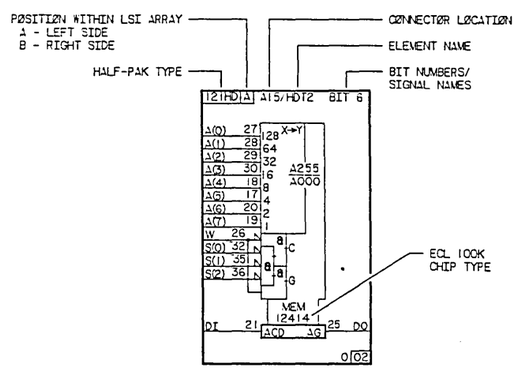
KEY: 1 REV A

Figure I-2-2. Key-to-Symbols Diagram (Sheet 1 of 2)

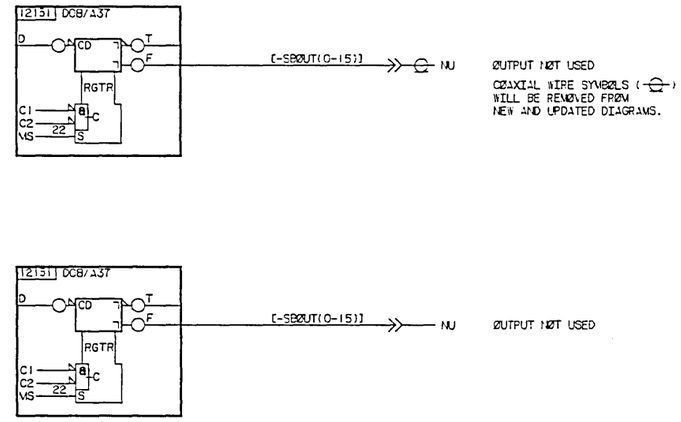
ARRAY SYMBØLS AND LABELS

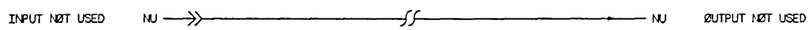


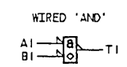
HALF-PAK ARRAY SYMBØLS AND LABELS



NØT USED LABELING







TWØ LØGIC SIGNAL CARRYING INPUT LINES PHYSICALLY WIRED TØGETHER TØ ØNE LØGIC CARRYING ØUTPUT LINE. LØWS ØN BØTH INPUT LINES PASS A LØW TØ THE ØUTPUT LINE.

Figure I-2-2. Key-to-Symbols Diagram (Sheet 2 of 2)

II. SYSTEM CLOCK

1. CLOCK PYRAMID (CLK)

SYSTEM FUNCTION

The clock pyramid provides and distributes synchronized clock pulses throughout the CYBERPLUS subsystem.

GENERAL DESCRIPTION

The master clock is an oscillator working at 21 nanoseconds, which is the cycle time of the clock pulses used in the CYBERPLUS. Attention must be paid to the wire-lengths and cable-lengths in a CYBERPLUS subsystem so that time zero of a clock pulse occurs at the same time throughout an entire single subsystem or multiple subsystems.

LOCATION

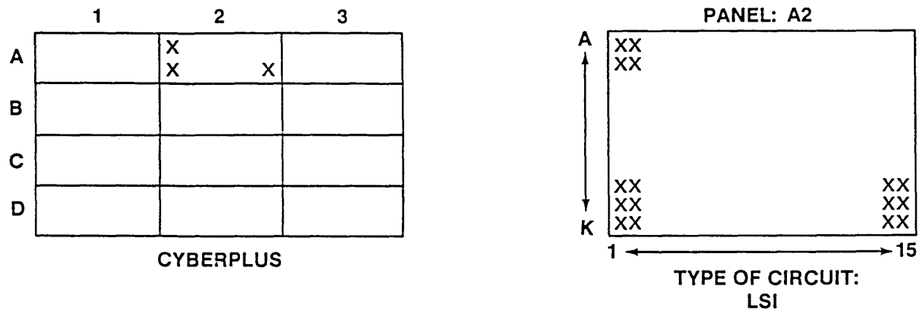


Figure II-1-1. Location of Clock Pyramid Logic Circuits

FUNCTIONAL DESCRIPTION

The clock pulses are propagated throughout a base processor by five levels of fanout circuits. Tuning of the clock to bring all time zeros into synchronization at the logic gate level is usually done between clock levels two and three or between three and four by varying the coaxial wire lengths entering fanouts. However, some clock pulses in certain logic areas are required at times 0 or time 10.5 plus or minus 2 to 3 nanoseconds. These times are achieved by varying individual clock wire lengths at the gate level. The tuning of the clock by using varying lengths of wire is initially done during manufacturing. Clock tuning can be done in the field by using the following guidelines: one nanosecond of delay is achieved by adding approximately 7.5 inches of clock coaxial wire.

In the floating point unit (FPU), there are two departures from the clocking in the base processor. One, in the divide/square root functional unit, employs frequency-doubling fanouts operating with a clock pulse of 10.5 nanoseconds, which is twice as fast as the master clock; and the second employs a timing chain to control the intermediate operations in those areas where multiple clock cycles are required to complete a function. (The integer multiply unit also employs a timing chain to control its intermediate operations.)

The above information is for one base processor. In a system where there is more than one base processor, timing must be synchronized between base processors. To achieve that, all base processors in a subsystem must be driven by a clock fanout from the base processor with the channel ring port (CRP). The connections between the level one oscillator and the level two fanout circuits must be changed so that all the base processors get their timing pulses from the same source. Additionally, it is necessary to see that there is no discernable difference in the start of each clock cycle from processor to processor. This is done by routing the clock pulses going to each base processor through equal length cables (usually 18-20 ft) including the clock signals to the processor in the clocks own cabinet.

When the direct memory access unit (DMAU) with central memory interface (CMI) option is installed, all base processors with CRPs must have their oscillators disabled except the subsystem with the DMAU with CMI. The subsystems must then be connected so that all base processors are driven by the clock fanout from that processor. The connections between the one oscillator and the level two fanouts in all subsystems must be changed so that each separate subsystem's clock pulses are routed through the DMAU panel before going directly to the base processors from the single clock source. Again, it is necessary that there is no discernable difference in the start of each clock cycle from DMAU to DMAU, processor to processor, and from subsystem to subsystem.

TIMING

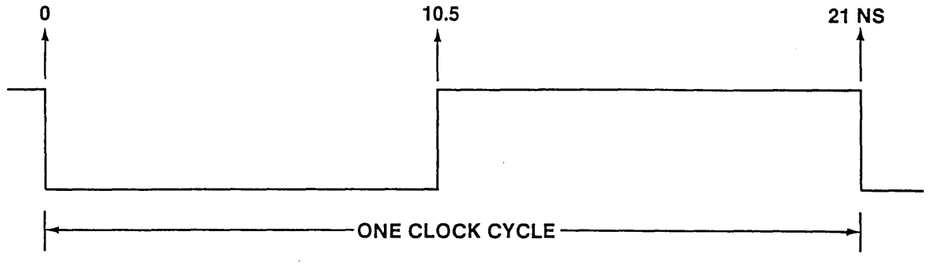
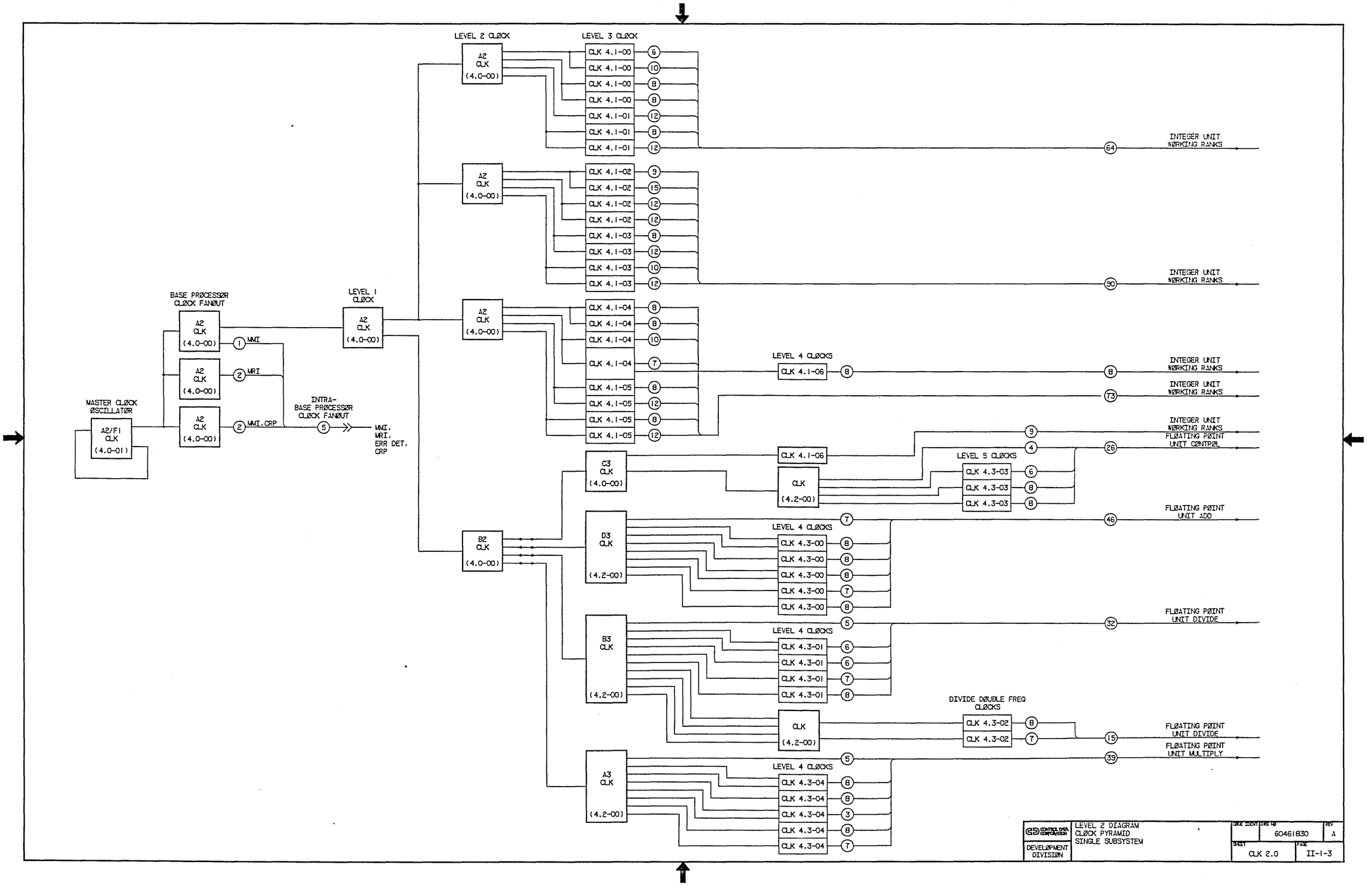
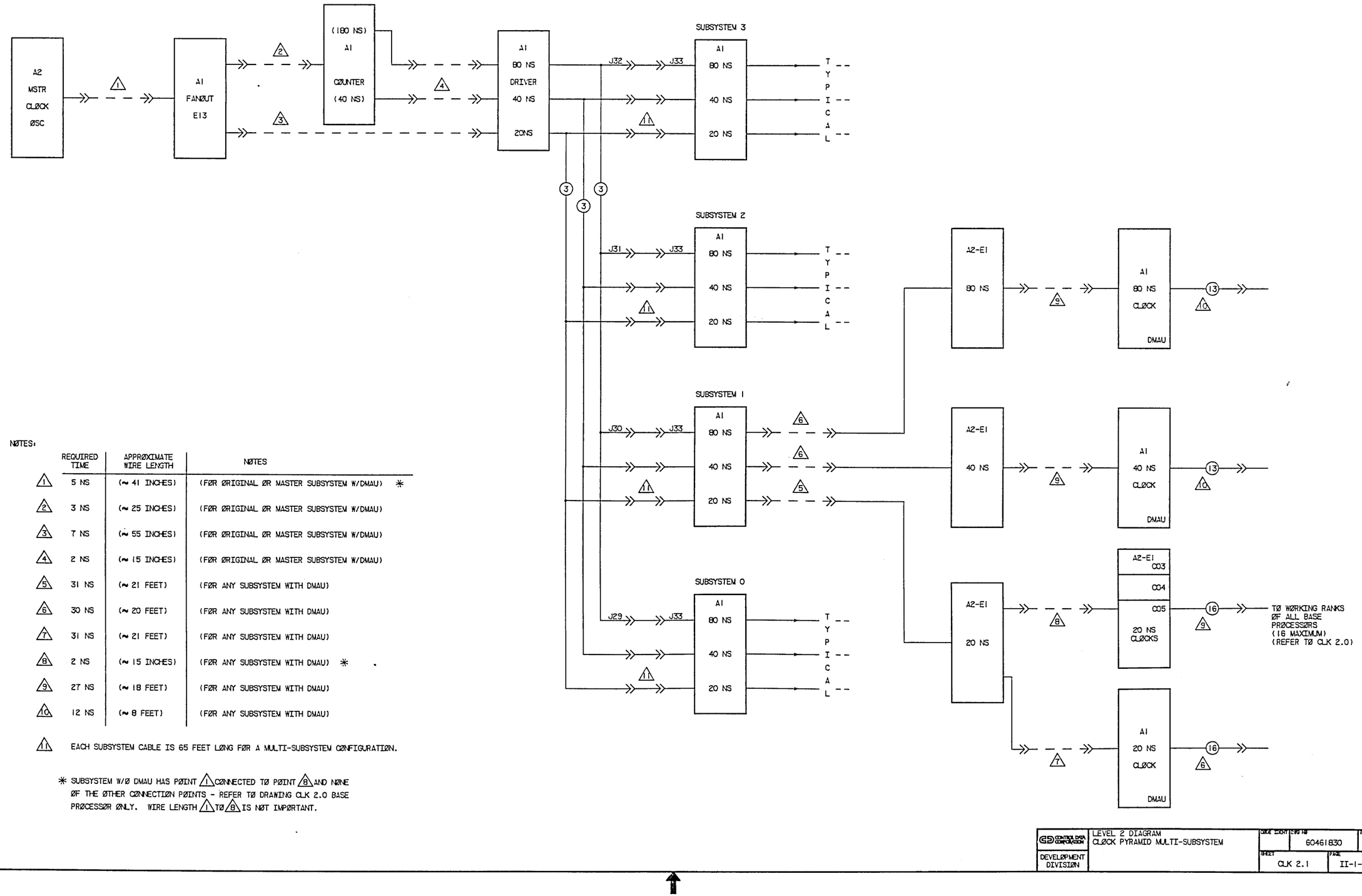


Figure II-1-2. CYBERPLUS Clock Cycle


LEVEL 2 CLØCK
LEVEL 3 CLØCK
A2 CLK (4.0-00)
CLK 4.1-00 6
CLK 4.1-00 10
CLK 4.1-00 8
CLK 4.1-00 8
CLK 4.1-01 12
CLK 4.1-01 8
CLK 4.1-01 12
64
INTEGER UNIT WØRKING RANKS
CLK 4.1-02 9
CLK 4.1-02 15
CLK 4.1-02 12
CLK 4.1-02 12
CLK 4.1-03 8
CLK 4.1-03 12
CLK 4.1-03 10
CLK 4.1-03 12
90
INTEGER UNIT WØRKING RANKS
CLK 4.1-04 8
CLK 4.1-04 8
CLK 4.1-04 10
CLK 4.1-04 7
CLK 4.1-05 8
CLK 4.1-05 12
CLK 4.1-05 8
CLK 4.1-05 12
LEVEL 4 CLØCKS
CLK 4.1-06 8
8
INTEGER UNIT WØRKING RANKS
73
INTEGER UNIT WØRKING RANKS
BASE PRØCESSØR CLØCK FANØUT
LEVEL 1 CLØCK
A2 CLK (4.0-00)
1 MMI
2 MRI
2 MMI.CRP
MASTER CLØCK ØSCILLATØR
A2/FI CLK (4.0-01)
INTRA-BASE PRØCESSØR CLØCK FANØUT
5
MMI, MRI, ERR DET, CRP
CLK 4.1-06
9
4
26
INTEGER UNIT WØRKING RANKS
FLØATING PØINT UNIT CØNTRØL
LEVEL 5 CLØCKS
CLK 4.3-03 6
CLK 4.3-03 8
CLK 4.3-03 8
C3 CLK (4.0-00)
CLK (4.2-00)
B2 CLK (4.0-00)
D3 CLK (4.2-00)
7
46
FLØATING PØINT UNIT ADD
LEVEL 4 CLØCKS
CLK 4.3-00 8
CLK 4.3-00 8
CLK 4.3-00 8
CLK 4.3-00 7
CLK 4.3-00 8
B3 CLK (4.2-00)
5
32
FLØATING PØINT UNIT DIVIDE
LEVEL 4 CLØCKS
CLK 4.3-01 6
CLK 4.3-01 6
CLK 4.3-01 7
CLK 4.3-01 8
DIVIDE DØUBLE FREQ CLØCKS
CLK 4.3-02 8
CLK 4.3-02 7
15
FLØATING PØINT UNIT DIVIDE
39
FLØATING PØINT UNIT MULTIPLY
A3 CLK (4.2-00)
5
LEVEL 4 CLØCKS
CLK 4.3-04 8
CLK 4.3-04 8
CLK 4.3-04 3
CLK 4.3-04 8
CLK 4.3-04 7
CONTROL DATA CORPORATION
DEVELØPMENT DIVISION
LEVEL 2 DIAGRAM
CLØCK PYRAMID
SINGLE SUBSYSTEM
CODE IDENT
DWG NO
60461830
REV
A
SHEET
CLK 2.0
PAGE
II-1-3



NØTES:

	REQUIRED TIME	APPRØXIMATE WIRE LENGTH	NØTES
1	5 NS	(≈ 41 INCHES)	(FØR ØRIGINAL ØR MASTER SUBSYSTEM W/DMAU) ✳
2	3 NS	(≈ 25 INCHES)	(FØR ØRIGINAL ØR MASTER SUBSYSTEM W/DMAU)
3	7 NS	(≈ 55 INCHES)	(FØR ØRIGINAL ØR MASTER SUBSYSTEM W/DMAU)
4	2 NS	(≈ 15 INCHES)	(FØR ØRIGINAL ØR MASTER SUBSYSTEM W/DMAU)
5	31 NS	(≈ 21 FEET)	(FØR ANY SUBSYSTEM WITH DMAU)
6	30 NS	(≈ 20 FEET)	(FØR ANY SUBSYSTEM WITH DMAU)
7	31 NS	(≈ 21 FEET)	(FØR ANY SUBSYSTEM WITH DMAU)
8	2 NS	(≈ 15 INCHES)	(FØR ANY SUBSYSTEM WITH DMAU) ✳
9	27 NS	(≈ 18 FEET)	(FØR ANY SUBSYSTEM WITH DMAU)
10	12 NS	(≈ 8 FEET)	(FØR ANY SUBSYSTEM WITH DMAU)

11 EACH SUBSYSTEM CABLE IS 65 FEET LØNG FØR A MULTI-SUBSYSTEM CØNFIGURATIØN.

✳ SUBSYSTEM W/Ø DMAU HAS PØINT 1 CØNNECTED TØ PØINT 8 AND NØNE ØF THE ØTHER CØNNECTIØN PØINTS - REFER TØ DRAWING CLK 2.0 BASE PRØCESSØR ØNLY. WIRE LENGTH 1 TØ 8 IS NØT IMPØRTANT.

CONTROL DATA CORPORATION	LEVEL 2 DIAGRAM CLØCK PYRAMID MULTI-SUBSYSTEM	CØDE IDENT	DRG NØ 60461830 REV A
DEVELØPMENT DIVISIØN		SHEET CLK 2.1	PAGE II-1-5

MASTER CLØCK FANØUT

121HB|A KØ2/7B5Ø-A/F
121HB|A KØ2/7B5Ø-B/F
121HB|A KØ2/7B5Ø-C/F
121HB|A KØ2/7B5Ø-D/F
121HE|B KØ2/7B51-E/F
121HE|B KØ2/7B51-F/F

[-CLØCK(00)]
[-CLØCK(01)] (A2-1-BS11) — (C1/P-P1C-91) MMI 4.0-00
[+CLØCK(02)] (A2-1-BR13) NU
[+CLØCK(03)] (A2-1-BM15) NU
[-CLØCK(04)] (A2-1-BW10) — (C1/E-P1C-56) MRI 4.0-05
[-CLØCK(05)] (A2-1-BP12) — (C1/F-P1C-39) MRI 4.1-03
[+CLØCK(06)] (A2-1-BP13)
[+CLØCK(07)] (A2-1-BK17)
-SYSCLK
[-CLØCK(08)] (A2-1-BT11) — (C1/B-D-P4-9) MEL 4.0-04 (C1/D-D08-22)
[-CLØCK(09)] (A2-1-BR12) — (C1/C-P1C-149) CRP 4.2-06 (C1/C-G11/B-23) 1
[+CLØCK(10)] (A2-1-BP17)
[+CLØCK(11)] (A2-1-BR18)

[-BPØCLK] (A2-1-BT09)
(A2-1-BW09) (A2-1-BS10)

LEVEL 1 CLØCK
-MASTER CLØSC(0) [MØSC]
[-MCKØUT(0)] [-MCKØUT(1)] [NMØSC0] [NMCKØT(0)]
(A2-1-BS13) NU
(A2-1-BR14) NU 4
[-ØSCØUT] (A2-1-AG08)
[-ØSØUT(1)] (A2-1-AH08)
(A2-1-BP14) (A2-1-BM16)
(A2-1-BU10) B45 11.0 NS (A2-1-AJ05) -LEVEL 1 CLØCK [-EXTCLK]
(A2-1-BN16)
(A2-1-BR17)
3

CLK 4.0-01 (A2/F1-C03-01)(A2-1-AD06) [-MASØSC]
2
[+MASØSC(0)] (A2-1-AE08)
[+MASØSC(1)] (A2-1-AE07)
(A2-1-BP18) (A2-1-BN19)
5

(A2-1-BR10) C11 2.5 NS (B2-1-AF09)

LEVEL 2 CLØCK

121HB|A B02/7B11-A/D
121HB|A B02/7B11-C/D
121HB|A B02/7B11-D/D

[-7B23-CX] (A2-1-AF05) D10 3.6 NS (A2-1-BU02) CLK 4.1-00 LEVEL 3 CLØCK (A2-K01-15,41)
[-7B29-CX] (A2-1-AE04) D28 8.0 NS (A2-3-BU18) CLK 4.1-00 LEVEL 3 CLØCK (A2-K15-15,41)
[-7B12-CX] (A2-1-AH07) D16 5.0 NS (A2-1-AF04) CLK 4.1-01 LEVEL 3 CLØCK (A2-B02-41)
[-7B17-CX] (A2-1-AE05) D24 7.0 NS (A2-1-BF02) CLK 4.1-01 LEVEL 3 CLØCK (A2-G01-15,41)
[-7B25-CX] (A2-1-AG04) D28 8.0 NS (A2-1-AB02) CLK 4.1-02 LEVEL 3 CLØCK (A2-A01-15,41)
[-7B33-CX] (A2-1-AJ04) D10 3.6 NS (A2-1-BK10) CLK 4.1-02 LEVEL 3 CLØCK (A2-H03-15,41)
[-7B13-CX] (A2-1-AG05) D20 6.0 NS (A2-1-AF02) CLK 4.1-03 LEVEL 3 CLØCK (A2-B01-15,41)
[-7B19-CX] (A2-1-AH04) D20 6.0 NS (A2-1-BK02) CLK 4.1-03 LEVEL 3 CLØCK (A2-H01-15,41)
[-7B27-CX] (A2-1-AH06) D28 8.0 NS (A2-3-BP18) CLK 4.1-04 LEVEL 3 CLØCK (A2-J15-15,41)
[-7B35-CX] (A2-1-AF06) D10 3.6 NS (A2-3-BF14) CLK 4.1-04 LEVEL 3 CLØCK (A2-G14-15,41)
[-7B15-CX] (A2-1-AH05) D16 5.0 NS (A2-1-AK02) CLK 4.1-05 LEVEL 3 CLØCK (A2-C01-15,41)
[-7B21-CX] (A2-1-AG06) D20 6.0 NS (A2-1-BP02) CLK 4.1-05 LEVEL 3 CLØCK (A2-J01-15,41)
[-7B32-A0] (B2-1-AG09) D29 8.2 NS (A2-1-AA07) CLK 4.1-06 LEVEL 4 CLØCK (A2-A02-43)

121HB|B A02/7B16-A/C
-LEVEL 1 CLØCK [-CLØCK(101)]
[-CLØCK(212)] (B2-1-AG04) (D3-3-AG20) CLK 4.2-00 LEVEL 3 CLØCK (D3-E15/A-15)
[-CLØCK(213)] (B2-1-AH08) (A3-3-BV14) CLK 4.2-00 LEVEL 3 CLØCK (A3-K15/B-41)
[+CLØCK(215)]
[+CLØCK(214)]
(B2-1-AH07) 1.5 NS (B2-1-AH02)

LEVEL 3 CLØCK
121HB|B A02/7B16-B/C
+LEVEL 2 CLØCK [+CLØCK(214)]
[-CLØCK(302)] (B2-1-AG02) (C3-1-AB02) CLK 4.2-00 LEVEL 4 CLØCK (C3-B01-15)
[-CLØCK(215)] (B2-1-AH10) (B3-1-BV14) CLK 4.2-00 LEVEL 3 CLØCK (B3-K03/B-41)

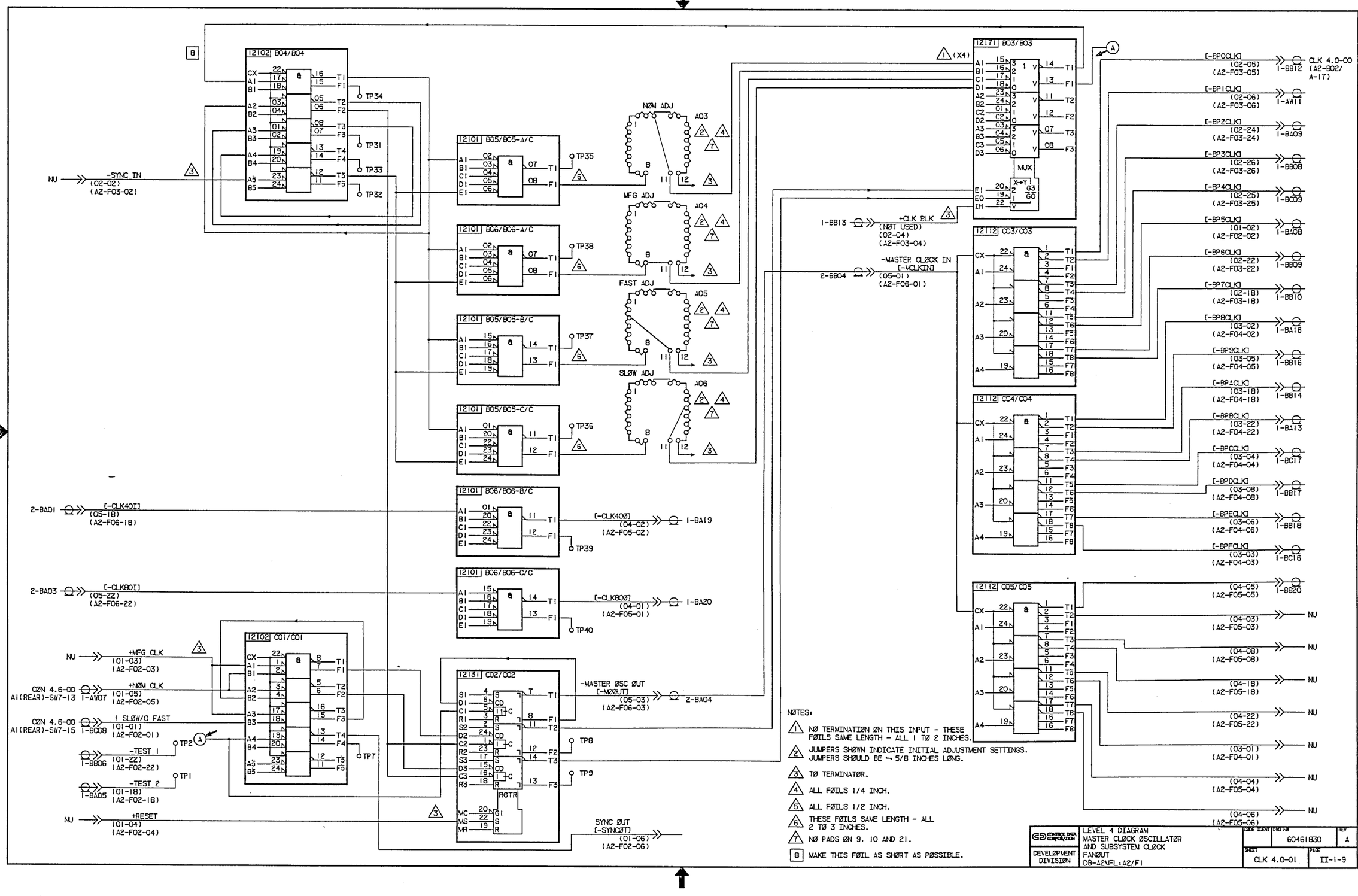
121HB|B A02/7B16-C/C
NU (B2-1-AG08)

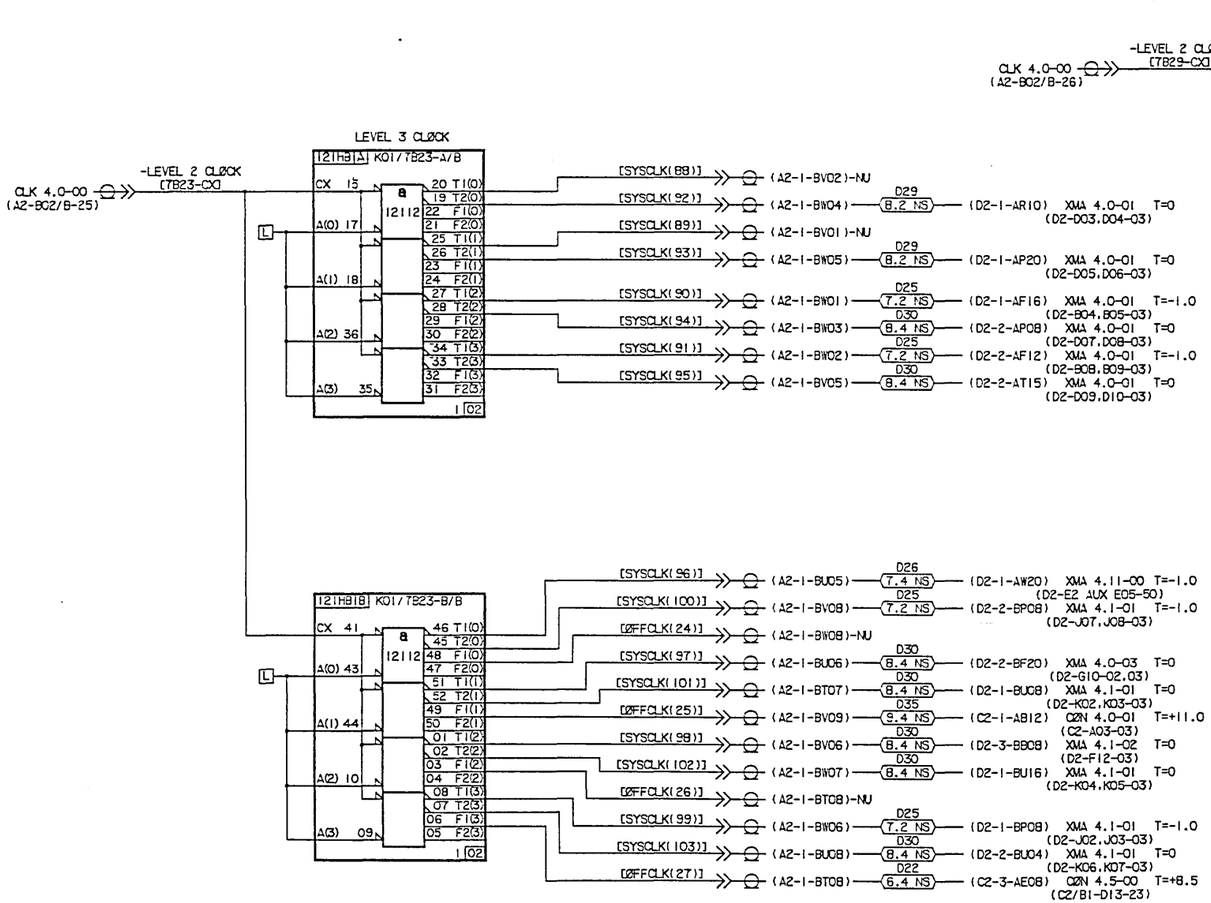
LSII-B2

NØTES:

1. USED ØN FIRST BASE PRØCESSØR ØNLY.
2. IN A MULTIPLE PRØCESSØR SYSTEM, THE SØURCE ØF THIS CLK IS DETERMINED BY THE BASE PRØCESSØR NUMBER. (SEE CLK 4.0-01 C03,C04, AND C05 FANØUTS).
3. DASHED LINE IS USED ØNLY IF THE LØGIC 0 PØRTIØN ØF THE CLØCK AT C2-A04-03 EXCEEDS THE LØGIC 1 PØRTIØN DURING INITIAL SYMMETRY ADJUSTMENT.
4. ADJUST THIS CØAX TØ ACHIEVE SYMMETRY IF THE LØGIC 1 PØRTIØN ØF THE CLØCK AT C2-A04-03 EXCEEDS THE LØGIC 0 PØRTIØN.
5. ADJUST THIS CØAX TØ ACHIEVE SYMMETRY IF THE LØGIC 0 PØRTIØN ØF THE CLØCK AT C2-A04-03 EXCEEDS THE LØGIC 1 PØRTIØN.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM CLØCK PYRAMID MASTER CLØCK ØSCILLATØR & FANØUT LEVEL 1 & 2 FANØUT (INTEGER UNIT) DB-A2MUL:A2, DB-B2RPU:B2	DRAWING NUMBER	REV A
DEVELØPMENT DIVISIØN		60461830	
		SHEET CLK 4.0-00	PAGE II-1-7


12102 B04/B04
12101 B05/B05-A/C
12101 B06/B06-A/C
12101 B05/B05-B/C
12101 B05/B05-C/C
12101 B06/B06-B/C
12101 B06/B06-C/C
12102 C01/C01
12131 C02/C02
12171 B03/B03
12112 C03/C03
12112 C04/C04
12112 C05/C05
NØM ADJ
MFG ADJ
FAST ADJ
SLØW ADJ
A03
A04
A05
A06
TP31
TP32
TP33
TP34
TP35
TP36
TP37
TP38
TP39
TP40
TP1
TP2
TP7
TP8
TP9
NU
-SYNC IN (02-02) (A2-F03-02)
2-BA01 [-CLK40I] (05-18) (A2-F06-18)
2-BA03 [-CLKBØI] (05-22) (A2-F06-22)
[-CLK40Ø] (04-02) (A2-F05-02) 1-BA19
[-CLKBØØ] (04-01) (A2-F05-01) 1-BA20
+MFG CLK (01-03) (A2-F02-03)
CØN 4.6-00 A1(REAR)-SWT-13 1-AW07 +NØM CLK (01-05) (A2-F02-05)
CØN 4.6-00 A1(REAR)-SWT-15 1-BC08 1 SLØW/O FAST (01-01) (A2-F02-01)
1-BB06 -TEST 1 (01-22) (A2-F02-22)
1-BA05 -TEST 2 (01-18) (A2-F02-18)
+RESET (01-04) (A2-F02-04)
1-BB13 +CLK BLK (NØT USED) (02-04) (A2-F03-04)
2-BB04 -MASTER CLØCK IN [-WCLKIN] (05-01) (A2-FC6-01)
-MASTER ØSC ØUT [-MØØUT] (05-03) (A2-F06-03) 2-BA04
SYNC ØUT [-SYNCØT] (01-06) (A2-F02-06)
[-BP0CLK] (02-05) (A2-F03-05) CLK 4.0-00 (A2-B02/A-17) 1-BB12
[-BP1CLK] (02-06) (A2-F03-06) 1-AW11
[-BP2CLK] (02-24) (A2-F03-24) 1-BA09
[-BP3CLK] (02-26) (A2-F03-26) 1-BB08
[-BP4CLK] (02-25) (A2-F03-25) 1-BC09
[-BP5CLK] (01-02) (A2-F02-02) 1-BA08
[-BP6CLK] (02-22) (A2-F03-22) 1-BB09
[-BP7CLK] (02-18) (A2-F03-18) 1-BB10
[-BP8CLK] (03-02) (A2-F04-02) 1-BA16
[-BP9CLK] (03-05) (A2-F04-05) 1-BB16
[-BPACLK] (03-18) (A2-F04-18) 1-BB14
[-BPBCLK] (03-22) (A2-F04-22) 1-BA13
[-BPCCLK] (03-04) (A2-F04-04) 1-BC17
[-BPDCLK] (03-08) (A2-F04-08) 1-BB17
[-BPECLK] (03-06) (A2-F04-06) 1-BB18
[-BPFCLK] (03-03) (A2-F04-03) 1-BC16
(04-05) (A2-F05-05) 1-BB20
(04-03) (A2-F05-03) NU
(04-08) (A2-F05-08) NU
(04-18) (A2-F05-18) NU
(04-22) (A2-F05-22) NU
(03-01) (A2-F04-01) NU
(04-04) (A2-F05-04) NU
(04-06) (A2-F05-06) NU
NØTES:
1 NØ TERMINATIØN ØN THIS INPUT - THESE FØILS SAME LENGTH - ALL 1 TØ 2 INCHES.
2 JUMPERS SHØWN INDICATE INITIAL ADJUSTMENT SETTINGS. JUMPERS SHØULD BE ¬ 5/8 INCHES LØNG.
3 TØ TERMINATØR.
4 ALL FØILS 1/4 INCH.
5 ALL FØILS 1/2 INCH.
6 THESE FØILS SAME LENGTH - ALL 2 TØ 3 INCHES.
7 NØ PADS ØN 9. 10 AND 21.
8 MAKE THIS FØIL AS SHØRT AS PØSSIBLE.
CONTROL DATA CORPORATION
DEVELØPMENT DIVISION
LEVEL 4 DIAGRAM
MASTER CLØCK ØSCILLATØR AND SUBSYSTEM CLØCK FANØUT
DB-A2WFL:A2/F1
CODE IDENT
DRG NO
60461830
REV
A
SHEET
CLK 4.0-01
SIZE
II-1-9

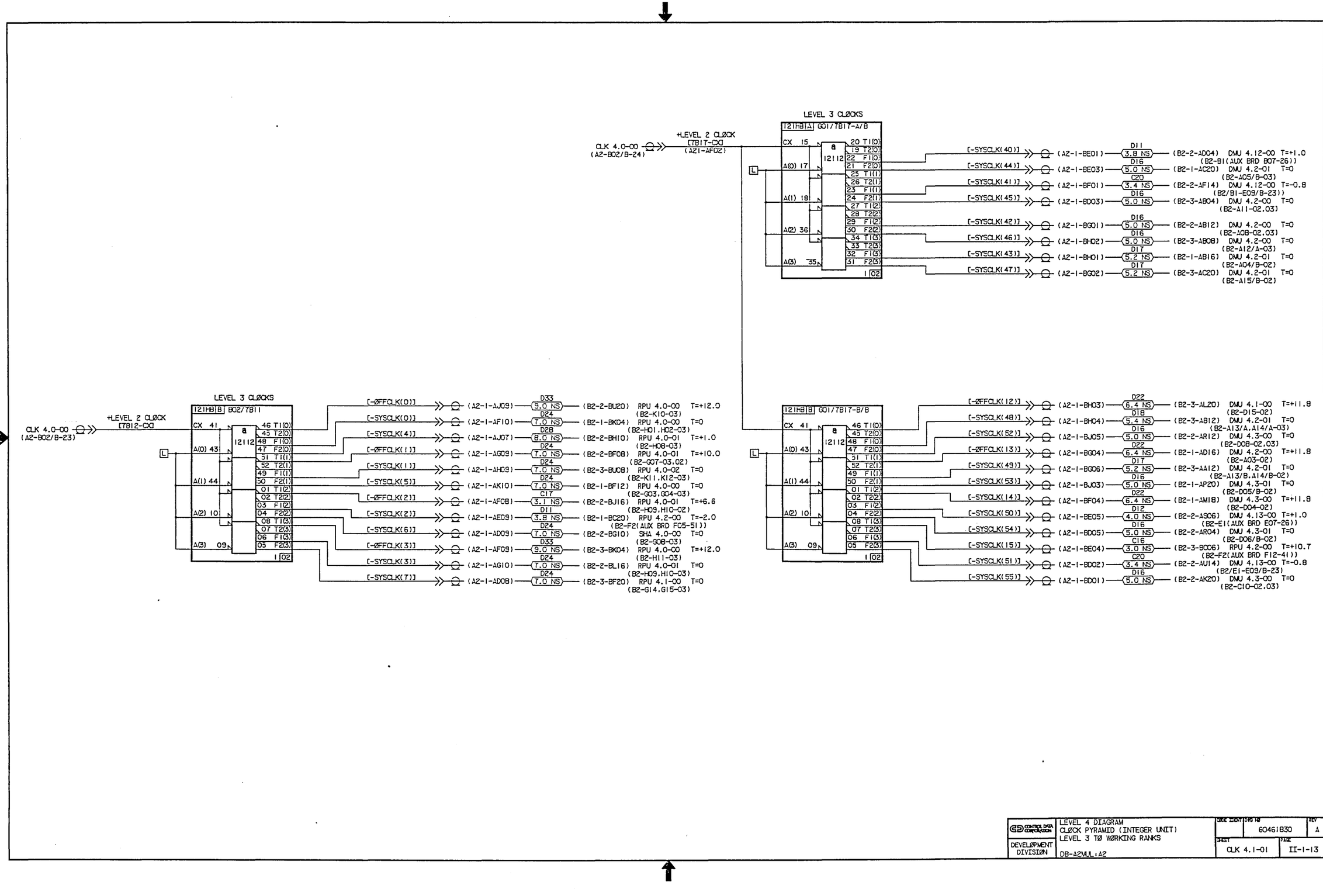


CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
CLØCK PYRAMID (INTEGER UNIT)
LEVEL 3 TØ WØRKING RANKS

DB-A2MUL:A2

CODE IDENT	DWG NO	REV
	60461830	A
SHEET	SIZE	
CLK 4.1-00	II-1-11	


LEVEL 3 CLØCKS
121HB1A G01/7B17-A/B
CLK 4.0-00 (A2-B02/B-24)
+LEVEL 2 CLØCK [7B17-CX] (A21-AF02)
CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35
8 12112
20 T1(0)
19 T2(0)
22 F1(0)
21 F2(0)
25 T1(1)
26 T2(1)
23 F1(1)
24 F2(1)
27 T1(2)
28 T2(2)
29 F1(2)
30 F2(2)
34 T1(3)
33 T2(3)
32 F1(3)
31 F2(3)
1 02
[-SYSCLK(40)] (A2-1-BE01) D11 3.8 NS (B2-2-AD04) DMU 4.12-00 T=+1.0 (B2-B1(AUX BRD B07-26))
[-SYSCLK(44)] (A2-1-BE03) D16 5.0 NS (B2-1-AC20) DMU 4.2-01 T=0 (B2-A05/B-03)
[-SYSCLK(41)] (A2-1-BF01) C20 3.4 NS (B2-2-AF14) DMU 4.12-00 T=-0.8 (B2/B1-E09/B-23))
[-SYSCLK(45)] (A2-1-BD03) D16 5.0 NS (B2-3-AB04) DMU 4.2-00 T=0 (B2-A11-02.03)
[-SYSCLK(42)] (A2-1-BG01) D16 5.0 NS (B2-2-AB12) DMU 4.2-00 T=0 (B2-A08-02.03)
[-SYSCLK(46)] (A2-1-BH02) D16 5.0 NS (B2-3-AB08) DMU 4.2-00 T=0 (B2-A12/A-03)
[-SYSCLK(43)] (A2-1-BH01) D17 5.2 NS (B2-1-AB16) DMU 4.2-01 T=0 (B2-A04/B-02)
[-SYSCLK(47)] (A2-1-BG02) D17 5.2 NS (B2-3-AC20) DMU 4.2-01 T=0 (B2-A15/B-02)
LEVEL 3 CLØCKS
121HB1B B02/7B11
CLK 4.0-00 (A2-B02/B-23)
+LEVEL 2 CLØCK [7B12-CX]
CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09
8 12112
46 T1(0)
45 T2(0)
48 F1(0)
47 F2(0)
51 T1(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)
1 02
[-ØFFCLK(0)] (A2-1-AJ09) D33 3.0 NS (B2-2-BU20) RPU 4.0-00 T=+12.0 (B2-K10-03)
[-SYSCLK(0)] (A2-1-AF10) D24 7.0 NS (B2-1-BK04) RPU 4.0-00 T=0 (B2-H01,H02-03)
[-SYSCLK(4)] (A2-1-AJ07) D28 8.0 NS (B2-2-BH10) RPU 4.0-01 T=+1.0 (B2-H08-03)
[-ØFFCLK(1)] (A2-1-AG09) D24 7.0 NS (B2-2-BF08) RPU 4.0-01 T=+10.0 (B2-G07-03.02)
[-SYSCLK(1)] (A2-1-AH09) D24 7.0 NS (B2-3-BU08) RPU 4.0-02 T=0 (B2-K11,K12-03)
[-SYSCLK(5)] (A2-1-AK10) D24 7.0 NS (B2-1-BF12) RPU 4.0-00 T=0 (B2-G03,G04-03)
[-ØFFCLK(2)] (A2-1-AF08) C17 3.1 NS (B2-2-BJ16) RPU 4.0-01 T=+6.6 (B2-H09,H10-02)
[-SYSCLK(2)] (A2-1-AE09) D11 3.8 NS (B2-1-BC20) RPU 4.2-00 T=-2.0 (B2-F2(AUX BRD F05-51))
[-SYSCLK(6)] (A2-1-AD09) D24 7.0 NS (B2-2-BG10) SHA 4.0-00 T=0 (B2-G08-03)
[-ØFFCLK(3)] (A2-1-AF09) D33 9.0 NS (B2-3-BK04) RPU 4.0-00 T=+12.0 (B2-H11-03)
[-SYSCLK(3)] (A2-1-AG10) D24 7.0 NS (B2-2-BL16) RPU 4.0-01 T=0 (B2-H09,H10-03)
[-SYSCLK(7)] (A2-1-AD08) D24 7.0 NS (B2-3-BF20) RPU 4.1-00 T=0 (B2-G14,G15-03)
121HB1B G01/7B17-B/B
CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09
8 12112
46 T1(0)
45 T2(0)
48 F1(0)
47 F2(0)
51 T1(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)
1 02
[-ØFFCLK(12)] (A2-1-BH03) D22 6.4 NS (B2-3-AL20) DMU 4.1-00 T=+11.8 (B2-D15-02)
[-SYSCLK(48)] (A2-1-BH04) D18 5.4 NS (B2-3-AB12) DMU 4.2-01 T=0 (B2-A13/A,A14/A-03)
[-SYSCLK(52)] (A2-1-BJ05) D16 5.0 NS (B2-2-AR12) DMU 4.3-00 T=0 (B2-D08-02.03)
[-ØFFCLK(13)] (A2-1-BG04) D22 6.4 NS (B2-1-AD16) DMU 4.2-00 T=+11.8 (B2-A03-02)
[-SYSCLK(49)] (A2-1-BG06) D17 5.2 NS (B2-3-AA12) DMU 4.2-01 T=0 (B2-A13/B,A14/B-02)
[-SYSCLK(53)] (A2-1-BJ03) D16 5.0 NS (B2-1-AP20) DMU 4.3-01 T=0 (B2-D05/B-02)
[-SYSCLK(14)] (A2-1-BF04) D22 6.4 NS (B2-1-AM18) DMU 4.3-00 T=+11.8 (B2-D04-02)
[-SYSCLK(50)] (A2-1-BE05) D12 4.0 NS (B2-2-AS06) DMU 4.13-00 T=+1.0 (B2-E1(AUX BRD E07-26))
[-SYSCLK(54)] (A2-1-BD05) D16 5.0 NS (B2-2-AR04) DMU 4.3-01 T=0 (B2-D06/B-02)
[-SYSCLK(15)] (A2-1-BE04) C16 3.0 NS (B2-3-BC06) RPU 4.2-00 T=+10.7 (B2-F2(AUX BRD F12-41))
[-SYSCLK(51)] (A2-1-BD02) C20 3.4 NS (B2-2-AU14) DMU 4.13-00 T=-0.8 (B2/E1-E09/B-23)
[-SYSCLK(55)] (A2-1-BD01) D16 5.0 NS (B2-2-AK20) DMU 4.3-00 T=0 (B2-C10-02.03)
CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 4 DIAGRAM
CLØCK PYRAMID (INTEGER UNIT)
LEVEL 3 TØ WØRKING RANKS
DB-A2MUL:A2
CODE IDENT
DWG NO 60461830
REV A
SHEET CLK 4.1-01
PAGE II-1-13

CLK 4.0-00 (A2-B02/C-27)

-LEVEL 2 CLØCK (T825-CX)

LEVEL 3 CLØCK

121HB|A| A01/7825-A/B

CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35

12112

20 T1(0)
19 T2(0)
22 F1(0)
21 F2(0)
25 T1(1)
26 T2(1)
23 F1(1)
24 F2(1)
27 T1(2)
28 T2(2)
29 F1(2)
30 F2(2)
34 T1(3)
33 T2(3)
32 F1(3)
31 F2(3)

1|02

[-CLKT0]	(A2-1-AA06)	D14 4.4 NS	(A2-3-BA09)	FGU 4.1-00 (A2-F1(AUX BRD F13-18))	W=+7.0
[-8802-C2]	(A2-1-AA02)	D17 5.2 NS	(A2-2-AT08)	MUL 4.0-00 (A2-E07/B-02)	T=+1.0
[-8822-C1]	(A2-1-AJ11)	D27 7.8 NS	(A2-2-BF08)	SBU 4.0-03 (A2-G07/A-03)	T=+15.0
[-CLKT5]	(A2-1-ACC6)	D31 8.6 NS	(A2-3-BA12)	FGU 4.1-00 (A2-F1(AUX BRD F13-02))	T=+8.3
[-8803-C1]	(A2-1-AA03)	D16 5.0 NS	(A2-1-AU16)	MUL 4.0-00 (A2-E04/B-02)	T=+1.0
[-2801-C1]	(A2-1-AB01)	D30 8.4 NS	(A2-1-AU20)	MUL 4.0-07 (A2-E05/A-03)	T=+15.0
[-8831-C1]	(A2-1-AA01)	D30 8.4 NS	(A2-2-BU16)	SBU 4.1-03 (A2-K09/A-03)	T=+15.0
[-1833-CLOCK]	(A2-1-AE01)	D18 5.4 NS	(A2-2-BF20)	SBU 4.1-01 (A2-G10-03)	T=+1.0
[-8804-C1]	(A2-1-AE03)	D17 5.2 NS	(A2-2-AU16)	MUL 4.0-08 (A2-E09/A-02)	T=+1.0
[-8802-C1]	(A2-1-ACD1)	D30 8.4 NS	(A2-2-AU08)	MUL 4.0-07 (A2-E07/A-03)	T=+15.0
[-8832-C1]	(A2-1-ADD2)	D30 8.4 NS	(A2-2-BF12)	SBU 4.1-03 (A2-G08/A-03)	T=+15.0
[-2801-C2]	(A2-1-ADD3)	C16 3.0 NS	(A2-1-AT20)	MUL 4.0-08 (A2-E05/B-02)	T=-1.0
[-8805-C1]	(A2-1-AA04)	D25 7.2 NS	(A2-3-AB12)	MUL 4.0-06 (A2-A13-02.03)	T=+3.0
[-8821-C1]	(A2-1-ADD1)	D30 8.4 NS	(A2-2-BU08)	SBU 4.0-03 (A2-K07/A-03)	T=+15.0
[-8841-C1]	(A2-1-ACD2)	B35 10.6 NS	(A2-2-BK12)	FGU 4.0-00 (A2-H08-03)	T=+17.0

LEVEL 3 CLØCK

121HB|B| A01/7825-B/B

CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09

12112

46 T1(0)
45 T2(0)
48 F1(0)
47 F2(0)
51 T1(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)

1|02

[-8806-C1]	(A2-1-ADD4)	D25 7.2 NS	(A2-3-AB04)	MUL 4.0-06 (A2-A11-02.03)	T=+3.0
[-8810-C1]	(A2-1-ADD5)	D15 4.8 NS	(A2-2-AU20)	MUL 4.0-08 (A2-E10/A-02)	T=+1.0
[-8843-C1]	(A2-1-AF01)	B35 10.6 NS	(A2-3-BK16)	FGU 4.0-00 (A2-H14-03)	T=+17.0
[-2807-C1]	(A2-1-ACC4)	D25 7.2 NS	(A2-2-AB12)	MUL 4.0-06 (A2-A08-02.03)	T=+3.0
[-8811-C1]	(A2-1-AB06)	D14 4.4 NS	(A2-3-AU04)	MUL 4.0-08 (A2-E11/A-02)	T=+1.0
[-2808-C1]	(A2-1-AB04)	D25 7.2 NS	(A2-1-AF20)	MUL 4.0-06 (A2-B05-02.03)	T=+3.0
[-8812-C1]	(A2-1-AA05)	C14 2.8 NS	(A2-3-AU20)	MUL 4.0-08 (A2-E15-02.03)	T=-1.0
[-8809-C1]	(A2-1-ACD5)	D24 7.0 NS	(A2-1-AF12)	MUL 4.0-06 (A2-B03-02.03)	T=+3.0
[-8813-C1]	(A2-1-AB05)	C14 2.8 NS	(A2-3-AB20)	MUL 4.0-08 (A2-A15-02.03)	T=-1.0

CLK 4.0-00 (A2-B02/C-28)

-LEVEL 2 CLØCK (T833-CX)

LEVEL 3 CLØCK

121HB|A| H03/7833-A/B

CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35

12112

20 T1(0)
19 T2(0)
22 F1(0)
21 F2(0)
25 T1(1)
26 T2(1)
23 F1(1)
24 F2(1)
27 T1(2)
28 T2(2)
29 F1(2)
30 F2(2)
34 T1(3)
33 T2(3)
32 F1(3)
31 F2(3)

1|02

[-SYSCLK(108)]	(A2-1-BK09)	D26 7.4 NS	(D2-1-BC16)	ADD 4.0-02 (D2-F04/B→G04/B-03)	T=-1.0
[-SYSCLK(112)]	(A2-1-BL10)	D26 7.4 NS	(D2-2-BC12)	ADD 4.1-02 (D2-F08/B,G08/B-03)	T=-1.0
[-ØFFCLK(32)]	(A2-1-BH08)	D29 8.2 NS	(D2-3-AF04)	XMA 4.0-03 (D2-B11-02.03)	T=+10.0
[-SYSCLK(109)]	(A2-1-BJ09)	D30 8.4 NS	(D2-1-BA17)	ADD 4.0-00 (D2-F04/A,G04/A-02)	T=0
[-SYSCLK(113)]	(A2-1-BJ08)	D30 8.4 NS	(D2-2-BA13)	ADD 4.1-00 (D2-F08/A,G08/A-02)	T=0
[-ØFFCLK(33)]	(A2-1-BJ11)	D28 8.0 NS	(D2-2-AF20)	XMA 4.0-03 (D2-B10-02.03)	T=+10.0
[-SYSCLK(110)]	(A2-1-BL09)	D30 8.4 NS	(D2-2-BB01)	ADD 4.1-02 (D2-F05/B-03)	T=0
[-SYSCLK(114)]	(A2-1-BM09)	D30 8.4 NS	(D2-1-BK08)	ADD 4.0-00 (D2-H02/A-02)	T=0
[-ØFFCLK(34)]	(A2-1-BM11)	D28 8.0 NS	(D2-2-AB16)	XMA 4.0-03 (D2-A09-02.03)	T=+10.0
[-SYSCLK(111)]	(A2-1-BM10)	D30 8.4 NS	(D2-2-BE01)	ADD 4.1-00 (D2-G05/A,F05/A-02)	T=0
[-SYSCLK(115)]	(A2-1-BM08)	D30 8.4 NS	(D2-1-BK12)	ADD 4.0-00 (D2-H03/A-02)	T=0
[-ØFFCLK(35)]	(A2-1-BN11)	D28 8.0 NS	(D2-2-AB12)	XMA 4.0-03 (D2-A08-02.03)	T=+10.0

LEVEL 3 CLØCK

121HB|B| H03/7833-B/B

CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09

12112

46 T1(0)
45 T2(0)
48 F1(0)
47 F2(0)
51 T1(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)

1|02

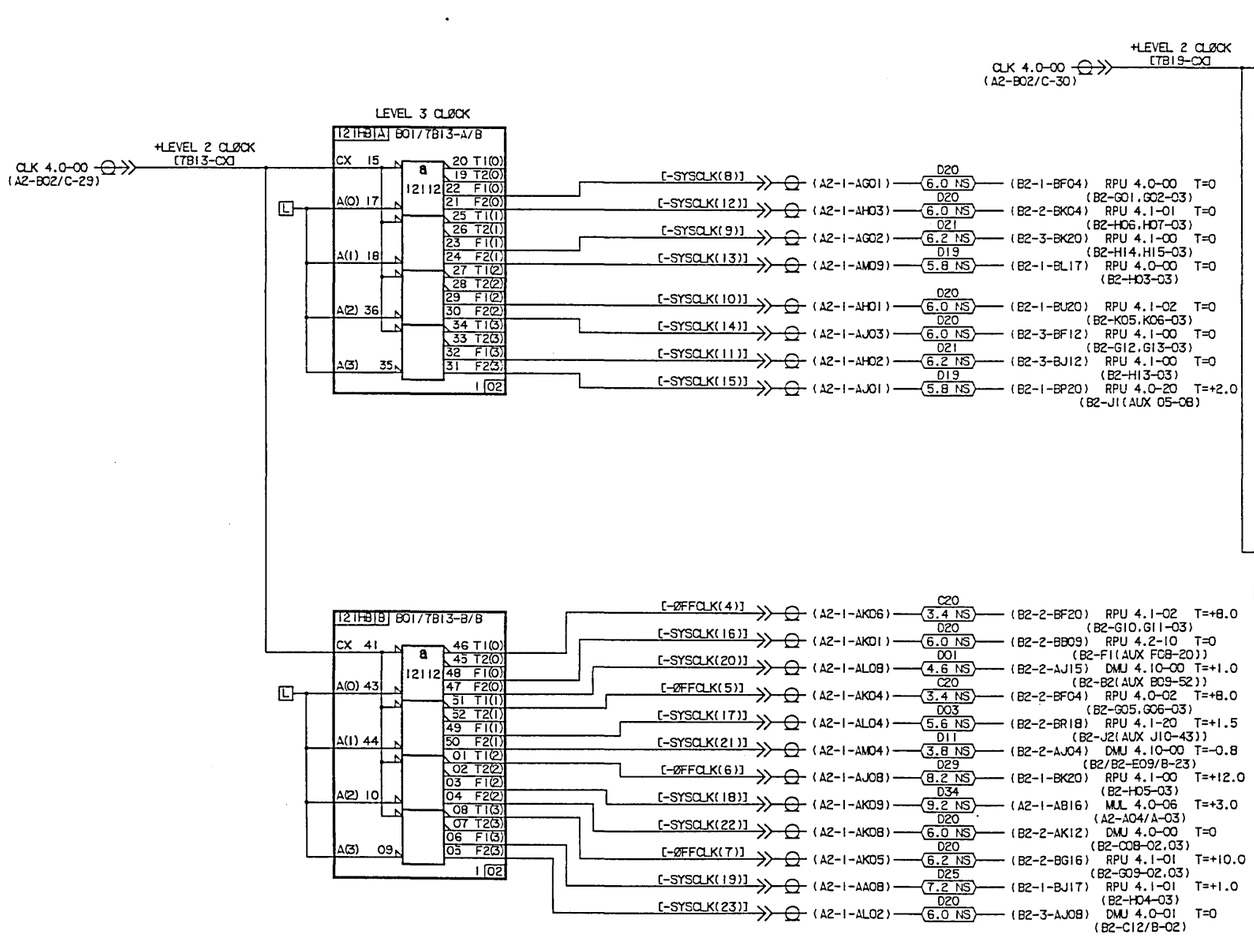
[-SYSCLK(116)]	(A2-1-BM12)	D30 8.4 NS	(D2-2-BK04)	ADD 4.1-00 (D2-H06/A-02)	T=0
[-SYSCLK(120)]	(A2-1-BM13)	D23 6.8 NS	(D2-2-AU04)	XMA 4.10-00 (D2-E1(AUX E06-07))	T=-1.0
[-ØFFCLK(36)]	(A2-1-BK13)	B40 10.8 NS	(D2-3-AP08)	XMA 4.0-00 (D2-D12-02.03)	T=+12.8
[-SYSCLK(117)]	(A2-1-BL12)	D30 8.4 NS	(D2-2-BK08)	ADD 4.1-00 (D2-H07/A-02)	T=0
[-SYSCLK(121)]	(A2-1-BN13)	D30 8.4 NS	(D2-2-BJ13)	ADD 4.1-01 (D2-H08/B-02)	T=0
[-ØFFCLK(37)]	(A2-1-BN12)	D28 8.0 NS	(D2-3-BB20)	XMA 4.1-03 (D2-F15-02.03)	T=+10.0
[-SYSCLK(118)]	(A2-1-BK12)	D30 8.4 NS	(D2-1-BL16)	ADD 4.0-01 (D2-H04/A-03)	T=0
[-SYSCLK(122)]	(A2-1-BJ13)	D30 8.4 NS	(D2-3-AK20)	XMA 4.0-00 (D2-C15,D15-03)	T=0
[-ØFFCLK(38)]	(A2-1-BK14)	D28 8.0 NS	(D2-3-BB16)	XMA 4.1-03 (D2-F14-02.03)	T=+10.0
[-SYSCLK(119)]	(A2-1-BJ12)	D26 7.4 NS	(D2-2-BF01)	ADD 4.1-02 (D2-G05/B-03)	T=-1.0
[-SYSCLK(123)]	(A2-1-BL13)	D29 8.2 NS	(D2-3-AK16)	XMA 4.0-00 (D2-C14,D14-03)	T=0
[-ØFFCLK(39)]	(A2-1-BL14)	D28 8.0 NS	(D2-3-BF12)	XMA 4.1-03 (D2-G13-02.03)	T=+10.0

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

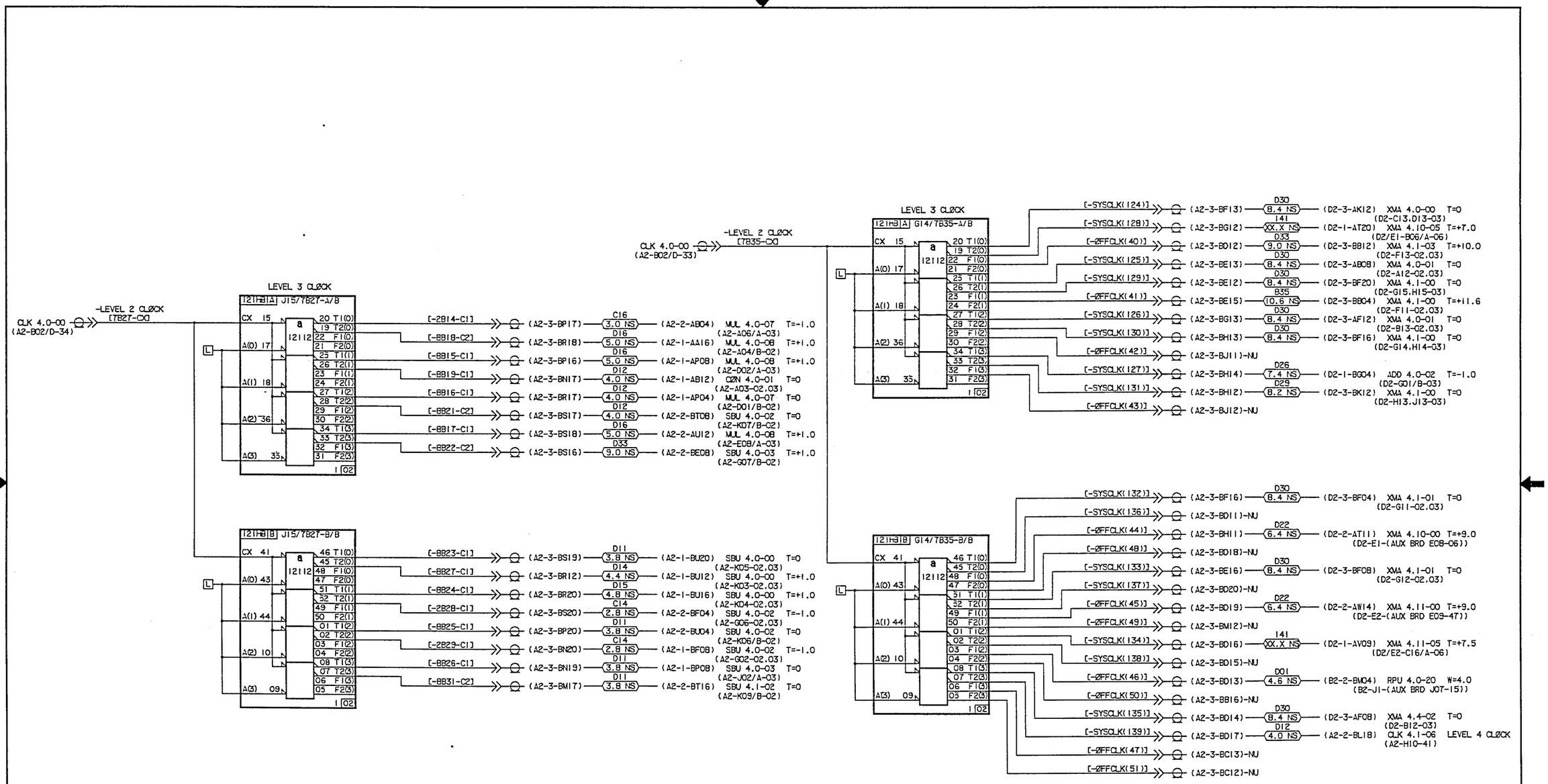
LEVEL 4 DIAGRAM
CLØCK PYRAMID (INTEGER UNIT)
LEVEL 3 TØ WØRKING RANKS

DB-A2MUL:A2

CAGE IDENT	DWG NO	REV
	60461830	A
SHEET	SIZE	
CLK 4.1-02	II-1-15	



CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM CLØCK PYRAMID(INTEGER UNIT) LEVEL 3 TØ WØRKING RANKS	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-A2MUL,A2	SHEET CLK 4.1-03	PAGE II-1-17



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
CLØCK PYRAMID(INTEGER UNIT)
LEVEL 3 TØ WØRKING RANKS

DB-A2MUL:A2

CODE IDENT	DWG NO	REV
	60461830	A
SHEET		PAGE
CLK 4.1-04		II-1-19

LEVEL 3 CLØCKS

121HB|A| C017B15-A/B

CLK 4.0-00 (A2-B02/D-32)

+LEVEL 2 CLØCK [7813-CX]

CX 15

A(0) 17

A(1) 18

A(2) 36

A(3) 35

20 T1(0)
19 T2(0)
22 F1(0)
21 F2(0)
25 T1(1)
26 T2(1)
23 F1(1)
24 F2(1)
27 T1(2)
28 T2(2)
29 F1(2)
30 F2(2)
34 T1(3)
33 T2(3)
32 F1(3)
31 F2(3)
1 02

[-SYSCLK(24)]	(A2-1-AL01)	D24 7.0 NS	(B2-3-AL04)	DMU 4.0-01	T=0	(B2-C11/B-02)
[-SYSCLK(28)]	(A2-1-AM05)	D24 7.0 NS	(B2-1-AK12)	DMU 4.0-01	T=0	(B2-C02/A.C03/A-03)
[-SYSCLK(25)]	(A2-1-AM01)	D24 7.0 NS	(B2-1-AK20)	DMU 4.0-00	T=0	(B2-C05-02.03)
[-SYSCLK(29)]	(A2-1-AN05)	D23 6.8 NS	(B2-1-AJ12)	DMU 4.0-01	T=0	(B2-C02/B.C03/B-02)
[-SYSCLK(26)]	(A2-1-AM03)	D24 7.0 NS	(B2-1-AK16)	DMU 4.0-00	T=0	(B2-C04/A-03)
[-SYSCLK(30)]	(A2-1-AN03)	D20 6.0 NS	(B2-2-BA15)	DMU 4.11-00	T=+1.7	(B2-E2(AUX BRD-E09-52))
[-SYSCLK(27)]	(A2-1-AM02)	D24 7.0 NS	(B2-1-AL04)	DMU 4.0-01	T=0	(B2-C01/B-02)
[-SYSCLK(31)]	(A2-1-AN04)	D18 5.4 NS	(B2-2-BA07)	DMU 4.11-00	T=0	(B2/E2-E09/B-23)

LEVEL 3 CLØCKS

121HB|A| J017B21-A/B

CLK 4.0-00 (A2-B02/D-31)

+LEVEL 2 CLØCK [7821-CX]

CX 15

A(0) 17

A(1) 18

A(2) 36

A(3) 35

20 T1(0)
19 T2(0)
22 F1(0)
21 F2(0)
25 T1(1)
26 T2(1)
23 F1(1)
24 F2(1)
27 T1(2)
28 T2(2)
29 F1(2)
30 F2(2)
34 T1(3)
33 T2(3)
32 F1(3)
31 F2(3)
1 02

[-SYSCLK(72)]	(A2-1-BR04)	D21 6.2 NS	(C2-2-AM07)	C2N 4.4-00	T=0	(C2-D07-02)
[-SYSCLK(76)]	(A2-1-BS04)	D21 6.2 NS	(C2-3-AB20)	C2N 4.4-00	T=0	(C2-A15-02.03)
[-SYSCLK(73)]	(A2-1-BR02)	D21 6.2 NS	(C2-2-AM11)	C2N 4.4-00	T=0	(C2-D08-02)
[-SYSCLK(77)]	(A2-1-BN09)	D20 6.0 NS	(C2-1-AB16)	C2N 4.0-00	T=0	(C2-A04,A05-03)
[-SYSCLK(74)]	(A2-1-BR01)	D21 6.2 NS	(C2-2-AM15)	C2N 4.4-00	T=0	(C2-D09-02)
[-SYSCLK(78)]	(A2-1-BS02)	B50 11.2 NS	(C2-3-AC12)	C2N 4.0-00	T=+5.2	(C2-A13,A14-03)
[-SYSCLK(75)]	(A2-1-BS01)	D21 6.2 NS	(C2-2-AT16)	C2N 4.4-00	T=0	(C2-E09-02)
[-SYSCLK(79)]	(A2-1-BS03)	D20 6.0 NS	(C2-1-AB08)	C2N 4.0-00	T=0	(C2-A01,A02-03)

121HB|B| C017B15-B/B

CX 41

A(0) 43

A(1) 44

A(2) 10

A(3) 09

46 T1(0)
45 T2(0)
47 F2(0)
48 F1(0)
51 T1(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)
1 02

[-ØFFCLK(8)]	(A2-1-AL05)	C14 2.8 NS	(B2-2-BJ05)	RPU 4.1-01	T=+6.6	(B2-H06-02)
[-SYSCLK(32)]	(A2-1-AP06)	D24 7.0 NS	(B2-2-AP16)	DMU 4.1-00	T=0	(B2-D09-02,03)
[-SYSCLK(36)]	(A2-1-AP02)	D24 7.0 NS	(B2-2-AK04)	DMU 4.1-00	T=0	(B2-C06/A-03)
[-ØFFCLK(9)]	(A2-1-AL06)	C14 2.8 NS	(B2-2-BJ08)	RPU 4.1-01	T=+6.6	(B2-H07-02)
[-SYSCLK(33)]	(A2-1-AR04)	D24 7.0 NS	(B2-3-AP08)	DMU 4.1-01	T=0	(B2-D12/B-02)
[-SYSCLK(37)]	(A2-1-AP05)	D24 7.0 NS	(B2-1-AP04)	DMU 4.1-01	T=0	(B2-D01/B-02)
[-ØFFCLK(10)]	(A2-1-AM07)	D30 8.4 NS	(B2-2-BJ09)	RPU 4.1-00	T=+12.0	(B2-K07-03)
[-SYSCLK(34)]	(A2-1-AN07)	D24 7.0 NS	(B2-3-AR04)	DMU 4.1-01	T=0	(B2-D11/B-02)
[-SYSCLK(38)]	(A2-1-AM08)	D23 6.8 NS	(B2-1-AN12)	DMU 4.1-01	T=0	(B2-D02/A.D03/A-03)
[-ØFFCLK(11)]	(A2-1-AM06)	D05 7.6 NS	(B2-3-AH13)	DMU 4.0-00	T=+11.5	(B2-C13-02)
[-SYSCLK(35)]	(A2-1-AN08)	D24 7.0 NS	(B2-2-AP08)	DMU 4.1-00	T=0	(B2-D07-02,03)
[-SYSCLK(39)]	(A2-1-AL09)	D23 6.8 NS	(B2-1-AM12)	DMU 4.1-01	T=0	(B2-D02/B.D03/B-02)

121HB|B| J017B21-B/B

CX 41

A(0) 43

A(1) 44

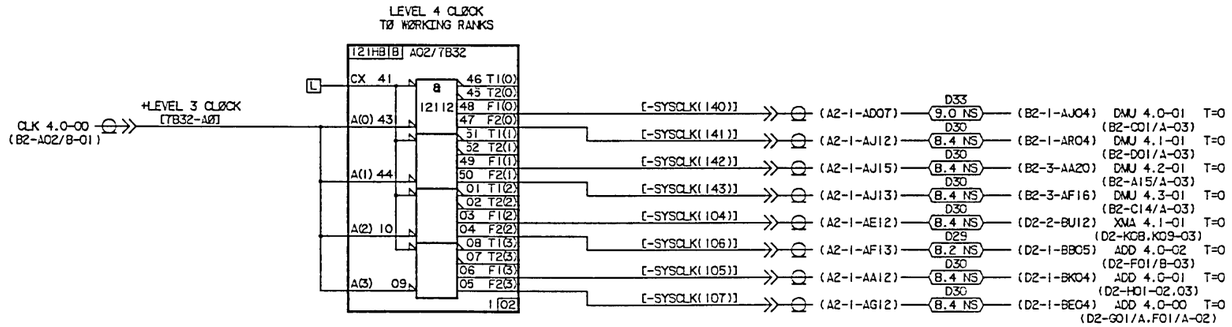
A(2) 10

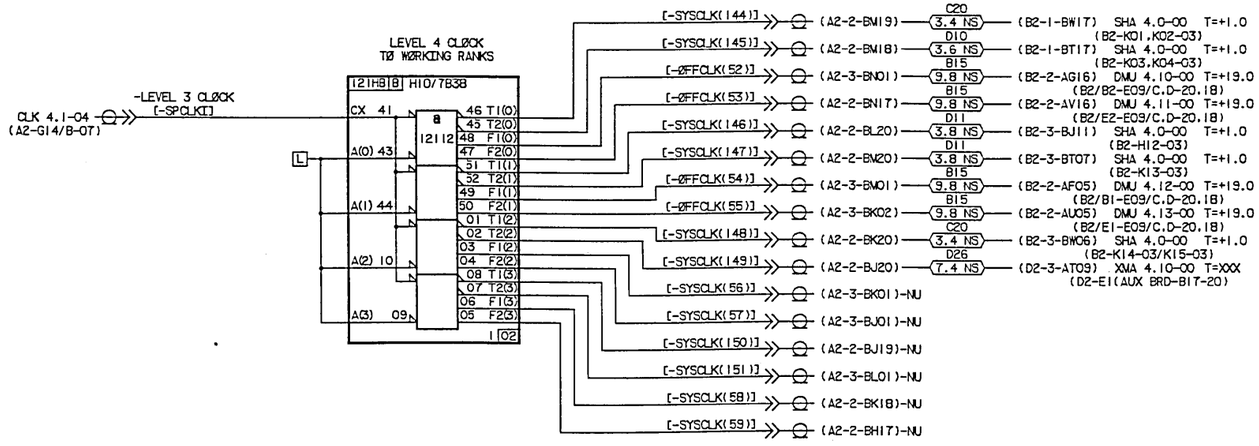
A(3) 09

46 T1(0)
45 T2(0)
48 F1(0)
47 F2(0)
51 T1(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)
1 02

[-ØFFCLK(20)]	(A2-1-BT01)	D25 7.2 NS	(B2-2-AH05)	DMU 4.10-00	W=2.8	(B2/B2-E09/B-24)
[-SYSCLK(80)]	(A2-1-BT03)	D22 6.4 NS	(C2-2-AR08)	C2N 4.4-00	T=0	(C2-D07-03)
[-SYSCLK(84)]	(A2-1-BU04)	D13 4.2 NS	(C2-2-AG20)	C2N 4.5-01	T=-1.0	(C2-B1-(AUX BRD-B11-21))
[-ØFFCLK(21)]	(A2-1-BT04)	D05 7.6 NS	(B2-2-AM05)	DMU 4.11-00	W=2.8	(B2/E2-E09/B-24)
[-SYSCLK(81)]	(A2-1-BV04)	D21 6.2 NS	(C2-2-AR12)	C2N 4.4-00	T=0	(C2-D08-03)
[-SYSCLK(85)]	(A2-1-BU01)	D21 6.2 NS	(C2-2-AU08)	C2N 4.4-00	T=0	(C2-E07-02,03)
[-ØFFCLK(22)]	(A2-1-BL08)	D25 7.2 NS	(B2-2-AE16)	DMU 4.12-00	W=2.8	(B2/B2-E09/B-24)
[-SYSCLK(82)]	(A2-1-BS09)	D21 6.2 NS	(C2-2-AR16)	C2N 4.4-00	T=0	(C2-D09-03)
[-SYSCLK(86)]	(A2-1-BN08)	D24 7.0 NS	(C2-2-AV12)	C2N 4.4-00	T=0	(C2-E08-02,03)
[-ØFFCLK(23)]	(A2-1-BR09)	D24 7.0 NS	(B2-2-AT16)	DMU 4.13-00	W=2.8	(B2/B2-E09/B-24)
[-SYSCLK(83)]	(A2-1-BK08)	D21 6.2 NS	(C2-2-AV16)	C2N 4.4-00	T=0	(C2-E09-03)
[-SYSCLK(87)]	(A2-1-BP10)	D27 7.8 NS	(B2-2-BD10)	RPU 4.2-00	T=+2.5	(B2-F2-(AUX BRD-F08-44))

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM CLØCK PYRAMID(INTEGER UNIT) LEVEL 3 TØ WØRKING RANKS	SIZE	DWG NO 60461830 REV A
DEVELOPMENT DIVISION	DB-A2MUL-A2	SHEET CLK 4.1-05	PAGE II-1-21





CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM CLØCK PYRAMID(INTEGER UNIT) LEVEL 4 TØ WØRKING RANKS	CAGE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-A2MUL:A2	SHEET CLK 4.1-06	SIZE II-1-23

LSI D3

LEVEL 3 CLØCK
121H8 A E15/7B30-A/B
-LEVEL 2 CLØCK [-CLØCK(212)]
CLK 4.0-00 (B2-A02/A-51)
CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35
8 12112
20 T1(0)
19 T2(0)
22 F1(0)
21 F2(0)
25 T1(1)
26 T2(1)
23 F1(1)
24 F2(1)
27 T1(2)
28 T2(2)
29 F1(2)
30 F2(2)
34 T1(3)
33 T2(3)
32 F1(3)
31 F2(3)
1 02

[-CLKT1(0)]	(D3-3-AU17)	B20 10.0 NS	(D3-1-BU08)	FPA 4.0-06 (D3-K02.K03-03)	T=+1.0		
[-CLKT0(5)]	(D3-3-AU18)	D28 8.0 NS	(D3-2-AB16)	FPA 4.0-10 (D3-A09-02.03)	T=0		
[+CLØCK(305)]	(D3-3-AV16)	D28 8.0 NS	(D3-3-BF18)	CLK 4.3-00 (D3-G15-17)	LEVEL 4 CLØCK		
[+CLØCK(306)]	(D3-3-AT19)	D12 4.0 NS	(D3-3-BH18)	CLK 4.3-00 (D3-G15-36)	LEVEL 4 CLØCK		
[-CLKT18(0)]	(D3-3-AU16)	D24 7.0 NS	(D3-2-AF12)	FPA 4.0-00 (D3-B08-03)	T=+18.0		
[-CLKT18(1)]	(D3-3-AT17)	D24 7.0 NS	(D3-3-AP04)	FPA 4.0-07 (D3-D11-03)	T=+18.0		
[+CLØCK(309)]	(D3-3-AT16)	D20 6.0 NS	(D3-3-AW19)	CLK 4.3-00 (D3-E15-41)	LEVEL 4 CLØCK		
[+CLØCK(310)]	(D3-3-AS16)	D20 6.0 NS	(D3-3-BG18)	CLK 4.3-00 (D3-G15-43)	LEVEL 4 CLØCK		
[-CLKT0(22)]	(D3-3-AV17)	D33 9.0 NS	(D3-2-AF08)	FPA 4.0-00 (D3-B07-03)	T=0		
[-CLKT0(23)]	(D3-3-AW17)	D33 9.0 NS	(D3-2-AP04)	FPA 4.0-06 (D3-D06-03)	T=0		
[+CLØCK(313)]	(D3-3-AW16)	D20 6.0 NS	(D3-3-BE19)	CLK 4.3-00 (D3-G15-10)	LEVEL 4 CLØCK		
[+CLØCK(314)]	(D3-3-BA15)	D16 5.0 NS	(D3-3-BK18)	CLK 4.3-00 (D3-H15-17)	LEVEL 4 CLØCK		
[-CLKT19(6)]	(D3-3-AW18)	D28 8.0 NS	(D3-3-BU16)	FPA 4.0-06 (D3-K14.K15-03)	T=+19.0		
[+CLØCK(316)]	(D3-3-AV18)	D16 5.0 NS	(D3-2-BC06)	CLK 4.3-00 (D3-F07-41)	LEVEL 4 CLØCK		
[+CLØCK(317)]	(D3-3-BA16)	D20 6.0 NS	(D3-3-BJ17)	CLK 4.3-00 (D3-H15-18)	LEVEL 4 CLØCK		
[+CLØCK(318)]	(D3-3-BA20)-NU						

LSI A3

LEVEL 3 CLØCK
121H8 B8 K15/7B30-B/B
-LEVEL 2 CLØCK [-CLØCK(213)]
CLK 4.0-00 (B2-A02/A-52)
CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09
8 12112
46 T1(0)
45 T2(0)
48 F1(0)
47 F2(0)
51 T1(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)
1 02

[-CLKT0(16)]	(A3-3-BW20)	D33 9.0 NS	(A3-1-BB20)	FPD 4.1-01 (A3-F05-03)	T=0		
[-CLKT0(17)]	(A3-3-BT17)	D33 9.0 NS	(A3-2-AF16)	FPD 4.1-01 (A3-B09.C09-03)	T=0		
[+CLØCK(321)]	(A3-3-BW19)	D28 8.0 NS	(A3-3-BV10)	CLK 4.3-01 (A3-K13-43)	LEVEL 4 CLØCK		
[+CLØCK(322)]	(A3-3-BW18)	D20 6.0 NS	(A3-3-BT11)	CLK 4.3-01 (A3-K13-10)	LEVEL 4 CLØCK		
[-CLKT0(18)]	(A3-3-BS20)	D33 9.0 NS	(A3-2-AF20)	FPD 4.1-01 (A3-B10-02.03)	T=0		
[-CLKT19(0)]	(A3-3-BW17)	D28 8.0 NS	(A3-1-BP08)	FPD 4.2-01 (A3-J02-03)	T=+19.0		
[+CLØCK(325)]	(A3-3-BV20)	D28 8.0 NS	(A3-3-BU18)	CLK 4.3-01 (A3-K15-15)	LEVEL 4 CLØCK		
[+CLØCK(326)]	(A3-3-BS16)-NU						
[-CLØCK(327)]	(A3-3-BP16)-NU						
[-CLKT0(21)]	(A3-3-BS19)	D33 9.0 NS	(A3-1-BU08)	FPD 4.2-01 (A3-K02-03)	T=0		
[+CLØCK(329)]	(A3-3-BU20)	D20 6.0 NS	(A3-3-BU10)	CLK 4.3-01 (A3-K13-15)	LEVEL 4 CLØCK		
[+CLØCK(330)]	(A3-3-BT20)	D12 4.0 NS	(A3-3-BV06)	CLK 4.3-01 (A3-K12-41)	LEVEL 4 CLØCK		
[-CLØCK(331)]	(A3-3-BS18)	D24 6.5 NS	(A3-2-BN01)				
[-CLØCK(332)]	(A3-3-BS17)	C06 1.5 NS	(A3-1-BP20)				
[+CLØCK(333)]	(A3-3-BT19)	C06 1.5 NS	(A3-2-BP02)				
[+CLØCK(334)]	(A3-3-BV18)	D24 6.5 NS	(A3-2-BP01)				

DIVIDE DØUBLE CLØCK GENERATØR
121H8 A J06/7E40-A/B
CX 15
A(0) 20
B(0) 19
A(1) 22
B(1) 21
A(2) 33
B(2) 34
A(3) 35
B(3) 36
A(4) 18
B(4) 17
8 12102
25 T(0)
26 F(0)
24 T(1)
23 F(1)
32 T(2)
31 F(2)
29 T(3)
30 F(3)
28 T(4)
27 F(4)
0 02

[-SYSCLK(XXX)]	(A3-2-BR01)	C06 1.5 NS	(A3-2-BF10)	CLK 4.3-02 (A3-G08-15)	LEVEL 5 CLØCK DØUBLE FREQUENCY
[-SYSCLK(XXX)]	(A3-2-BS01)	C06 1.5 NS	(A3-2-BH11)	CLK 4.3-02 (A3-G08-41)	LEVEL 5 CLØCK DØUBLE FREQUENCY
[-SYSCLK(XXX)]	NU				

LSI B3

CLK 4.0-00 (B2-A02/B-03)
-LEVEL 3 CLØCK [-CLØCK(302)]

LEVEL 3 CLØCK
121H8 B8 K03/7B30-B/B
+LEVEL 2 CLØCK [-CLØCK(215)]
CLK 4.0-00 (B2-A02/B-04)
CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09
8 12112
46 T1(0)
45 T2(0)
48 F1(0)
47 F2(0)
51 T1(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)
1 02

[-CLØCK(335)]	(B3-1-BU13)	D28 8.0 NS	(B3-1-BF16)	FPM 4.0-00 (B3-H04.G04-03)	T=0		
[-CLØCK(336)]	(B3-1-BU12)	B45 11.0 NS	(B3-3-AK16)	FPM 4.0-05 (B3-C14.D14-03)	T=+3.0		
[+CLØCK(337)]	(B3-1-BW11)	C06 2.0 NS	(B3-1-BU10)	CLK 4.3-04 (B3-K03-15)	LEVEL 4 CLØCK		
[+CLØCK(338)]	(B3-1-BV12)	C16 3.0 NS	(B3-3-BU06)	CLK 4.3-04 (B3-K12-17)	LEVEL 4 CLØCK		
[-CLØCK(339)]	(B3-1-BV13)	D28 8.0 NS	(B3-3-BP04)	FPM 4.1-01 (B3-J11-04)	T=0		
[-CLØCK(340)]	NU						
[+CLØCK(341)]	(B3-1-BW12)	C16 3.0 NS	(B3-3-BW06)	CLK 4.3-04 (B3-K12-36)	LEVEL 4 CLØCK		
[+CLØCK(342)]	(B3-1-BW13)	C06 2.0 NS	(B3-3-BV02)	CLK 4.3-04 (B3-K11-43)	LEVEL 4 CLØCK		
[-CLØCK(343)]	(B3-1-BT12)-NU						
[-CLØCK(344)]	(B3-1-BT13)	B50 11.2 NS	(B3-3-BK04)	FPM 4.0-04 (B3-H11.H12-03)	T=+4.0		
[+CLØCK(345)]	(B3-1-BW14)-NU						
[+CLØCK(346)]	(B3-1-BS13)	C16 3.0 NS	(B3-3-BW07)	CLK 4.3-04 (B3-K12-41)	LEVEL 4 CLØCK		
[-CLØCK(347)]	(B3-1-BT11)	D12 4.0 NS	(B3-1-BF10)	CLK 4.3-04 (B3-G03-15)	LEVEL 4 CLØCK		
[-CLØCK(348)]	(B3-1-BU14)-NU						
[+CLØCK(349)]	NU						
[-CLKT16]	(B3-1-BS10)	D28 8.0 NS	(B3-1-BB04)	FPM 4.2-00 (B3-F01.F02-03)	T=+16.0		

LEVEL 4 CLØCK
121H8 A B01/7B50
CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35
8 12112
20 T1(0)
19 T2(0)
22 F1(0)
21 F2(0)
25 T1(1)
26 T2(1)
23 F1(1)
24 F2(1)
27 T1(2)
28 T2(2)
29 F1(2)
30 F2(2)
34 T1(3)
33 T2(3)
32 F1(3)
31 F2(3)
1 02

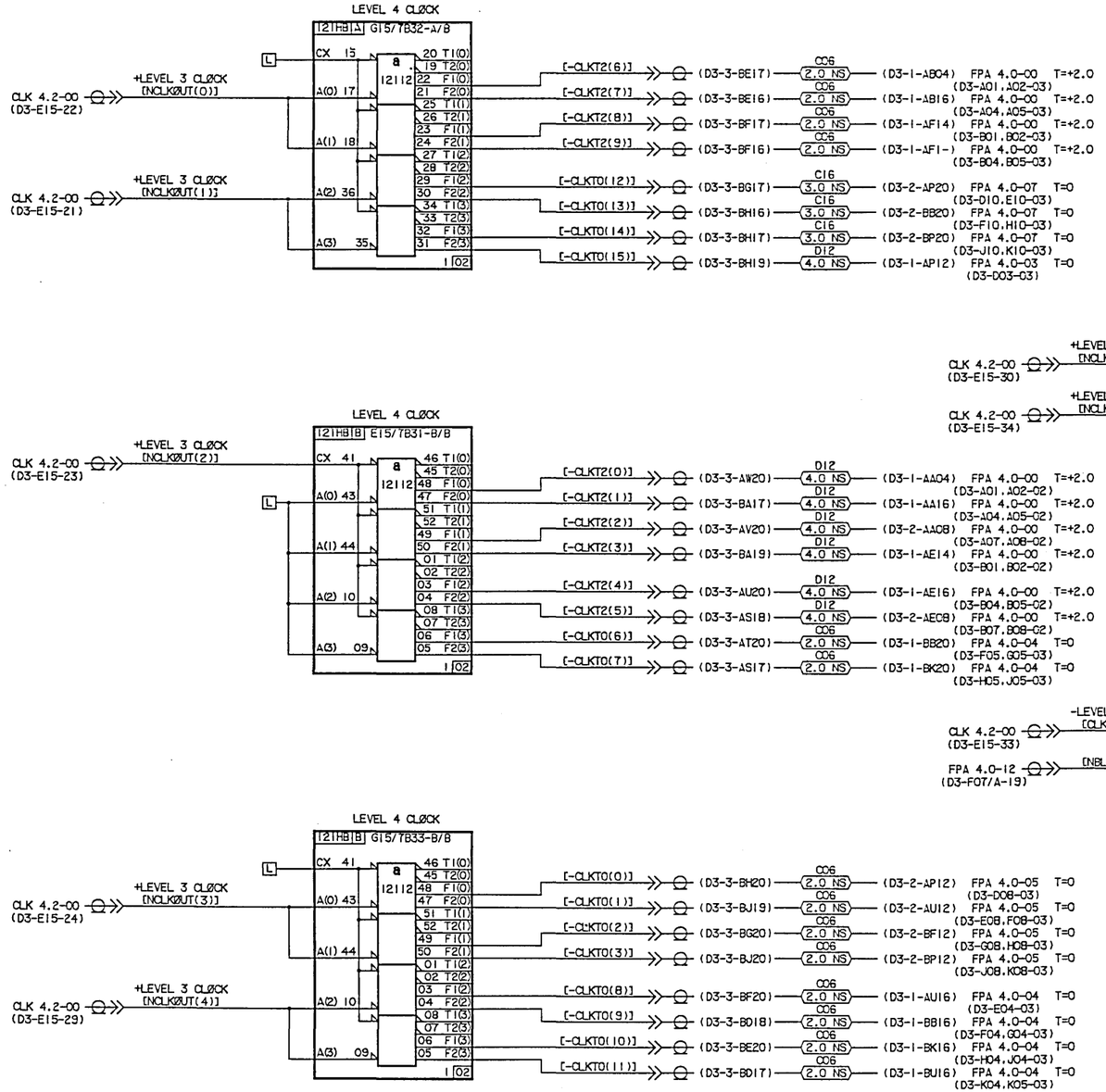
[-CLØCK(400)]	(C3-1-AC02)	C16 3.0 NS	(C3-1-AC02)	CLK 4.3-03 (C3-B01-41)	LEVEL 5 CLØCK		
[-CLØCK(401)]	(C3-1-AF02)	C16 3.0 NS	(C3-1-AK02)	CLK 4.3-03 (C3-C01-15)	LEVEL 5 CLØCK		
[+CLØCK(402)]	(C3-1-AD03)-NU						
[+CLØCK(403)]	(C3-1-AE03)-NU						
[-CLØCK(404)]	(C3-1-AF01)	C16 3.0 NS	(C3-1-AL02)	CLK 4.3-03 (C3-C01-41)	LEVEL 5 CLØCK		
[-CLKTO(X)]	(C3-1-AD02)	D30	(C3-1-AA04)	FPC 4.0-03 (C3-A01-02.03)	T=+18.0		
[+CLØCK(407)]	NU						
[+CLØCK(408)]	NU						
[-CLKT0Ø]	(C3-1-AE01)	D28 8.0 NS	(C3-3-AU04)	FPC 4.1-01 (C3-E1-E13-01)	T=0		
[-CLK5Ø]	(C3-1-AD01)	B45 11.0 NS	(C3-3-AT03)	FPC 4.1-01 (C3-E1-E13-02)	T=+5.0		
[+SYSCLK(XXX)]	NU						
[+SYSCLK(XXX)]	NU						
[-CLKT16(0)]	(C3-1-AH02)	D16 5.0 NS	(C3-3-AN20)	FPC 4.0-03 (C3-D15-02)	T=+16.0		
[-CLKT16(1)]	(C3-1-AG01)	D16 5.0 NS	(C3-3-AB20)	FPC 4.0-03 (C3-A15-02.03)	T=+16.0X		
[+SYSCLK(XXX)]	NU						
[+SYSCLK(XXX)]	NU						

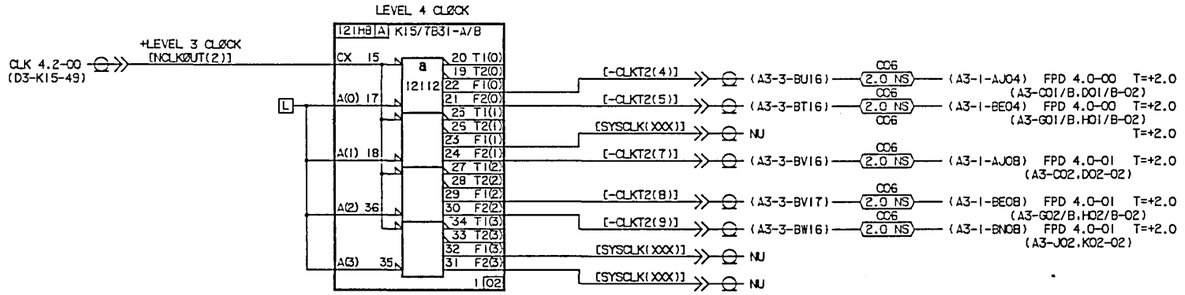
LSI C3

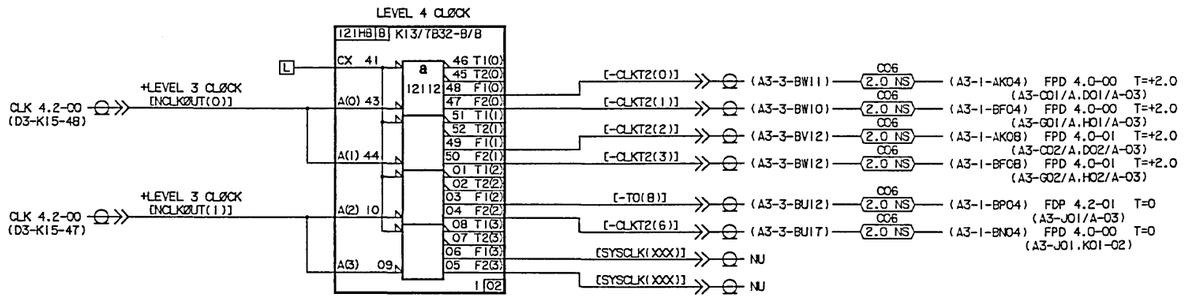
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

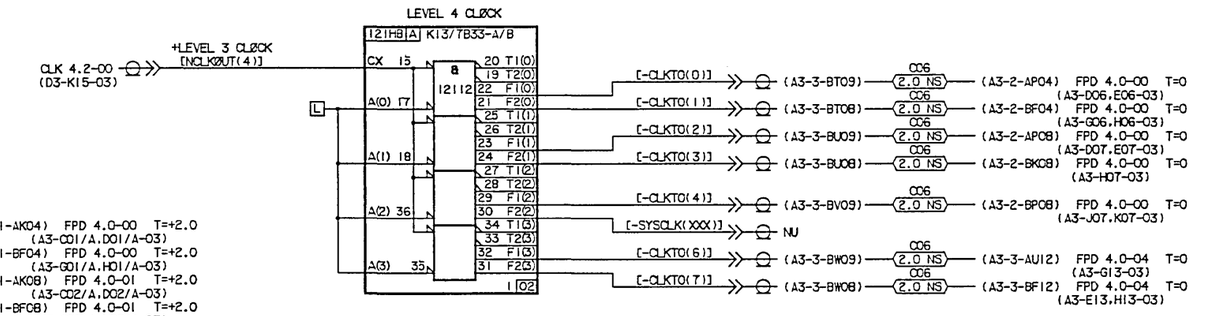
LEVEL 4 DIAGRAM
CLØCK PYRAMID(FLØATING PØINT UNIT)
LEVELS 3,4 & DIVIDE DØUBLE-CLØCK GENERATØR A3,B3,C3,D3

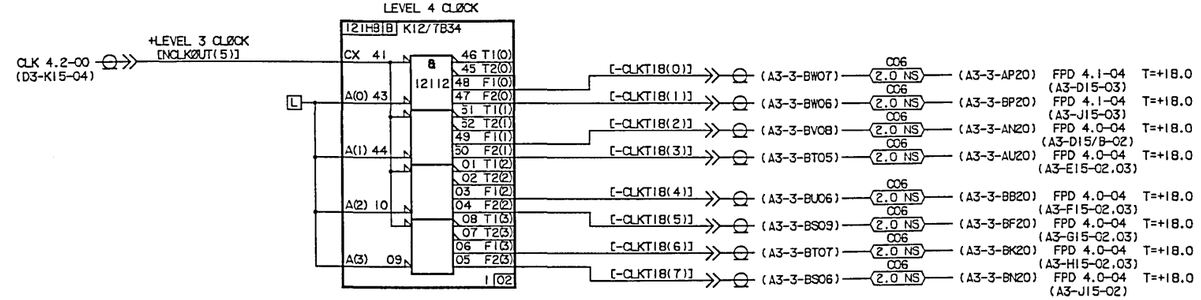
CODE IDENT | DRG NO: 60461830 | REV: A
SHEET: CLK 4.2-00 | SIZE: II-1-25


LEVEL 4 CLØCK
121HB|A| G15/7B32-A/B
CLK 4.2-00 (D3-E15-22)
+LEVEL 3 CLØCK [NCLKØUT(0)]
CLK 4.2-00 (D3-E15-21)
+LEVEL 3 CLØCK [NCLKØUT(1)]
[-CLKT2(6)] (D3-3-BE17) CØ6 2.0 NS (D3-1-AB04) FPA 4.0-00 T=+2.0 (D3-A01,A02-03)
[-CLKT2(7)] (D3-3-BE16) CØ6 2.0 NS (D3-1-AB16) FPA 4.0-00 T=+2.0 (D3-A04,A05-03)
[-CLKT2(8)] (D3-3-BF17) CØ6 2.0 NS (D3-1-AF14) FPA 4.0-00 T=+2.0 (D3-B01,B02-03)
[-CLKT2(9)] (D3-3-BF16) CØ6 2.0 NS (D3-1-AF1-) FPA 4.0-00 T=+2.0 (D3-B04,B05-03)
[-CLKT0(12)] (D3-3-BG17) C16 3.0 NS (D3-2-AP20) FPA 4.0-07 T=0 (D3-D10,E10-03)
[-CLKT0(13)] (D3-3-BH16) C16 3.0 NS (D3-2-BB20) FPA 4.0-07 T=0 (D3-F10,H10-03)
[-CLKT0(14)] (D3-3-BH17) C16 3.0 NS (D3-2-BP20) FPA 4.0-07 T=0 (D3-J10,K10-03)
[-CLKT0(15)] (D3-3-BH19) D12 4.0 NS (D3-1-AP12) FPA 4.0-03 T=0 (D3-D03-03)
LEVEL 4 CLØCK
121HB|A| H15/7B34-A/B
CLK 4.2-00 (D3-E15-30)
+LEVEL 3 CLØCK [NCLKØUT(5)]
CLK 4.2-00 (D3-E15-34)
+LEVEL 3 CLØCK [NCLKØUT(6)]
[-CLKT19(8)] (D3-3-BK16) CØ6 2.0 NS (D3-3-AU04) FPA 4.0-07 T=+19.0 (D3-E11,G11-03)
[-CLKT19(9)] (D3-3-BJ16) CØ6 2.0 NS (D3-3-BP04) FPA 4.0-07 T=+19.0 (D3-J11-03)
[-CLKT0(16)] (D3-3-BK17) CØ6 2.0 NS (D3-3-AA12) FPA 4.0-11 T=0 (D3-A13-02)
[-CLKT0(17)] (D3-3-BL16) CØ6 2.0 NS (D3-3-AB16) FPA 4.0-11 T=0 (D3-A14-02.03)
[-CLKT0(18)] (D3-3-BL17) CØ6 2.0 NS (D3-3-AB20) FPA 4.0-11 T=0 (D3-A15-02.03)
[-CLKT0(19)] (D3-3-BM16) CØ6 2.0 NS (D3-3-AP16) FPA 4.0-11 T=0 (D3-D14-02.03)
[-CLKT0(20)] (D3-3-BM17) CØ6 2.0 NS (D3-3-AP20) FPA 4.0-11 T=0 (D3-D15-02.03)
[-CLKT0(21)] (D3-3-BL18) CØ6 2.0 NS (D3-3-AE20) FPA 4.0-11 T=0 (D3-B15-02)
LEVEL 4 CLØCK
121HB|B| E15/7B31-B/B
CLK 4.2-00 (D3-E15-23)
+LEVEL 3 CLØCK [NCLKØUT(2)]
[-CLKT2(0)] (D3-3-AW20) D12 4.0 NS (D3-1-AA04) FPA 4.0-00 T=+2.0 (D3-A01,A02-02)
[-CLKT2(1)] (D3-3-BA17) D12 4.0 NS (D3-1-AA16) FPA 4.0-00 T=+2.0 (D3-A04,A05-02)
[-CLKT2(2)] (D3-3-AV20) D12 4.0 NS (D3-2-AA08) FPA 4.0-00 T=+2.0 (D3-A07,A08-02)
[-CLKT2(3)] (D3-3-BA19) D12 4.0 NS (D3-1-AE14) FPA 4.0-00 T=+2.0 (D3-B01,B02-02)
[-CLKT2(4)] (D3-3-AU20) D12 4.0 NS (D3-1-AE16) FPA 4.0-00 T=+2.0 (D3-B04,B05-02)
[-CLKT2(5)] (D3-3-AS18) D12 4.0 NS (D3-2-AE08) FPA 4.0-00 T=+2.0 (D3-B07,B08-02)
[-CLKT0(6)] (D3-3-AT20) CØ6 2.0 NS (D3-1-BB20) FPA 4.0-04 T=0 (D3-F05,G05-03)
[-CLKT0(7)] (D3-3-AS17) CØ6 2.0 NS (D3-1-BK20) FPA 4.0-04 T=0 (D3-H05,J05-03)
LEVEL 4 CLØCK
121HB|B| F07/7B35-B/B
CLK 4.2-00 (D3-E15-33)
+LEVEL 3 CLØCK [CLKØUT(7)]
FPA 4.0-12 (D3-F07/A-19)
[NBLØCK(1)]
[-CLKT19(0)] (D3-2-BD07) CØ6 2.0 NS (D3-2-AP16) FPA 4.0-04 T=+19.0 (D3-D09-03)
[-CLKT19(1)] (D3-2-BD06) CØ6 2.0 NS (D3-2-AU16) FPA 4.0-04 T=+19.0 (D3-E09,F09-03)
[-CLKT19(2)] (D3-2-BC08) CØ6 2.0 NS (D3-2-BF16) FPA 4.0-04 T=+19.0 (D3-G09,H09-03)
[-CLKT19(3)] (D3-2-BD08) CØ6 2.0 NS (D3-2-BP16) FPA 4.0-04 T=+19.0 (D3-J09,K09-03)
[-CLKT19(4)] (D3-2-BB08) CØ6 2.0 NS (D3-2-AF16) FPA 4.0-09 T=+19.0 (D3-B09,C09-03)
[SYSCLK(XXX)] NU
[-CLKT4(0)] (D3-2-BA07) D20 6.0 NS (D3-3-AB12) FPA 4.0-11 T=+4.0 (D3-A13-03)
[-CLKT4(1)] (D3-2-BC09) D20 6.0 NS (D3-3-AF20) FPA 4.0-11 T=+4.0 (D3-B15-03)
LEVEL 4 CLØCK
121HB|B| G15/7B33-B/B
CLK 4.2-00 (D3-E15-24)
+LEVEL 3 CLØCK [NCLKØUT(3)]
CLK 4.2-00 (D3-E15-29)
+LEVEL 3 CLØCK [NCLKØUT(4)]
[-CLKT0(0)] (D3-3-BH20) CØ6 2.0 NS (D3-2-AP12) FPA 4.0-05 T=0 (D3-D08-03)
[-CLKT0(1)] (D3-3-BJ19) CØ6 2.0 NS (D3-2-AU12) FPA 4.0-05 T=0 (D3-E08,F08-03)
[-CLKT0(2)] (D3-3-BG20) CØ6 2.0 NS (D3-2-BF12) FPA 4.0-05 T=0 (D3-G08,H08-03)
[-CLKT0(3)] (D3-3-BJ20) CØ6 2.0 NS (D3-2-BP12) FPA 4.0-05 T=0 (D3-J08,K08-03)
[-CLKT0(8)] (D3-3-BF20) CØ6 2.0 NS (D3-1-AU16) FPA 4.0-04 T=0 (D3-E04-03)
[-CLKT0(9)] (D3-3-BD18) CØ6 2.0 NS (D3-1-BB16) FPA 4.0-04 T=0 (D3-F04,G04-03)
[-CLKT0(10)] (D3-3-BE20) CØ6 2.0 NS (D3-1-BK16) FPA 4.0-04 T=0 (D3-H04,J04-03)
[-CLKT0(11)] (D3-3-BD17) CØ6 2.0 NS (D3-1-BU16) FPA 4.0-04 T=0 (D3-K04,K05-03)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
CLØCK PYRAMID(FPU-ADD)
LEVEL 4 CLØCKS TØ WØRKING RANKS
DB-D3FPA:D3
ORDER IDENT 60461830
REV A
SHEET CLK 4.3-00
PAGE II-1-27



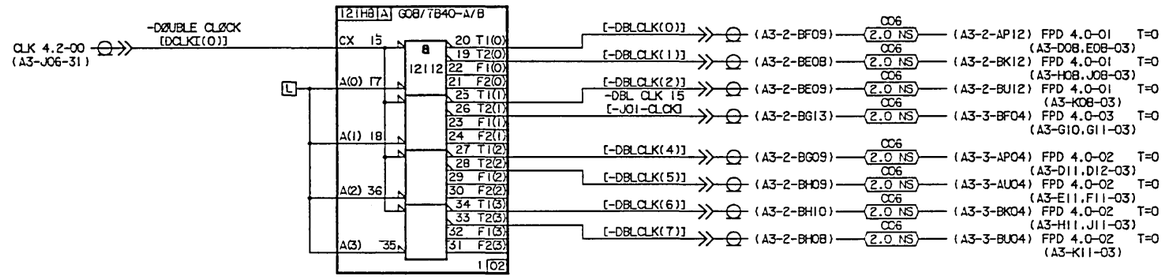




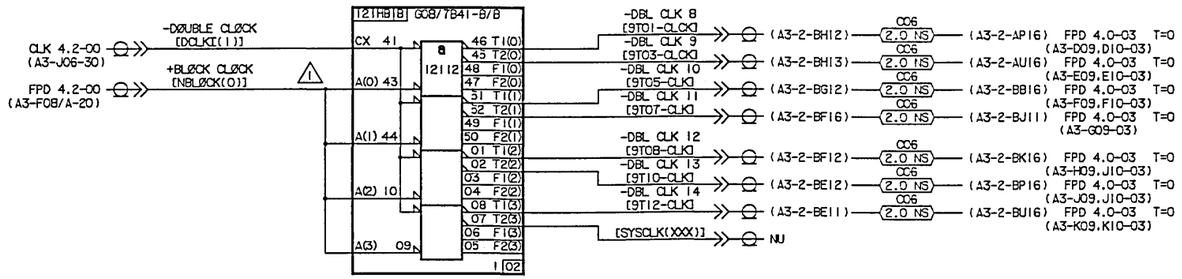


CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM CLØCK PYRAMID(FPU-DIVIDE) LEVEL 4 CLØCKS TØ WØRKING RANKS	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-A3FPD:A3	SHEET CLK 4.3-01	SIZE II-1-29

LEVEL 5
DIVIDE DØUBLE FREQUENCY
CLØCKS



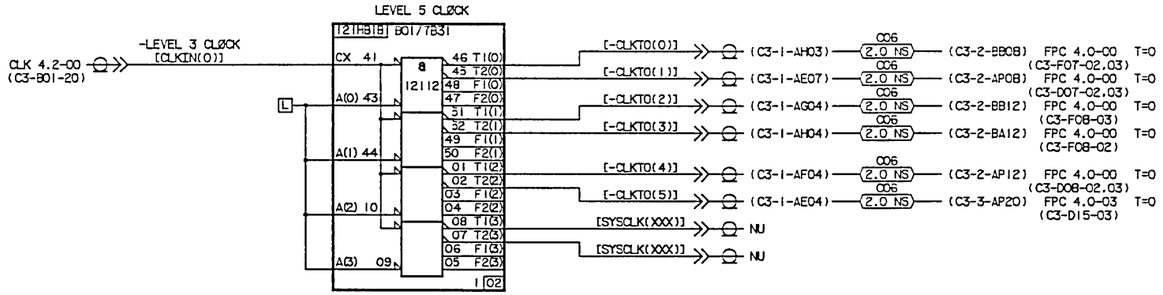
LEVEL 5
DIVIDE DØUBLE FREQUENCY
CLØCKS

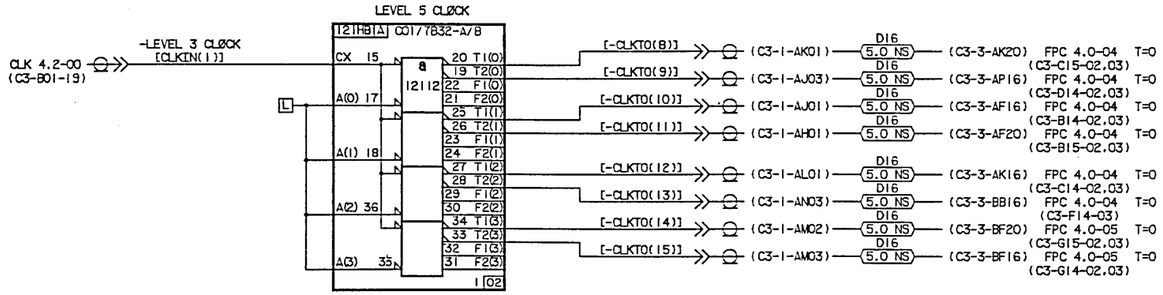


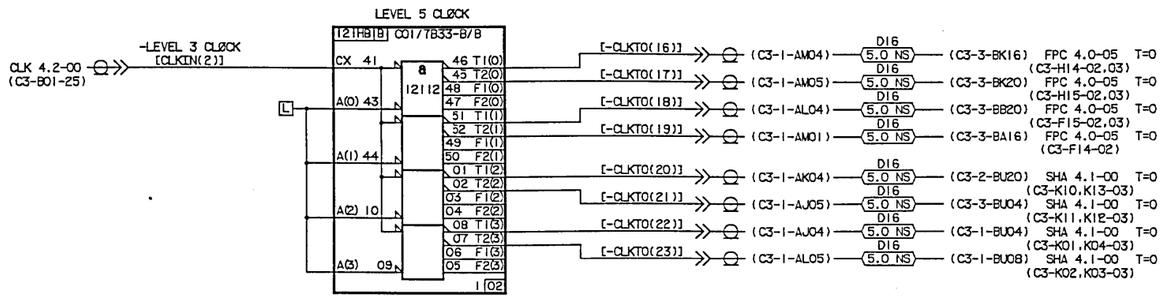
NØTE:

⚠1 DELAY AS REQUIRED.

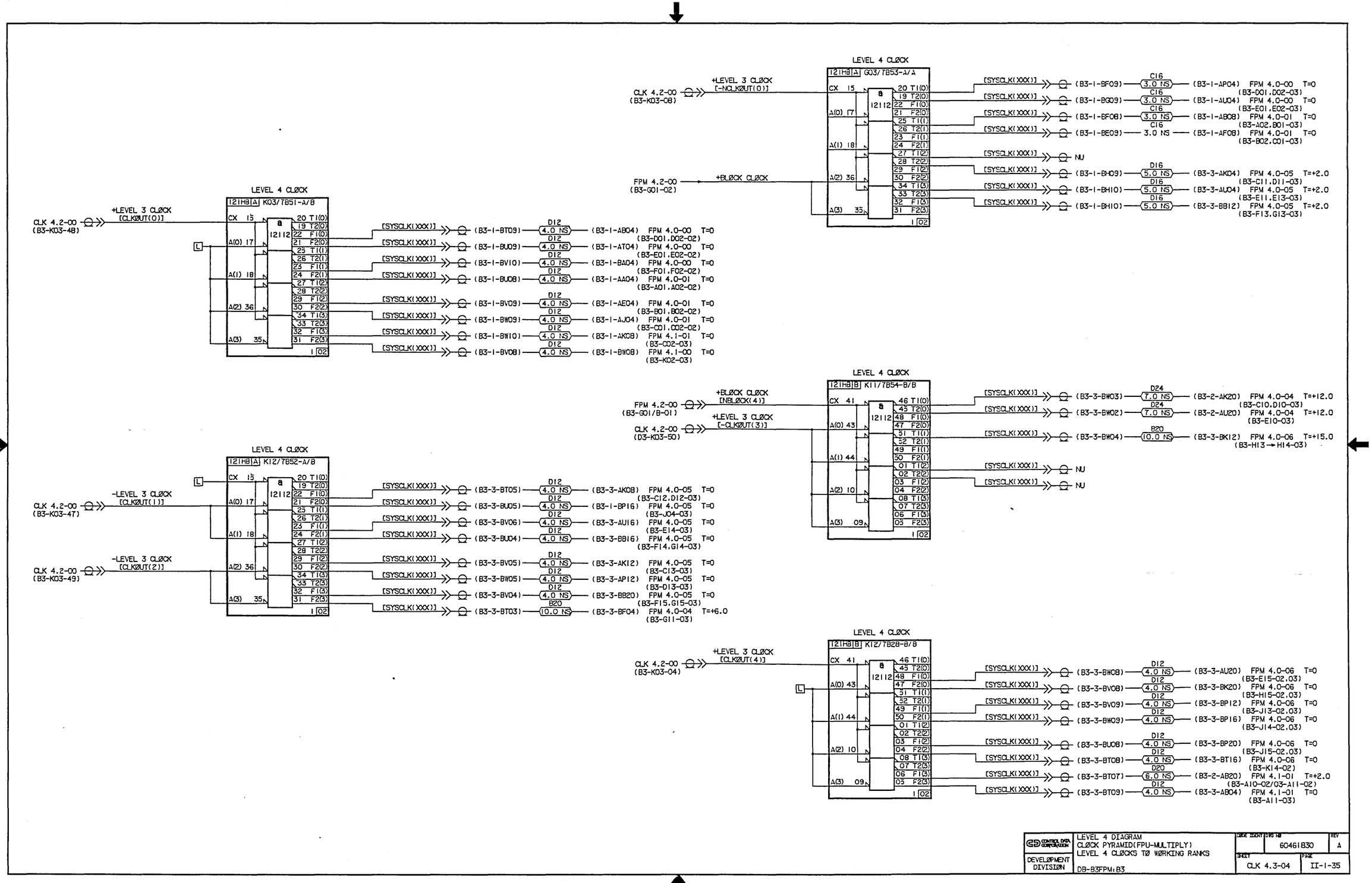
CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM CLØCK PYRAMID(FPU-DIVIDE) LEVEL 5 DØUBLE FREQUENCY CLØCKS	CODE IDENT / DWG NO	REV
		60461830	A
DEVELOPMENT DIVISION	DB-A3FPD:A3	SHEET: CLK 4.3-02	PAGE: II-1-31







CONTROL DATA CORPORATION	LEVEL 5 DIAGRAM CLØCK PYRAMID(FPU-CØNTRØL) LEVEL 4 CLØCKS TØ WØRKING RANKS	CAGE IDENT:	DWG NO: 60461830 REV: A
DEVELØPMENT DIVISIØN	DB-C3FPK1C3	SHEET: CLK 4.3-03	PAGE: II-1-33


LEVEL 4 CLØCK
121HB|A| K03/7B51-A/B
CLK 4.2-00 (B3-K03-48)
+LEVEL 3 CLØCK [CLKØUT(0)]
CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35
12112
20 T1(0)
19 T2(0)
22 F1(0)
21 F2(0)
25 T1(1)
26 T2(1)
23 F1(1)
24 F2(1)
27 T1(2)
28 T2(2)
29 F1(2)
30 F2(2)
34 T1(3)
33 T2(3)
32 F1(3)
31 F2(3)
[SYSCLK(XXX)] (B3-1-BT09) D12 4.0 NS (B3-1-AB04) FPM 4.0-00 T=0 (B3-D01,D02-02)
[SYSCLK(XXX)] (B3-1-BU09) D12 4.0 NS (B3-1-AT04) FPM 4.0-00 T=0 (B3-E01,E02-02)
[SYSCLK(XXX)] (B3-1-BV10) D12 4.0 NS (B3-1-BA04) FPM 4.0-00 T=0 (B3-F01,F02-02)
[SYSCLK(XXX)] (B3-1-BU08) D12 4.0 NS (B3-1-AA04) FPM 4.0-01 T=0 (B3-A01,A02-02)
[SYSCLK(XXX)] (B3-1-BV09) D12 4.0 NS (B3-1-AE04) FPM 4.0-01 T=0 (B3-B01,B02-02)
[SYSCLK(XXX)] (B3-1-BW09) D12 4.0 NS (B3-1-AJ04) FPM 4.0-01 T=0 (B3-C01,C02-02)
[SYSCLK(XXX)] (B3-1-BW10) D12 4.0 NS (B3-1-AK08) FPM 4.1-01 T=0 (B3-C02-03)
[SYSCLK(XXX)] (B3-1-BV08) D12 4.0 NS (B3-1-BW08) FPM 4.1-00 T=0 (B3-K02-03)
LEVEL 4 CLØCK
121HB|A| K12/7B52-A/B
CLK 4.2-00 (B3-K03-47)
+LEVEL 3 CLØCK [CLKØUT(1)]
CLK 4.2-00 (B3-K03-49)
+LEVEL 3 CLØCK [CLKØUT(2)]
[SYSCLK(XXX)] (B3-3-BT05) D12 4.0 NS (B3-3-AK08) FPM 4.0-05 T=0 (B3-C12,D12-03)
[SYSCLK(XXX)] (B3-3-BU05) D12 4.0 NS (B3-1-BP16) FPM 4.0-05 T=0 (B3-J04-03)
[SYSCLK(XXX)] (B3-3-BV06) D12 4.0 NS (B3-3-AU16) FPM 4.0-05 T=0 (B3-E14-03)
[SYSCLK(XXX)] (B3-3-BU04) D12 4.0 NS (B3-3-BB16) FPM 4.0-05 T=0 (B3-F14,G14-03)
[SYSCLK(XXX)] (B3-3-BV05) D12 4.0 NS (B3-3-AK12) FPM 4.0-05 T=0 (B3-C13-03)
[SYSCLK(XXX)] (B3-3-BW05) D12 4.0 NS (B3-3-AP12) FPM 4.0-05 T=0 (B3-D13-03)
[SYSCLK(XXX)] (B3-3-BV04) D12 4.0 NS (B3-3-BB20) FPM 4.0-05 T=0 (B3-F15,G15-03)
[SYSCLK(XXX)] (B3-3-BT03) B20 10.0 NS (B3-3-BF04) FPM 4.0-04 T=+6.0 (B3-G11-03)
LEVEL 4 CLØCK
121HB|A| G03/7B53-A/A
CLK 4.2-00 (B3-K03-08)
+LEVEL 3 CLØCK [-NCLKØUT(0)]
FPM 4.2-00 (B3-G01-02)
+BLØCK CLØCK
[SYSCLK(XXX)] (B3-1-BF09) C16 3.0 NS (B3-1-AP04) FPM 4.0-00 T=0 (B3-D01,D02-03)
[SYSCLK(XXX)] (B3-1-BG09) C16 3.0 NS (B3-1-AU04) FPM 4.0-00 T=0 (B3-E01,E02-03)
[SYSCLK(XXX)] (B3-1-BF08) C16 3.0 NS (B3-1-AB08) FPM 4.0-01 T=0 (B3-A02,B01-03)
[SYSCLK(XXX)] (B3-1-BE09) C16 3.0 NS (B3-1-AF08) FPM 4.0-01 T=0 (B3-B02,C01-03)
[SYSCLK(XXX)] NU
[SYSCLK(XXX)] (B3-1-BH09) D16 5.0 NS (B3-3-AK04) FPM 4.0-05 T=+2.0 (B3-C11,D11-03)
[SYSCLK(XXX)] (B3-1-BH10) D16 5.0 NS (B3-3-AU04) FPM 4.0-05 T=+2.0 (B3-E11,E13-03)
[SYSCLK(XXX)] (B3-1-BH10) D16 5.0 NS (B3-3-BB12) FPM 4.0-05 T=+2.0 (B3-F13,G13-03)
LEVEL 4 CLØCK
121HB|B| K11/7B54-B/B
FPM 4.2-00 (B3-G01/B-01)
+BLØCK CLØCK [NBLØCK(4)]
CLK 4.2-00 (D3-K03-50)
+LEVEL 3 CLØCK [-CLKØUT(3)]
CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09
46 T1(0)
45 T2(0)
48 F1(0)
47 F2(0)
51 T1(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)
[SYSCLK(XXX)] (B3-3-BW03) D24 7.0 NS (B3-2-AK20) FPM 4.0-04 T=+12.0 (B3-C10,D10-03)
[SYSCLK(XXX)] (B3-3-BW02) D24 7.0 NS (B3-2-AU20) FPM 4.0-04 T=+12.0 (B3-E10-03)
[SYSCLK(XXX)] (B3-3-BW04) B20 10.0 NS (B3-3-BK12) FPM 4.0-06 T=+15.0 (B3-H13→H14-03)
[SYSCLK(XXX)] NU
[SYSCLK(XXX)] NU
LEVEL 4 CLØCK
121HB|B| K12/7B28-B/B
CLK 4.2-00 (B3-K03-04)
+LEVEL 3 CLØCK [CLKØUT(4)]
[SYSCLK(XXX)] (B3-3-BW08) D12 4.0 NS (B3-3-AU20) FPM 4.0-06 T=0 (B3-E15-02,03)
[SYSCLK(XXX)] (B3-3-BV08) D12 4.0 NS (B3-3-BK20) FPM 4.0-06 T=0 (B3-H15-02,03)
[SYSCLK(XXX)] (B3-3-BV09) D12 4.0 NS (B3-3-BP12) FPM 4.0-06 T=0 (B3-J13-02,03)
[SYSCLK(XXX)] (B3-3-BW09) D12 4.0 NS (B3-3-BP16) FPM 4.0-06 T=0 (B3-J14-02,03)
[SYSCLK(XXX)] (B3-3-BU08) D12 4.0 NS (B3-3-BP20) FPM 4.0-06 T=0 (B3-J15-02,03)
[SYSCLK(XXX)] (B3-3-BT08) D12 4.0 NS (B3-3-BT16) FPM 4.0-06 T=0 (B3-K14-02)
[SYSCLK(XXX)] (B3-3-BT07) D20 6.0 NS (B3-2-AB20) FPM 4.1-01 T=+2.0 (B3-A10-02/03-A11-02)
[SYSCLK(XXX)] (B3-3-BT09) D12 4.0 NS (B3-3-AB04) FPM 4.1-01 T=0 (B3-A11-03)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
CLOCK PYRAMID(FPU-MULTIPLY)
LEVEL 4 CLOCKS TO WORKING RANKS
DB-B3FPM:B3
DWG NO 60461830
REV A
SHEET CLK 4.3-04
PAGE II-1-35

III. CYBER CHANNEL RING PORT

1. CYBER CHANNEL RING PORT (CRP)

SYSTEM FUNCTION

The CYBER channel ring port (CRP) is the CYBER host computer's interface with the CYBERPLUS. The CYBER host's peripheral processor unit (PPU) 12-bit channel (170/800) connects to the CRP. Through the CRP, the CYBER host can control from 1 to 16 CYBERPLUS base processors.

GENERAL DESCRIPTION

The CRP links the CYBER host to the system ring of the CYBERPLUS. At one interface, the CRP provides the necessary handshaking responses with the CYBER host's PPU to establish the connection of the channel and to coordinate data transmissions with the PPU channel. At the other interface, the CRP receives data from units on the system ring, monitors any stopped/halted transmissions on the system ring, places data from other units back onto the system ring if it's not for the CRP, and initiates those transmissions of data originated by the CYBER host and destined for other units on the system ring.

LOCATION

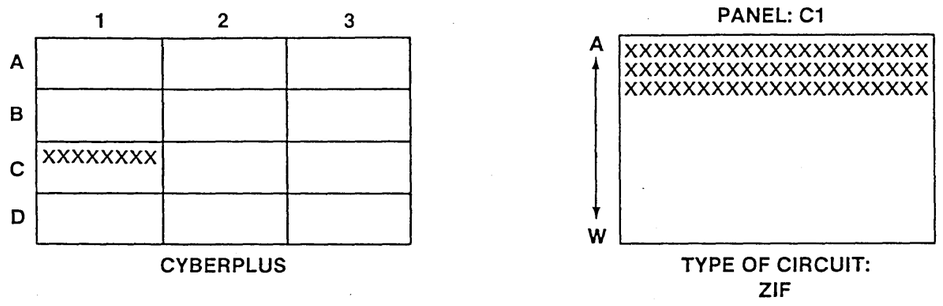


Figure III-1-1. Location of CYBER Channel Ring Port Logic Circuits

FUNCTIONAL DESCRIPTION

The CRP (shown in simplified block diagram form in figure III-1-2 and on the level 2 diagram CRP 2.0) interfaces to a dedicated channel of the CYBER 170/800 PPU. When the CYBER PP channel initiates communications with the CYBERPLUS, it sends a 12-bit function word that is entered into the function register. There it is translated to determine the mode of data conversion, whether it is a read or write operation, its source or destination loop register, and whether it is to be the normal or diagnostic mode of operation.

The input and output registers include 12-bit to 16-bit converters on the input side, and 16-bit to 12-bit converters on the output side. Because of the interface bit-size conversion, data can be handled in three different modes: mode 0, where bits 0--3 (the four MSB) in the CRP are zero filled and the remaining bits contain the 12-bit CYBER word; mode 1, where the bits are strung together to form three 16-bit words from four 12-bit CYBER words in the input side, or just the opposite conversion in the output side; mode 2, where a character transfer of two 12-bit CYBER words, each with bits 11--8 unused, form one 16-bit word in the input side, or one 16-bit word forms two 12-bit CYBER words when bits 11--8 are zero filled in the output side.

After bit conversion the I/O shift register receives 16-bit parallel data from the CYBER input side or sends out 16-bit parallel data to the CYBER output side . The I/O shift register also sends or receives single-bit data to or from the multiplexers that service the loop registers. Any parallel data coming from the CYBER input channel is shifted out serially from the I/O shift register to the 1 to 16 multiplexer transmitting to the loop registers. Any parallel data coming from the system ring and set into the loop registers may be serially shifted from the loop registers through the 16 to 1 multiplexer to the I/O shift register and converted back to parallel data for transmission to the CYBER host.

The multiplexers send serial data to or receive serial data from the loop register designated in the register code portion (bits 5--0) of the CYBER function word. When bit 5 is clear, it is a read operation; when it is set, it is a write operation. Some codes in each group are not used.

There are 19 loop registers addressable by the CRP. Fifteen of the loop registers (6 of which are grouped into serial pairs) are registers located within the CRP. Four of the loop registers, those connected to the DMAU and HPM, are registers located in the respective units and only connected by cables to the CRP. The loop registers are (or in the case of the DMAU and HPM, function as) 16-bit, parallel, left-shift registers within the CRP. They are each connected so they can function both as parallel and serial registers. Depending on their assigned purpose, they can receive parallel or serial data and transmit serial or parallel data. The loop registers receive and store information about the status of operations throughout the CYBERPLUS. Additionally, some of registers can be used to write information into the subsystem units. The serial inputs to the loop registers are connected to the 1 X 16 serial write multiplexer. The serial outputs from the loop registers are connected to the 16 X 1 serial read multiplexer.

The loop registers are used to initialize portions of the subsystem, provide diagnostic access to registers within the subsystem, record status of the CRP and the system ring, exert and record control over traffic on the system, and some are used in all data transfers between the CYBER and the base processors.

The 29-bit ring output register places ring packets on the system ring every clock cycle unless the ring has been stopped. The ring packets come from three different sources. The first is the ring input register which provides 28-bit packets that have arrived from the ring, are not addressed to the CRP, and have not yet been around the ring. The ring output register adds the 29th bit, the lost packet bit, and places the packet back on the ring. The second is the data that comes from the CYBER via the ring control and ring data loop registers. This data is assembled as a ring packet in the ring output register and placed on the ring. Ring packets coming from other sources on the ring have priority over the ring packets that originate from the CYBER. The third is the ring output register, itself, when there is no ring traffic and an empty (all zeros) packet is placed on the ring.

The 29-bit ring input register receives ring packets every clock cycle unless the ring has been stopped. Once in the ring input register, the packet is transmitted to one of four possible locations according to the translation of the lost packet bit, function code, and equipment select codes in its 12-bit control field. If the packet is a lost packet, it is immediately gated into the lost packet loop registers. Secondly, if the packet is not a lost packet and is not for the CRP, it is sent back out on the ring via the ring output register. Lastly, once the packet has been identified as for the CRP, it is directed either to the 1000-word by 28-bit control/data FIFO or to the 15-word by 16-bit request stack, according to the function specified by the function code. On those occasions when the function code is a not-used (illegal) function code, the packet is gated to the lost packet registers.

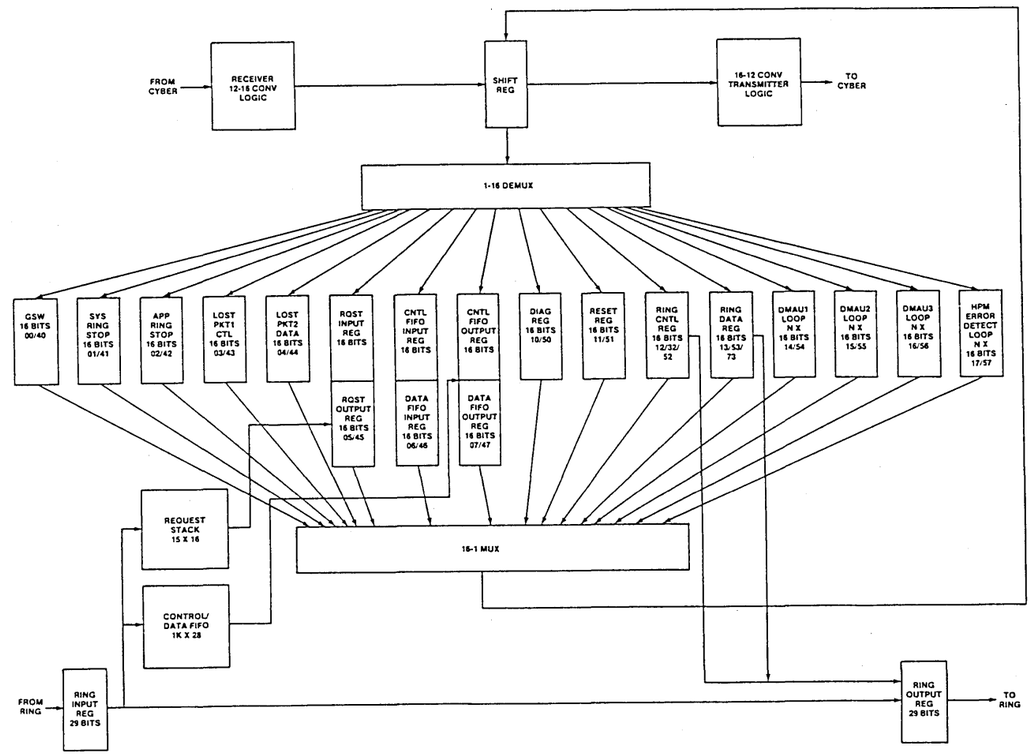

FROM CYBER
RECEIVER 12-16 CONV LOGIC
SHIFT REG
16-12 CONV TRANSMITTER LOGIC
TO CYBER
1-16 DEMUX
GSW 16 BITS 00/40
SYS RING STOP 16 BITS 01/41
APP RING STOP 16 BITS 02/42
LOST PKT1 CTL 16 BITS 03/43
LOST PKT2 DATA 16 BITS 04/44
ROST INPUT REG 16 BITS
CNTL FIFO INPUT REG 16 BITS
CNTL FIFO OUTPUT REG 16 BITS
DIAG REG 16 BITS 10/50
RESET REG 16 BITS 11/51
RING CNTL REG 16 BITS 12/32/52
RING DATA REG 16 BITS 13,53/73
DMAU1 LOOP N X 16 BITS 14/54
DMAU2 LOOP N X 16 BITS 15/55
DMAU3 LOOP N X 16 BITS 16/56
HPM ERROR DETECT LOOP N X 16 BITS 17/57
ROST OUTPUT REG 16 BITS 05/45
DATA FIFO INPUT REG 16 BITS 06/46
DATA FIFO OUTPUT REG 16 BITS 07/47
REQUEST STACK 15 X 16
16-1 MUX
CONTROL/ DATA FIFO 1K X 28
FROM RING
RING INPUT REG 29 BITS
RING OUTPUT REG 29 BITS
TO RING
01283

Figure III-1-2. CYBER Channel Ring Port Block Diagram

FRØM CYBER CHANNEL

FRØM CYBER CHANNEL

FUNCTIØN RGTR 4.2-03

CYBER FUNCTIØN DECØDER 4.2-01

SERIAL WRITE 1 X 16 DEMUX 4.1-01

12/16 CØNVERSIØN 4.2-01

INPUT HANDSHAKE 4 4.2-01 4.2-05

SERIAL READ 16 X 1 MUX 4.1-01

I/Ø SHIFT RGTR 4.1-04

16/12 CØNVERSIØN 4.2-02

ØUTPUT HANDSHAKE 4 4.2-05 4.2-02

TØ CYBER CHANNEL

TØ CYBER CHANNEL

BP

SYS RING STØP RGTR FC=01/41 4.1-02

CRP STATUS

BP

GSW FC=00/40 4.1-04

LØST PKT 1 RGTR CØNTR FC=03/43 4.0-08

BP

APP RING STØP RGTR FC=02/42 4.1-02

BP

REQ INPUT RGTR 4.0-01

REQUEST STACK 16 X 16 4.0-06

LØST PKT 2 DATA RGTR FC=04/44 4.0-08

CTL INPUT RGTR 4.0-02

DATA INPUT RGTR FC=06/46 4.0-02

REQ ØUTPUT RGTR FC=05/45 4.0-01

CØNTRØL/DATA FIFØ 1K X 28 4.0-02

CTL ØUTPUT FIFØ RGTR 4.0-02

DATA ØUTPUT FIFØ RGTR FC=07/47 4.0-02

DIAGNØSTIC RGTR FC=10/50 4.1-03

RESET RGTR FC=11/51 4.1-03

CRP FUNCTIØN CØNTRØL

BP

RING CTL RGTR FC=12/32/52 4.1-01

RING DATA RGTR FC=13/53/73 4.1-01

DMAU LØØP RGTR 1 FC=14/54 4.1-03 ⚠1

DMAU LØØP RGTR 2 FC=15/55 4.1-03 ⚠1

DMAU LØØP RGTR 3 FC=16/56 4.1-03 ⚠1

HPM ERRØR LØØP RGTR 4 FC=17/57 4.1-03 ⚠1

TØ SYSTEM RING

CRP EQUIP I.D. SW.

ADDRESS.FUNCTIØN AND LØST PACKET DECØDER CRP 4.0

FRØM SYSTEM RING

RING INPUT RGTR 4.0-01

RING ØUTPUT RGTR 4.0-01

NØTE:

THESE ARE CØNTRØL LINES. EACH CARRYING DESCRETE SIGNALS.

THE NUMBER ØF LINES,X, IS EGUAL TØ THE NUMBER ØF BP'S (BASE PRØCESSØRS) IN THE SUBSYSTEM.

⚠1 THESE REGISTERS EXIST ØNLY IN THE DESIGNATED FUNCTIØNAL UNITS. THEY ARE SHØWN HERE FØR CLARIFICATIØN ØF USE.

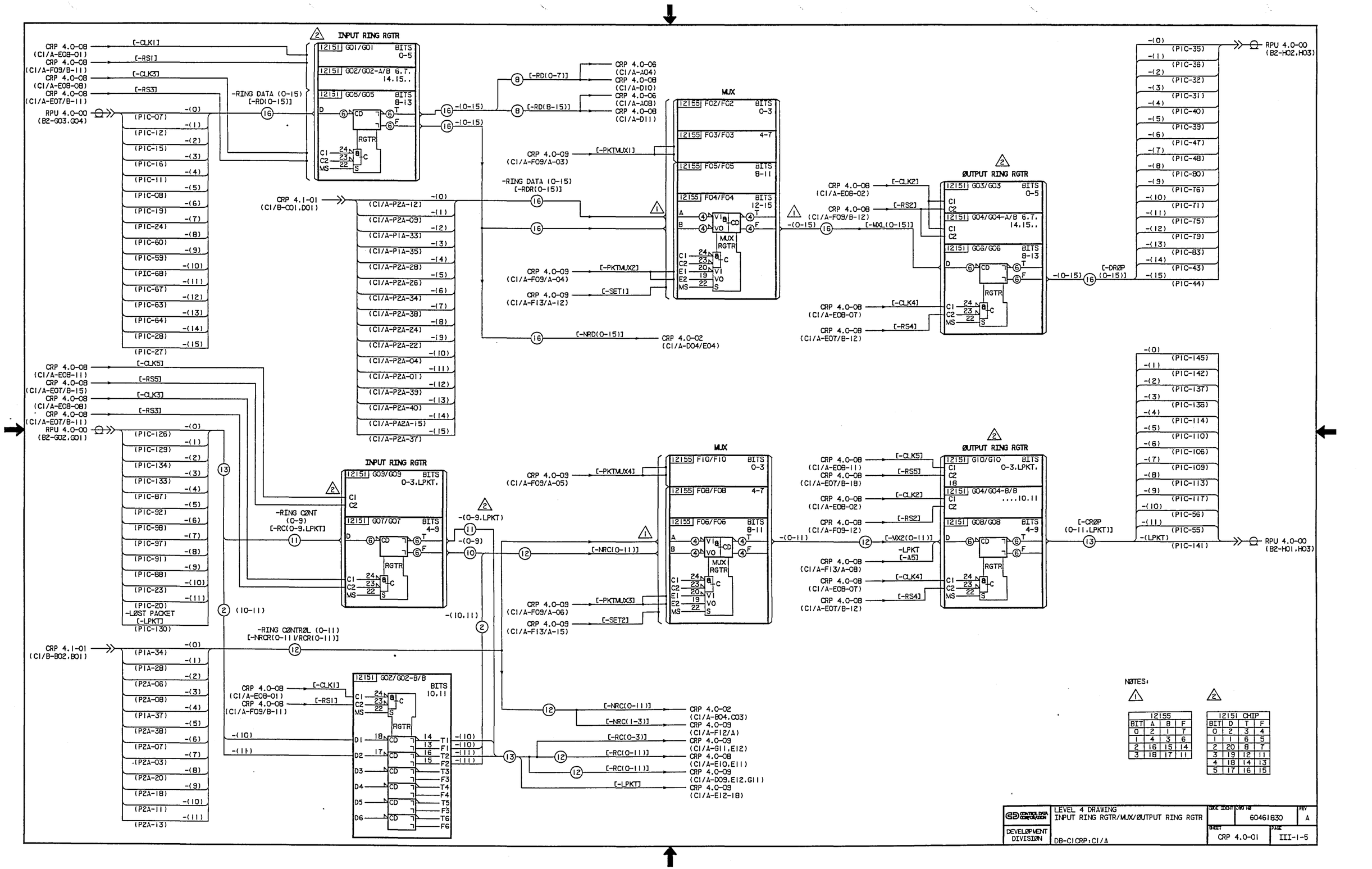
CONTROL DATA CORPORATION

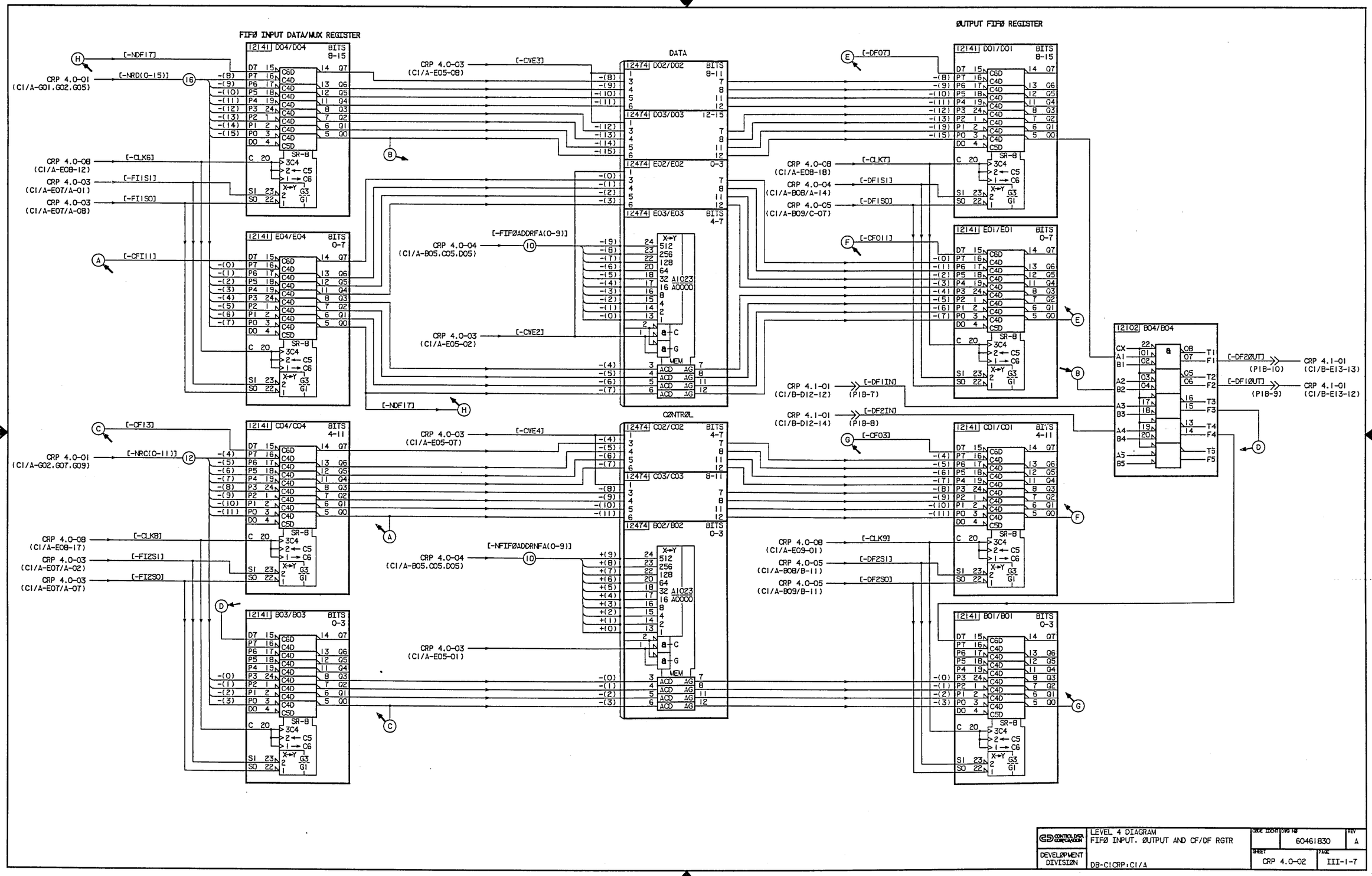
DEVELØPMENT DIVISIØN

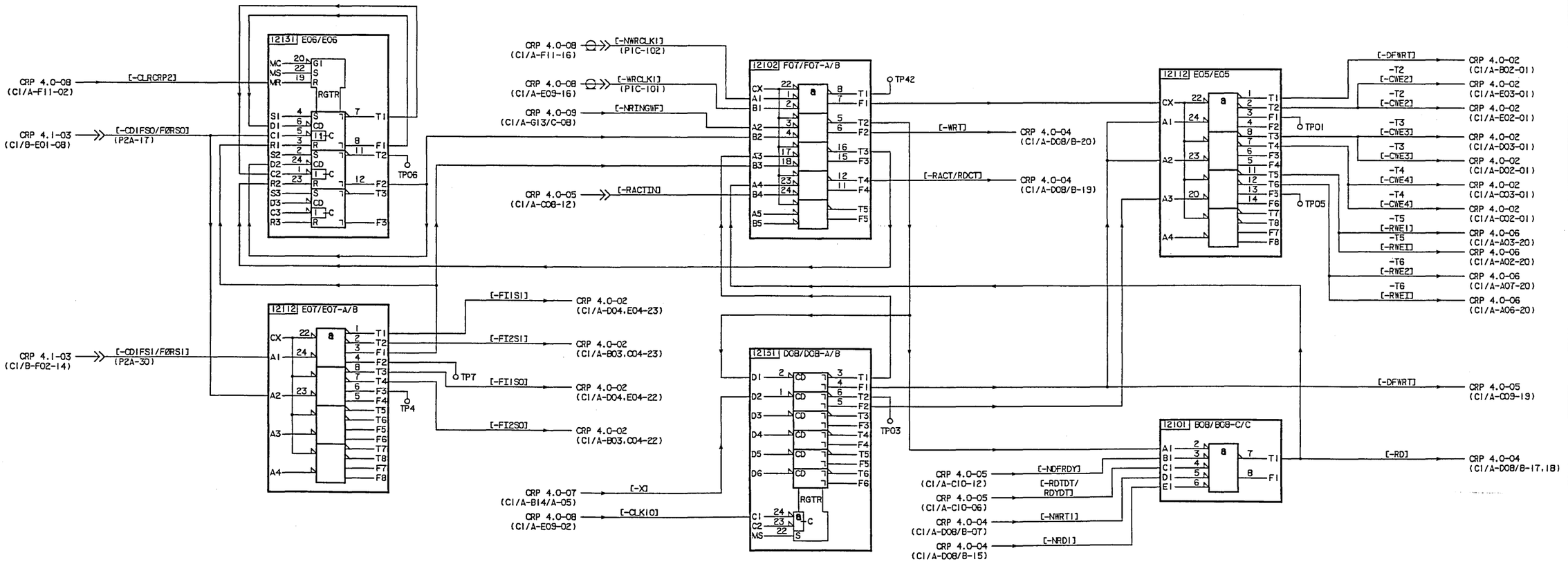
LEVEL 2 DIAGRAM
CRP BLØCK DIAGRAM

CODE IDENT 60461830 REV A

SHEET CRP 2.0 PAGE III-1-3


INPUT RING RGTR
12151 G01/G01 BITS 0-5
12151 G02/G02-A/B 6,7, 14,15,,
12151 G05/G05 BITS 8-13
RGTR
-RING DATA (0-15) [-RD(0-15)]
RPU 4.0-00 (B2-G03,G04)
(PIC-07) (PIC-12) (PIC-15) (PIC-16) (PIC-11) (PIC-08) (PIC-19) (PIC-24) (PIC-60) (PIC-59) (PIC-68) (PIC-67) (PIC-63) (PIC-64) (PIC-28) (PIC-27)
[-CLK1] [-RS1] [-CLK3] [-RS3]
CRP 4.0-08 (C1/A-E08-01)
CRP 4.0-08 (C1/A-F09/B-11)
CRP 4.0-08 (C1/A-E08-08)
CRP 4.0-08 (C1/A-E07/B-11)
[-RD(0-7)] [-RD(8-15)]
CRP 4.0-06 (C1/A-A04)
CRP 4.0-08 (C1/A-D10)
CRP 4.0-06 (C1/A-A08)
CRP 4.0-08 (C1/A-D11)
MUX
12155 F02/F02 BITS 0-3
12155 F03/F03 4-7
12155 F05/F05 BITS 8-11
12155 F04/F04 BITS 12-15
MUX RGTR
CRP 4.0-09 (C1/A-F09/A-03)
[-PKTMUX1]
CRP 4.0-09 (C1/A-F09/A-04)
[-PKTMUX2]
CRP 4.0-09 (C1/A-F13/A-12)
[-SET1]
-RING DATA (0-15) [-RDR(0-15)]
CRP 4.1-01 (C1/B-C01,D01)
(C1/A-P2A-12) (C1/A-P2A-09) (C1/A-P1A-33) (C1/A-P1A-35) (C1/A-P2A-28) (C1/A-P2A-26) (C1/A-P2A-34) (C1/A-P2A-38) (C1/A-P2A-24) (C1/A-P2A-22) (C1/A-P2A-04) (C1/A-P2A-01) (C1/A-P2A-39) (C1/A-P2A-40) (C1/A-PA2A-15) (C1/A-P2A-37)
[-NRD(0-15)]
CRP 4.0-02 (C1/A-D04/E04)
ØUTPUT RING RGTR
12151 G03/G03 BITS 0-5
12151 G04/G04-A/B 6,7, 14,15,,
12151 G06/G06 BITS 8-13
[-MXL(0-15)]
CRP 4.0-08 (C1/A-E08-02)
CRP 4.0-08 (C1/A-F09/B-12)
[-CLK2] [-RS2]
CRP 4.0-08 (C1/A-E08-07)
CRP 4.0-08 (C1/A-E07/B-12)
[-CLK4] [-RS4]
[-DR2P (0-15)]
(PIC-35) (PIC-36) (PIC-32) (PIC-31) (PIC-40) (PIC-39) (PIC-47) (PIC-48) (PIC-80) (PIC-76) (PIC-71) (PIC-75) (PIC-79) (PIC-83) (PIC-43) (PIC-44)
RPU 4.0-00 (B2-H02,H03)
CRP 4.0-08 (C1/A-E08-11)
CRP 4.0-08 (C1/A-E07/B-15)
CRP 4.0-08 (C1/A-E08-08)
CRP 4.0-08 (C1/A-E07/B-11)
[-CLK5] [-RS5] [-CLK3] [-RS3]
RPU 4.0-00 (B2-G02,G01)
(PIC-126) (PIC-129) (PIC-134) (PIC-133) (PIC-87) (PIC-92) (PIC-98) (PIC-97) (PIC-91) (PIC-88) (PIC-23) (PIC-20) -LØST PACKET [-LPKT] (PIC-130)
INPUT RING RGTR
12151 G09/G09 BITS 0-3,LPKT,
12151 G07/G07 BITS 4-9
-RING CØNT (0-9) [-RC(0-9,LPKT)]
-(0-9,LPKT)
-(0-9)
-(10,11)
(10-11)
-RING CØNTRØL (0-11) [-NRCR(0-11)/RCR(0-11)]
CRP 4.1-01 (C1/B-B02,B01)
(P1A-34) (P1A-28) (P2A-06) (P2A-08) (P1A-37) (P2A-38) (P2A-07) (P2A-03) (P2A-20) (P2A-18) (P2A-11) (P2A-13)
12151 G02/G02-B/B BITS 10,11
CRP 4.0-08 (C1/A-E08-01)
CRP 4.0-08 (C1/A-F09/B-11)
[-CLK1] [-RS1]
MUX
12155 F10/F10 BITS 0-3
12155 F08/F08 4-7
12155 F06/F06 BITS 8-11
MUX RGTR
CRP 4.0-09 (C1/A-F09/A-05)
[-PKTMUX4]
CRP 4.0-09 (C1/A-F09/A-06)
[-PKTMUX3]
CRP 4.0-09 (C1/A-F13/A-15)
[-SET2]
[-NRC(0-11)]
[-NRC(0-3)]
[-NRC(1-3)]
[-RC(0-11)]
[-RC(0-11)]
[-LPKT]
CRP 4.0-02 (C1/A-B04,C03)
CRP 4.0-09 (C1/A-F12/A)
CRP 4.0-09 (C1/A-G11,E12)
CRP 4.0-08 (C1/A-E10,E11)
CRP 4.0-09 (C1/A-D09,E12,G11)
CRP 4.0-09 (C1/A-E12-18)
ØUTPUT RING RGTR
12151 G10/G10 BITS 0-3,LPKT,
12151 G04/G04-B/B ,,,,10,11
12151 G08/G08 BITS 4-9
[-LPKT [-A5]
CRP 4.0-08 (C1/A-E08-11)
CRP 4.0-08 (C1/A-E07/B-18)
CRP 4.0-08 (C1/A-E08-02)
CRP 4.0-08 (C1/A-F09-12)
CRP 4.0-08 (C1/A-F13/A-08)
CRP 4.0-08 (C1/A-E08-07)
CRP 4.0-08 (C1/A-E07/B-12)
[-CLK5] [-RS5] [-CLK2] [-RS2] [-CLK4] [-RS4]
[-CRØP (0-11,LPKT)]
(PIC-145) (PIC-142) (PIC-137) (PIC-138) (PIC-114) (PIC-110) (PIC-106) (PIC-109) (PIC-113) (PIC-117) (PIC-56) (PIC-55) -(LPKT) (PIC-141)
RPU 4.0-00 (B2-H01,H03)
NØTES:
12155
12151 CHIP
LEVEL 4 DRAWING
INPUT RING RGTR/MUX/ØUTPUT RING RGTR
DEVELØPMENT DIVISIØN
DB-C1CRP:C1/A
60461830
A
CRP 4.0-01
III-1-5


FIFØ INPUT DATA/MUX REGISTER
ØUTPUT FIFØ REGISTER
DATA
CØNTRØL
[-NDF17]
CRP 4.0-01 (CI/A-G01,G02,G05)
[-NRD(0-15)]
CRP 4.0-08 (CI/A-E08-12)
[-CLK6]
CRP 4.0-03 (CI/A-E07/A-01)
[-FI1SI]
CRP 4.0-03 (CI/A-E07/A-08)
[-FI1SO]
[-CF11]
[-CWE3]
CRP 4.0-03 (CI/A-E05-08)
[-FIFØADDRFA(0-9)]
CRP 4.0-04 (CI/A-B05,C05,D05)
[-CWE2]
CRP 4.0-03 (CI/A-E05-02)
[-CF13]
CRP 4.0-01 (CI/A-G02,G07,G09)
[-NRC(0-11)]
CRP 4.0-08 (CI/A-E08-17)
[-CLK8]
CRP 4.0-03 (CI/A-E07/A-02)
[-FI2SI]
CRP 4.0-03 (CI/A-E07/A-07)
[-FI2SO]
[-CWE4]
CRP 4.0-03 (CI/A-E05-07)
[-NFIFØADDRNFA(0-9)]
CRP 4.0-04 (CI/A-B05,C05,D05)
CRP 4.0-03 (CI/A-E05-01)
[-DF0T]
CRP 4.0-08 (CI/A-E08-18)
[-CLK7]
CRP 4.0-04 (CI/A-B08/A-14)
[-DF1SI]
CRP 4.0-05 (CI/A-B09/C-07)
[-DF1SO]
[-CF01]
CRP 4.1-01 (CI/B-D12-12)
[-DF1IN]
(PIB-7)
CRP 4.1-01 (CI/B-D12-14)
[-DF2IN]
(PIB-8)
[-CF03]
CRP 4.0-08 (CI/A-E09-01)
[-CLK9]
CRP 4.0-05 (CI/A-B08/B-11)
[-DF2SI]
CRP 4.0-05 (CI/A-B09/B-11)
[-DF2SO]
[-DF2ØUT]
(PIB-10)
CRP 4.1-01 (CI/B-E13-13)
[-DF1ØUT]
(PIB-9)
CRP 4.1-01 (CI/B-E13-12)
LEVEL 4 DIAGRAM
FIFØ INPUT, ØUTPUT AND CF/DF RGTR
DEVELOPMENT DIVISION
DB-CICRP:CI/A
60461830
A
CRP 4.0-02
III-1-7



CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM CONTROL	CODE IDENT	DWG NO 60461830 REV A
DEVELOPMENT DIVISION	DB-CICRP:CI/A	SHEET CRP 4.0-03	SIZE III-1-9

FIFØ READ ADDR

FIFØ WRITE ADDR

MUX

12136 B07/B07 BITS 8,9
12136 C07/ BITS 4-7
12136 D07/D07 BITS 0-3
12136 B06/B06
12136 C06/C06
12136 D06/D06
12155 B05/B05 BITS 8,9
12155 C05/C05 BITS 4-7
12155 D05/D05 BITS 0-3
12131 D08/D08-B/B
16CNTR/SR-4
MUX RGTR
RGTR

CRP 4.0-08 (C1/A-E08-02) [-NCLK1]
CRP 4.0-08 (C1/A-E08-04) [-NCLK2]
CRP 4.0-05 (C1/A-C10-15) [-CLRF1]
CRP 4.0-05 (C1/A-C10-14) [-CLRF2]
CRP 4.0-03 (C1/A-F07/A-06) [-WRT]
CRP 4.0-03 (C1/A-F07/A-12) [-RACT/RDCT]
CRP 4.0-03 (C1/A-B08/C-07) [-RD]
CRP 4.0-08 (C1/A-E08-06) [-NCLK3]
CRP 4.0-08 (C1/A-E08-05) [-NCLK4]

[-NWRT1] CRP 4.0-05 (C1/A-C09-04)
[-NWRT1] CRP 4.0-03 (C1/A-B08/C-05)
[-UDT] CRP 4.0-05 (C1/A-C09-02,03)
[-RD1] CRP 4.0-05 (C1/A-C10-02)
[-NRD1] CRP 4.0-03 (C1/A-B08/C-06)

[FIFØADDRFA(0-9)] CRP 4.0-02 (C1/A-E02,E03,D02,D03)
[NFIFØADDRNFA(0-9)] CRP 4.0-02 (C1/A-B02,C02,C03)

TP02
TP19

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM FIFØ READ ADDR/FIFØ WRITE ADDR/MUX	CAGE IDENT / DWG NO: 60461830	REV: A
DEVELOPMENT DIVISION	DB-C1CRP.C1/A	SHEET: CRP 4.0-04	PAGE: III-1-11

READY DETECT

FULL DETECT

FIFØ UP/DØWN CØUNT

[+NUD(1-9)]

[-UD(0-9)]

12136 A09/A09 BITS 8,9

12136 A10/A10 BITS 4-7

12136 A11/A11 BITS 0-3

12101 B10/B10-C/C BITS 5-9

12101 B10/B10-B/C BITS 0-4

12101 B10/B10-A/C

12101 B11/B11-C/C

12101 B11/B11-B/C BITS 5-9

12101 B11/B11-A/C BITS 3,4

12101 B09/B09-C/C

12101 B09/B09-B/C

12101 B08/B08-A/C

12101 B08/B08-B/C

12102 C10/C10

12102 C09/C09

12131 C08/C08

12102 D13/D13-A/C

DF ØUTPUT CØNTRØL RGTR

CRP 4.0-08 (C1/A-E09-08) [-CLK11]

CRP 4.1-03 (C1/B-D11-04) [-CLRFIFØ] (P1B-21)

CRP 4.0-04 (C1/A-D08/B-11) [-UDT]

CRP 4.0-04 (C1/A-D08/B-07) [-NWRT1]

CRP 4.0-08 (C1/A-F11-01) [-CLRCRP1]

CRP 4.0-03 (C1/A-D08/A-04) [-DFWRT]

CRP 4.1-03 (C1/B-F02-16) [-CDOFS1/DFRS1] (P1A-21)

CRP 4.1-03 (C1/B-E01-12) [-CDOFS0/DFRS0] (P1A-04)

CRP 4.1-04 (C1/B-A12-04) [-RAD4/AD4] (P1A-24)

CRP 4.0-09 (C1/A-C12/B-19) [/SHF1]

[-NUD2] (P1C-153)

[-NUD1] (P1C-154)

[-RINGSTØP] (P2A-10) CRP 4.1-02 (C1/B-F07/B-06)

CRP 4.0-08 (C1/A-E09-08) [-CLK11]

CRP 4.0-04 (C1/A-D08/B-16) [-RD1]

[-RACTIN] CRP 4.0-03 (C1/A-F07/A-24)

[-RACTIN] CRP 4.0-09 (C1/A-F12/B-24)

[-NDFRDY] CRP 4.0-03 (C1/A-B08/C-03)

[-DFISO] CRP 4.0-02 (C1/A-D01, E01-22)

[-DF2SO] CRP 4.0-02 (C1/A-B01-22)

[-DF2SO] CRP 4.0-02 (C1/A-C01-22)

[-DF1SI] CRP 4.0-02 (C1/A-D01-23)

[-DF1SI] CRP 4.0-02 (C1/A-E01-23)

[-DF2SI] CRP 4.0-02 (C1/A-C01-23)

[-DF2SI] CRP 4.0-02 (C1/A-B01-23)

[-RDTDT/ -RDYDT] CRP 4.0-03 (C1/A-B08/C-04)

[-CLRF1] CRP 4.0-04 (C1/A-B07, C07, D07-22)

[-CLRF2] CRP 4.0-04 (C1/A-D06, C06, B06-23)

[-DFRDY] (P1A-20) CRP 4.1-04 (C1/B-D08-02)

TP23 TP11 TP20 TP9 TP26 TP10 TP12 TP8

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM FIFØ UP/DØWN CØUNT/READY DETECT/ FULL DETECT/DF ØUTPUT RGTR CØNTRØL	CRDE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-C1CRP:C1/A	SHEET CRP 4.0-05	SIZE III-1-13

REQUEST STACK

REQUEST STACK INPUT REGISTER

REQUEST STACK ØUTPUT REGISTER

CRP 4.0-07 (CI/A-AI2) [-WRA(0-3)]
CRP 4.0-07 (CI/A-BI2) [-RRA(0-3)]
CRP 4.0-03 (CI/A-E05-11) [-RWE1]
CRP 4.0-07 (CI/A-AI4-12) [-CLRMEM]
CRP 4.1-01 (CI/B-DI2-13) [-RQSTSI/RQIN] (CI/A-PIB-11)
CRP 4.0-01 (CI/A-G01,G02) [-RD(0-7)]
CRP 4.0-08 (CI/A-E09-07) [-CLK12]
CRP 4.0-07 (CI/A-AI4-08) [-RIRSI]
CRP 4.0-07 (CI/A-AI4-05) [-RIRSO]
CRP 4.0-01 (CI/A-G02,G05) [-RD(8-15)]
CRP 4.0-03 (CI/A-E05-12) [-RWE2]
CRP 4.0-07 (CI/A-AI4-12) [-CLRMEM]
CRP 4.0-08 (CI/A-E09-11) [-CLK13]
CRP 4.0-07 (CI/A-CII/C-07) [-RQRSI]
CRP 4.0-07 (CI/A-CII/B-11) [-RQRSO]
[-RQXOUT] (PIB-3) CRP 4.1-01 (CI/B-EI3-14)

12143 A02/A02
12143 A03/A03
12145 A06/A06
12145 A07/A07
12141 A04/A04
12141 A08/A08
12141 A01/A01
12141 A05/A05

MEM

LEVEL 4 DIAGRAM	ORDER IDENT	DWG NO	REV
RQ STK INPUT RGTR/REQ STACK/ RQ STK ØUTPUT RGTR		60461830	A
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	DB-CICRP:CI/A	SHEET CRP 4.0-06	PAGE III-1-15

REQUEST UP/DOWN COUNT

12136 A13/A13

16CNTR/SR-4

12102 DI3/DI3-C/C

12101 BI3/BI3-C/C

12101 BI3/BI3-B/C

12101 BI3/BI3-A/C

12131 CI3/CI3

RGTR

12102 AI4/AI4

12102 BI4/BI4-A/B

12131 CI2/CI2-A/B

REQUEST STACK WRITE ADDRESS

12136 AI2/AI2

REQUEST STACK READ ADDRESS

12136 BI2/BI2

12101 CII/CII-C/C

12101 CII/CII-B/C

12101 CII/CII-A/C

-CLOCK 14 [-CLK14]

CRP 4.0-08 (CI/A-E09-12)

CRP 4.0-09

CRP 4.2-03 (CI/C-A09-15)

-READ [-RD] (PIB-02)

[-RUD3] [-NRUD3] [-RUD2] [-NRUD2] [-RUD1] [-RUD0]

CRP 4.1-03 (CI/B-CII-04)

[-DRQRS] (PIB-04)

[-RQRS] (PIA-12)

CRP 4.1-02 (CI/B-F07/B, E06/A-05.03)

TP35

CRP 4.1-03 (CI/B-E02-03)

[-RQSI] (PIA-18)

CRP 4.1-03 (CI/B-E01-14)

[-RQSO] (PIA-26)

CRP 4.1-04 (CI/B-AI2-06)

+DIAGNOSTIC [-NDW/NDIAG] (PIA-07)

[-RIRSI]

CRP 4.0-06 (CI/A-A08-23)

[-RIRSO]

CRP 4.0-06 (CI/A-A08-22)

CRP 4.1-03 (CI/B-E09-13)

[-CLRRQ] (P2B-06)

CRP 4.0-08 (CI/A-FII-01)

[-CLRCRPI]

[-CLRMEM]

CRP 4.0-06 (CI/A-A02, A03-22)

[-CLRMEM]

CRP 4.0-06 (CI/A-A06, A07-22)

-WRITE TP17

-REQUEST STACK READY [-RQSTKRDY] (PIA-23)

CRP 4.1-04 (CI/B-D08-03)

CRP 4.0-09 (CI/A-GI3/B-12)

[-NRINGWR]

CRP 4.1-02 (CI/B-G05-14)

-RING STOP INTERRUPT [-RSIN] (PIC-15B)

[-RSIN]

CRP 4.0-08 (CI/A-F09/B, E07/B)

[-X]

CRP 4.0-03 (CI/A-D08/A-01)

CRP 4.0-08 (CI/A-E09-02)

[-CLK10]

-REQUEST STACK WRITE ADDRESS 3 [-WRA3] → CRP 4.0-06 (CI/A-A02-02)

-REQUEST STACK WRITE ADDRESS 2 [-WRA2] → CRP 4.0-06 (CI/A-A02-01)

-REQUEST STACK WRITE ADDRESS 1 [-WRA1] → CRP 4.0-06 (CI/A-A02-24)

-REQUEST STACK WRITE ADDRESS 0 [-WRA0] → CRP 4.0-06 (CI/A-A02-23)

TP14

TP15

-REQUEST STACK READ ADDRESS 3 [-RRA3] → CRP 4.0-06 (CI/A-A02-03)

-REQUEST STACK READ ADDRESS 2 [-RRA2] → CRP 4.0-06 (CI/A-A02-04)

-REQUEST STACK READ ADDRESS 1 [-RRA1] → CRP 4.0-06 (CI/A-A02-05)

-REQUEST STACK READ ADDRESS 0 [-RRA0] → CRP 4.0-06 (CI/A-A02-06)

TP13

TP16

-REQUEST RING SHIFT 1 [-RQRSI] → CRP 4.0-06 (CI/A-A01-23)

TP25

-REQUEST RING SHIFT 0 [-RQRSO] → CRP 4.0-06 (CI/A-A01-22)

TP24

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM READ/WRITE REQUEST STACKS REQUEST UP/DOWN COUNT	DRAWING NUMBER 60461830	REV A
DEVELOPMENT DIVISION	DB-CICRP:CI/A	SHEET CRP 4.0-07	PAGE III-1-17

CONTROL RGTR

LØST PACKET RGTR

DATA RGTR

SYSTEM CLØCK FANØUT

12141 E10/E10

12141 D10/D10

12141 E11/E11

12141 D11/D11

12102 D12/D12

12112 E08/E08

12112 E09/E09

12112 F11/F11

12112 F09/F09-B/B

12112 E07/E07-B/B

12102 F07/F07-B/B

RING STØP

CRP 4.1-01 (CI/B-D12-06)

[-LP1S1] (P2B-04)

CRP 4.0-01 (CI/A-G09)

[-RC(0-3)]

CRP 4.1-01 (CI/B-D12-11)

[-LP2S1] (P2B-01)

CRP 4.0-01 (CI/A-G01,G02)

[-RD(0-7)]

CRP 4.0-01 (CI/A-G07,G02/B)

[-RC(4-11)]

[-CLK15]

CRP 4.0-01 (CI/A-G02,G05)

[-RD(8-15)]

[-CLK16]

-LØST PACKET 1 [-LP1] (P2B-17)

CRP 4.1-01 (CI/B-E13-16)

[-LP2] (P2B-15)

CRP 4.1-01 (CI/B-E13-15)

CRP 4.1-03 (CI/B-D12-11)

[-LP1S1] (P1A-01)

CRP 4.1-03 (CI/B-D02-3)

[-LP1S0] (P1A-06)

CRP 4.1-03 (CI/B-E02-06)

[-LP2S1] (P1A-02)

CRP 4.0-09 (CI/A-G12-11)

[-ELP2S1]

CRP 4.1-03 (CI/B-E01-16)

[-LP2S0] (P1A-03)

CRP 4.0-09 (CI/A-E12-12)

[-LP]

[-LP2S1]

CRP 4.0-09 (CI/A-F12/C,G12-04,24)

TP28

TP31

TP30

TP29

TP27

TP21

CRP 4.0-07 (CI/A-C12/A-08)

[-RSIN]

[-RS1]

CRP 4.0-01 (CI/A-G02,G01-23)

[-RS2]

CRP 4.0-01 (CI/A-G03,G04-23)

[-RS3]

CRP 4.0-01 (CI/A-G05,G07-23)

[-RS4]

CRP 4.0-01 (CI/A-G06,G08-23)

[-RS5]

CRP 4.0-01 (CI/A-G09,G10-23)

[-RS6]

CRP 4.0-09 (CI/A-G13-06,15,20)

CRP 4.1-04 (CI/B-C08-05)

[-CLRCRP]

(PIA-13)

CRP 4.2-06 (CI/C-G11/B-06)

[-SCLK2] (P1C-105)

[-CLK1] CRP 4.0-01 (CI/A-G01,G02-24)

[-CLK2] CRP 4.0-01 (CI/A-G03,G04-24)

[-CLK3] CRP 4.0-01 (CI/A-G05,G07-24)

[-CLK4] CRP 4.0-01 (CI/A-G06,G08-24)

[-CLK5] CRP 4.0-01 (CI/A-G09-24)

[-CLK6] CRP 4.0-02 (CI/A-E04,D04-20)

[-NCLK5] (P2A-32) NU

[-CLK7] CRP 4.0-09 (CI/A-G13/A,G14)

CRP 4.0-02 (CI/A-E01,D01-20)

[-CLK8] CRP 4.0-02 (CI/A-C04,B03-20)

[-CLK9] CRP 4.0-02 (CI/A-C01,B01-20)

[-CLK10] CRP 4.0-03 (CI/A-D08/A-24)

[-CLK10] CRP 4.0-08 (CI/A-A12,B12-20)

[-CLK11] CRP 4.0-05 (CI/A-A09,A10, A11,C10)

[-CLK12] CRP 4.0-06 (CI/A-A04-20)

[-NCLK11] (P1C-118) NU

[-NCLK12] (P1C-122) NU

[-CLK13] CRP 4.0-06 (CI/A-A01,A05-20)

[-CLK14] CRP 4.0-07 (CI/A-A13,C12/A-20,24)

[-WRCLK1] (P1C-125)

[-WRCLK2] (P1C-121)

CRP 4.0-03 (CI/A-F07/A-02)

[-CLRCRP1] CRP 4.0-07 (CI/A-A14-20)

[-CLRCRP1] CRP 4.0-05 (CI/A-C09-18)

[-CLRCRP2] CRP 4.0-03 (CI/A-E06-19)

[-CLRCRP2] CRP 4.0-09 (CI/A-G14-19)

[-NCLK1] CRP 4.0-04 (CI/A-B07, C07,D07-20)

[-NCLK2] CRP 4.0-04 (CI/A-B06, C06,D06-20)

[-NCLK3] CRP 4.0-04 (CI/A-B05,C05-24)

[-NCLK4] CRP 4.0-04 (CI/A-D05-24)

[-NWRCLK1] (P1C-157) CRP 4.0-03 (CI/A-F07/A-01)

[-CLK17] CRP 4.0-09 (CI/A-G14, G13-20,17)

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM LØST PACKET RGTR/RING STØP/CLØCK FANØUT	CODE IDENT	DWG NO 60461830 REV A
DEVELOPMENT DIVISION	DB-CICRP:CI/A	SHEET CRP 4.0-08	SIZE III-1-19

RING FUNCTION DECODE

12170 G11/G11

DEMUX

12101 F12/F12-A/C

12101 E13/E13

12102 G12/G12

12102 F13/F13-A/B

12101 G13/G13-C/C

12101 G13/G13-B/C

12101 G13/G13-A/C

12131 G14/G14

12102 E12/E12

12102 D13/D13-B/C

BIAS LØ=22

12102 B14/B14-B/B

BIAS LØ=22

12101 B09/B09-A/C

12101 F12/F12-C/C

ADDRESS COMPARE

12166 D09/D09

12131 C12/C12-B/B

RGTR

12101 F12/F12-B/C

12102 F13/F13-B/B

BIAS LØ=22

12102 F14/F14-A/B

BIAS LØ=22

12102 F14/F14-B/B

BIAS LØ=22

12112 F09/F09-A/B

CRP 4.0-01 (CI/A-G09-06) [-RC1]

CRP 4.0-01 (CI/A-G09-08) [-RC2]

CRP 4.0-01 (CI/A-G09-11) [-RC3]

[-NRC(1-3)]

CRP 4.0-01 (CI/A-G09)

CRP 4.1-03 (CI/B-D11-07) [-NALLRT] (P2B-02)

CRP 4.0-01 (CI/A-G09-03) [-RC0]

CRP 4.0-01 (CI/A-G09-14) [-LPKT]

[-LP] CRP 4.0-08 (CI/A-D12-24)

-RING CØNTRØL 4 [-RC4]

CRP 4.0-01 (CI/A-G07-03) -RING CØNTRØL 5 [-RC5]

CRP 4.0-01 (CI/A-G07-06) -RING CØNTRØL 6 [-RC6]

CRP 4.0-01 (CI/A-G07-08) -RING CØNTRØL 7 [-RC7]

CRP 4.0-01 (CI/A-G07-12) -RING CØNTRØL 8 [-RC8]

CRP 4.0-01 (CI/A-G07-14) -RING CØNTRØL 9 [-RC9]

CRP 4.0-01 (CI/A-G07-16) -RING CØNTRØL 10 [-RC10]

CRP 4.0-01 (CI/A-G02-14) -RING CØNTRØL 11 [-RC11]

CRP 4.0-01 (CI/A-G02-16)

CØN 4.6-00 AI(REAR)-SW3 [-SW3(1)] (P2B-13)

[-SW3(2)] (P2B-11)

[-SW3(3)] (P2B-19)

[-SW3(4)] (P2B-18)

[-SW3(5)] (P2B-09)

[-SW3(6)] (P2B-10)

[-SW3(7)] (P2B-12)

[-SW3(8)] (P2B-14)

CRP 4.1-04 (CI/B-C10/A-13) [-NDFRD] (P1A-31)

CRP 4.1-03 (CI/B-C11-15) [-DLPD] (P2A-33)

CRP 4.1-03 (CI/B-E09-15) [-CLRLP] (P2B-07)

CRP 4.0-08 (CI/A-D12-18) [-LP2SI]

CRP 4.0-05 (CI/A-B10/A-14) [-SHFI]

CRP 4.2-06 (CI/C-E09/A-14) [-CLRENDI] (P2A-21)

CRP 4.0-05 (CI/A-C08-12) [-RACTIN]

CRP 4.0-05 (CI/A-D09-17) [-CLRFIFØ]

[-EPKT] (P2A-29) CRP 4.1-04 (CI/B-C08-23)

CRP 4.1-04 (CI/B-C08-15) [-NPKTRDY] (P2A-27)

[-ELP2SI] CRP 4.0-08 (CI/A-D12-19)

CRP 4.0-08 (CI/A-E07/B-17) [-RS6]

CRP 4.0-08 (CI/A-E08-18) [-CLKT]

CRP 4.0-08 (CI/A-F11-02) [-CLRCRP2]

-END ØF TRANSFER [-EØT] (P2A-35) CRP 4.1-04 (CI/B-C09-13)

[-A5] CRP 4.0-01 (CI/A-G10-18)

[-SET1] CRP 4.0-01 (CI/A-F03-22)

[-SET2] CRP 4.0-01 (CI/A-F06-22)

[-NRINGWF] CRP 4.0-03 (CI/A-F07/A-03)

[-NRINGWR] CRP 4.0-07 (CI/A-B14/A-03)

[-LPKT] (P1A-29) CRP 4.1-04 (CI/B-D08-18)

[-WLP] (P1A-30) CRP 4.1-04 (CI/B-D08-17)

[-ENDFLAG] (P1A-31) CRP 4.1-04 (CI/B-D08-01)

[-PKTMUX1] CRP 4.0-01 (CI/A-F02-20)

[-PKTMUX2] CRP 4.0-01 (CI/A-F05-20,19)

[-PKTMUX3] CRP 4.0-01 (CI/A-F08-20)

[-PKTMUX4] CRP 4.0-01 (CI/A-F10-20)

TP18 TP37 TP38 TP36 TP34 TP45 TP44 TP43 TP33 TP32 TP22 TP41 TP40 TP39

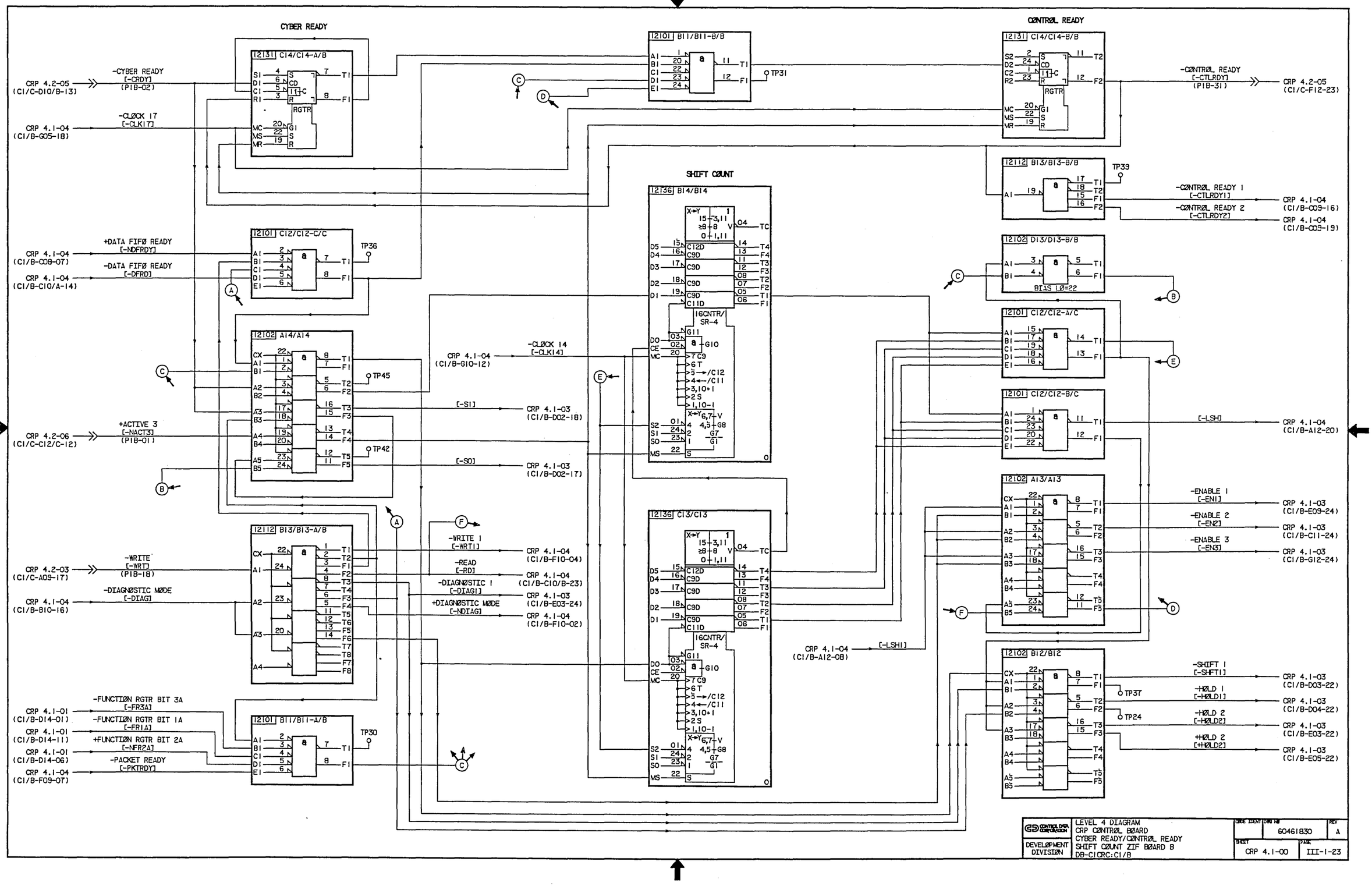
CONTROLDATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
RING FUNCTION DECODE
ADDRESS COMPARE EPKT

DB-CICRP:CI/A

CODE IDENT | DWG NO 60461830 | REV A

SHEET CRP 4.0-09 | PAGE III-1-21


CYBER READY
CONTROL READY
SHIFT COUNT
CRP 4.2-05 (C1/C-D10/B-13)
-CYBER READY [-CRDY] (P1B-02)
-CLOCK 17 [-CLK17]
CRP 4.1-04 (C1/B-G05-18)
+DATA FIFO READY [-NDFRDY]
CRP 4.1-04 (C1/B-C08-07)
-DATA FIFO READY [-DFRD]
CRP 4.1-04 (C1/B-C10/A-14)
CRP 4.2-06 (C1/C-C12/C-12)
+ACTIVE 3 [-NACT3] (P1B-01)
CRP 4.2-03 (C1/C-A09-17)
-WRITE [-WRT] (P1B-18)
CRP 4.1-04 (C1/B-B10-16)
-DIAGNOSTIC MODE [-DIAG]
CRP 4.1-01 (C1/B-D14-01)
-FUNCTION RGTR BIT 3A [-FR3A]
CRP 4.1-01 (C1/B-D14-11)
-FUNCTION RGTR BIT 1A [-FR1A]
CRP 4.1-01 (C1/B-D14-06)
+FUNCTION RGTR BIT 2A [-NFR2A]
CRP 4.1-04 (C1/B-F09-07)
-PACKET READY [-PKTRDY]
-CLOCK 14 [-CLK14]
CRP 4.1-04 (C1/B-G10-12)
[-SI]
CRP 4.1-03 (C1/B-D02-18)
[-SO]
CRP 4.1-03 (C1/B-D02-17)
-WRITE 1 [-WRT1]
CRP 4.1-04 (C1/B-F10-04)
-READ [-RD]
CRP 4.1-04 (C1/B-C10/B-23)
-DIAGNOSTIC 1 [-DIAG1]
CRP 4.1-03 (C1/B-E03-24)
+DIAGNOSTIC MODE [-NDIAG]
CRP 4.1-04 (C1/B-F10-02)
CRP 4.1-04 (C1/B-A12-08)
[-LSH1]
-CONTROL READY [-CTLRDY] (P1B-31)
CRP 4.2-05 (C1/C-F12-23)
-CONTROL READY 1 [-CTLRDY1]
CRP 4.1-04 (C1/B-C09-16)
-CONTROL READY 2 [-CTLRDY2]
CRP 4.1-04 (C1/B-C09-19)
[-LSH]
CRP 4.1-04 (C1/B-A12-20)
-ENABLE 1 [-EN1]
CRP 4.1-03 (C1/B-E09-24)
-ENABLE 2 [-EN2]
CRP 4.1-03 (C1/B-C11-24)
-ENABLE 3 [-EN3]
CRP 4.1-03 (C1/B-G12-24)
-SHIFT 1 [-SHFT1]
CRP 4.1-03 (C1/B-D03-22)
-HOLD 1 [-HOLD1]
CRP 4.1-03 (C1/B-D04-22)
-HOLD 2 [-HOLD2]
CRP 4.1-03 (C1/B-E03-22)
+HOLD 2 [+HOLD2]
CRP 4.1-03 (C1/B-E05-22)
TP31
TP36
TP45
TP42
TP30
TP39
TP37
TP24
12101 B11/B11-B/B
12131 C14/C14-A/B
12131 C14/C14-B/B
12101 C12/C12-C/C
12102 A14/A14
12112 B13/B13-A/B
12101 B11/B11-A/B
12136 B14/B14
12136 C13/C13
12112 B13/B13-B/B
12102 D13/D13-B/B
12101 C12/C12-A/C
12101 C12/C12-B/C
12102 A13/A13
12102 B12/B12
16CNTR/SR-4
BIAS LØ=22
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
CRP CONTROL BOARD
CYBER READY/CONTROL READY
SHIFT COUNT ZIF BOARD B
DB-C1CRC:C1/B
CODE IDENTIFICATION NO 60461830
REV A
SHEET CRP 4.1-00
PAGE III-1-23

16 X 1 MUX

12164 E13/E13

CONTROL RGTR

12141 B02/B02 BITS ...0-3

12141 B01/B01 BITS 4-11

SHIFT RGTR

12141 F14/F14 BITS 0-7

12141 E14/E14 BITS 8-15

FUNCTION RGTR

12112 D14/D14

I X 16 MUX

12170 E12/E12

12170 D12/D12

DATA RGTR

12141 C01/C01 BITS 0-7

12141 D01/D01 BITS 8-15

12102 B03/B03

12101 C03/C03-A/B

12101 C03/C03-B/B

12102 C02/C02

12102 D13/D13-A/B

CRP 4.1-04 (CI/B-D08-05) [-GSWI]

CRP 4.1-02 (CI/B-E07-05) [-RS1I]

CRP 4.1-02 (CI/B-F04-05) [-RS2I]

CRP 4.0-08 (CI/A-E11-05) [-LP1I] (P2B-17)

CRP 4.0-08 (CI/A-D11-05) [-LP2I] (P2B-15)

CRP 4.0-06 (CI/A-A05-05) [-RQ OUT] (P1B-03)

CRP 4.0-02 (CI/A-B04-07) [-DF2 OUT] (P1B-10)

CRP 4.0-02 (CI/A-B04-06) [-DF1 OUT] (P1B-09)

CRP 4.1-03 (CI/B-D10-05) [-DIAG]

CRP 4.1-03 (CI/B-F13-05) [-RESET]

-CWI RING RGTR

PMI 4.0-04 (AI/L-G14/B-08) [-SERIN-1]

-MEM RING RGTR (P2B-29)

MRI 4.11-02 (AI/H-E08/B-13) [-SERIN-2]

-CWI STATUS (P2B-28)

PMI 4.0-03 (AI/L-E01/C-14) [-SERIN-3]

-HPM ERROR DET. (P2B-26)

MEL 4.0-05 (CI/D-G08/B-07) [-SERIN-4] (P2B-27)

[-FR3A] [-FR2A] [-FR1A] [-FR0A]

CRP 4.1-03 (CI/B-G09-01) [-CLK1]

CRP 4.1-03 (CI/B-D02-14) [-S1]

CRP 4.1-03 (CI/B-D02-16) [-S0]

CRP 4.1-04 (CI/B-B10) [-AD4]

[-AD3] [-AD2] [-AD1] [-AD0]

CRP 4.2-01 (CI/C-C13→D14) -HOLDING RGTR DATA (0-15) [-HR(0-15)/ -ID(0-15)]

CRP 4.1-03 (CI/B-E03,D03, E04,D04)

CRP 4.1-00 (CI/B-B11/A)

CRP 4.1-03 (CI/B-F01-16) [-CRSHFT]

CRP 4.1-03 (CI/B-F01-14) [-DRSHFT]

CRP 4.1-03 (CI/B-F01-15) [+CRSHFT]

CRP 4.1-03 (CI/B-F01-13) [+DRSHFT]

CRP 4.1-04 (CI/B-G09-02)

TP13 [-RCR15]

TP12 [-RCRSO] [+RCRSO]

TP11 [-RDRSO]

TP14 [-RDR15]

TP8

TP43

TP40

TP44

TP38

CRP 4.1-04 (CI/B-C10/C-07) [-ENCR/DR]

CRP 4.1-04 (CI/B-C10/C-08) [-NCR/DR]

-READ DATA (0-15) [-IR(0-15)] → CRP 4.2-02 (CI/B-F14,G14)

CRP 4.1-04 (CI/B-G09-08) [-CLK3]

-RING CONTROL (0-11) [-NRCR(0-11)/RCR(0-11)] → CRP 4.0-01 CRP RING

-RING DATA (0-15) [-NRDR(17-32/ RDR(0-15)] → CRP 4.0-01 (CI/A-F02→F04)

[-RCRSI] [-RSTSI] [-DIAGSI] [-DF1IN] [-DF2IN] [-RQSTSI/RQIN] [-LP2SI] [-LP1SI] [-RS2SI] [-RS1SI] [-GSWSI]

CRP 4.1-03 (CI/B-F12-15)

CRP 4.1-03 (CI/B-E10-15)

CRP 4.0-02 (CI/A-B04-17)

CRP 4.0-02 (CI/A-B04-19)

CRP 4.0-06 (CI/A-A04-15)

CRP 4.0-08 (CI/A-D10-15)

CRP 4.0-08 (CI/A-E10-15)

CRP 4.1-02 (CI/B-F03-15)

CRP 4.1-02 (CI/B-E08-15)

CRP 4.1-04 (CI/B-D07-15)

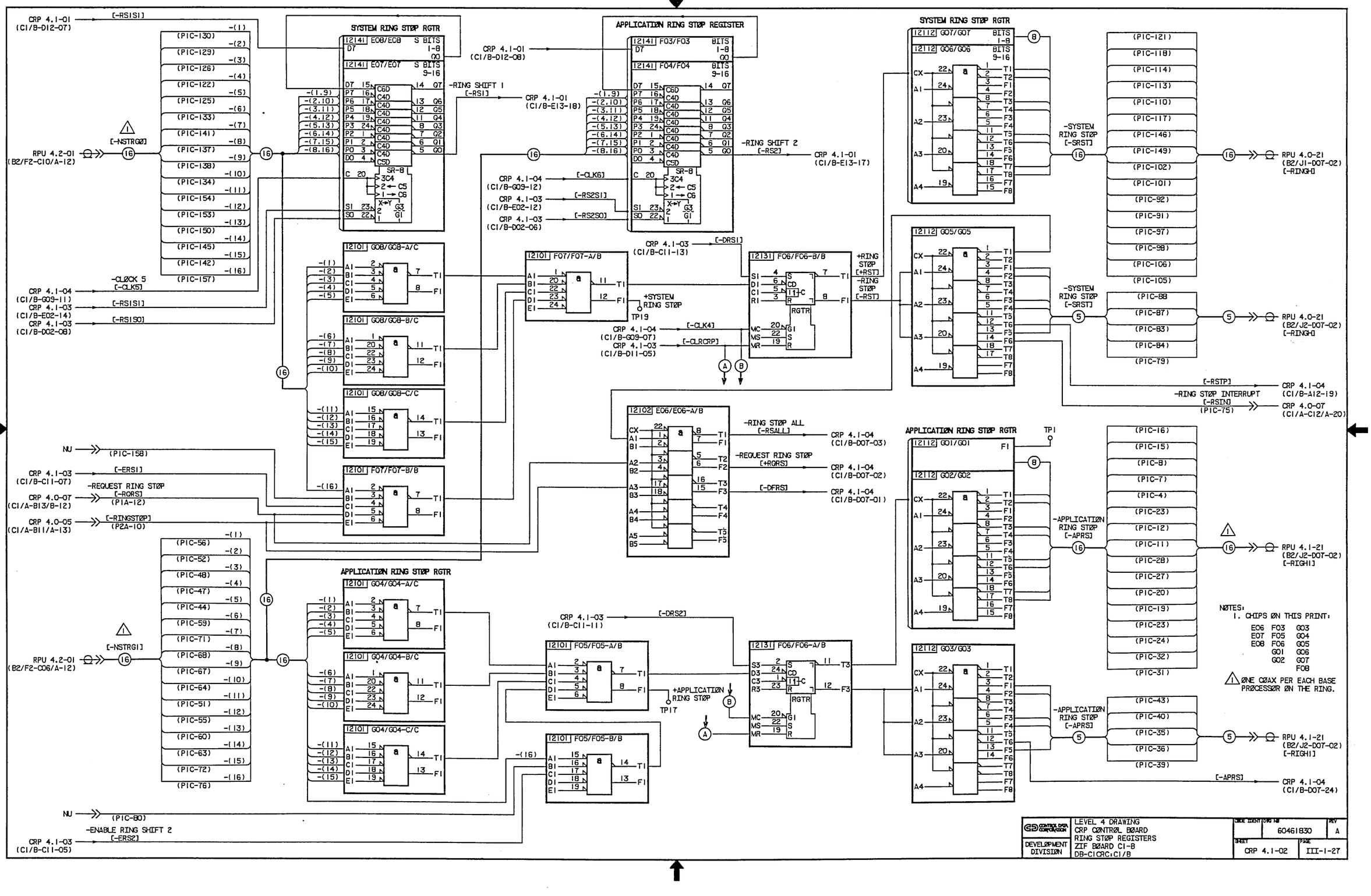
MEL 4.0-05 (CI/D-G12-20)

PMI 4.0-03 (AI/L-G06-02)

MRI 4.11-02 (AI/H-G08-20)

PMI 4.0-03 (AI/L-G13-02)

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM	DRAWING NO 60461830 REV A
	CRP CONTROL BOARD	
	CONTROL/DATA REGISTERS	
DEVELOPMENT DIVISION	I/O REGISTER, MUX/DMUX	SHEET CRP 4.1-01 PAGE III-1-25
	DB-C1CRC:C1/B	


SYSTEM RING STØP RGTR
APPLICATIØN RING STØP REGISTER
SYSTEM RING STØP RGTR
APPLICATIØN RING STØP RGTR
CRP 4.1-01 (CI/B-DI2-07)
[-RSISI]
RPU 4.2-01 (B2/F2-C10/A-12)
[-NSTRG0]
-CLØCK 5 [-CLK5]
CRP 4.1-04 (CI/B-G09-11)
CRP 4.1-03 (CI/B-E02-14)
CRP 4.1-03 (CI/B-D02-08)
[-RSISI]
[-RSISO]
-RING SHIFT 1 [-RSI]
CRP 4.1-01 (CI/B-DI2-08)
CRP 4.1-01 (CI/B-EI3-18)
-RING SHIFT 2 [-RS2]
CRP 4.1-01 (CI/B-EI3-17)
CRP 4.1-04 (CI/B-G09-12)
CRP 4.1-03 (CI/B-E02-12)
CRP 4.1-03 (CI/B-D02-06)
[-CLK6]
[-RS2SI]
[-RS2SO]
CRP 4.1-03 (CI/B-CII-13)
[-DRSI]
+RING STØP [+RST]
-RING STØP [-RST]
+SYSTEM RING STØP
TP19
CRP 4.1-04 (CI/B-G09-07)
CRP 4.1-03 (CI/B-DII-05)
[-CLK4]
[-CLRCRP]
-SYSTEM RING STØP [-SRST]
RPU 4.0-21 (B2/J1-D0T-02) [-RINGH]
RPU 4.0-21 (B2/J2-D0T-02) [-RINGH]
[-RSTP]
-RING STØP INTERRUPT [-RSIN]
CRP 4.1-04 (CI/B-AI2-19)
CRP 4.0-07 (CI/A-CI2/A-20)
NU (PIC-158)
CRP 4.1-03 (CI/B-CII-07)
[-ERSI]
-REQUEST RING STØP [-RQRS]
CRP 4.0-07 (CI/A-BI3/B-12)
(PIA-12)
CRP 4.0-05 (CI/A-BII/A-13)
[-RINGSTØP]
(PZA-10)
-RING STØP ALL [-RSALL]
-REQUEST RING STØP [+RQRS]
[-DFRS]
CRP 4.1-04 (CI/B-D0T-03)
CRP 4.1-04 (CI/B-D0T-02)
CRP 4.1-04 (CI/B-D0T-01)
TP1
-APPLICATIØN RING STØP [-APRS]
RPU 4.1-21 (B2/J2-D0T-02) [-RIGHI]
CRP 4.1-03 (CI/B-CII-11)
[-DRS2]
+APPLICATIØN RING STØP
TP17
[-APRS]
CRP 4.1-04 (CI/B-D0T-24)
NU (PIC-80)
-ENABLE RING SHIFT 2 [-ERS2]
CRP 4.1-03 (CI/B-CII-05)
NØTES:
1. CHIPS ØN THIS PRINT:
E06 F03 G03
E07 F05 G04
E08 F06 G05
G01 G06
G02 G07
F08
ØNE CØAX PER EACH BASE PRØCESSØR ØN THE RING.
LEVEL 4 DRAWING
CRP CØNTRØL BØARD
RING STØP REGISTERS
ZIF BØARD CI-B
DB-CICRC:CI/B
DEVELOPMENT DIVISION
60461830
A
CRP 4.1-02
III-1-27

LØØP SHIFT CØNTRØL REGISTER

SHIFT REGISTER

SØ REGISTER

HØLD/LØAD/SI REGISTER

EXTERNAL RESET REGISTER

DIAGNØSTIC REGISTER

NØTES:

1. 12151

BIT	D	T	F
0	2	3	4
1	1	6	5
2	20	8	7
3	19	12	11
4	18	14	13
5	17	16	15

2. ØNE C0AX PER EACH BASE PRØCESSØR ØN THE RING.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM CRP CØNTRØL BØARD DIAGNØSTIC RGTR RESET RGTR. SHIFT RGTR HØLD/LØAD RGTR SO/SI RGTR. DB-CIRC:CI/B	ORDER IDENT DWG NO: 60461830	REV: A
DEVELØPMENT DIVISIØN		SHEET: CRP 4.1-03	SIZE: III-1-29

-GENERAL STATUS WØRD SHIFT 1 [-GSWS1]

CRP 4.1-01 (C1/B-D12-05)

12102 DO6/DO6

-STATUS BIT, SPARE [-GSW0] (P1A-17) — NU

-D B HPM ERRØR [-GSW1] (P1A-19) — MEL 4.0-05 (C1/D-F03-13)

-S B HPM ERRØR [-GSW2] (P1A-09) — MEL 4.0-05 (C1/D-F03-16)

-CENTRAL MEM INTF ERRØR [-GSW3] (P2A-17) — NU

GENERAL STATUS WØRD REGISTER

12141 DO7/DO7

12141 DO8/DO8

-APPLICATIØN RING STØP [-APRS] — CRP 4.1-02 (C1/B-G02-12)

-DATA FIFØ RING STØP [-DFRS] — CRP 4.1-02 (C1/B-E06/A-15)

-REQUEST RING STØP [-RQRS] — CRP 4.1-02 (C1/B-E06/A-06)

-RING STØP ALL [-RSALL] — CRP 4.1-02 (C1/B-E06/A-08)

-17Ø CHANNEL PARITY ERRØR [-CHPRTY] (P1B-06) — CRP 4.2-03 (C1/C-A08/B-07)

-MULTIPLE LØST PACKET ERRØR [-MULTILP] (P1A-30) — CRP 4.0-09 (C1/A-G14-11)

-LØST PACKET ERRØR [-LP] (P1A-29) — CRP 4.0-09 (C1/A-G14-07)

-DEADMAN TIMEØUT [-DMT] (P2B-03) — CRP 4.2-03 (C1/C-B12/A-07)

-END FLAG [-ENDFLAG] (P2A-31) — CRP 4.0-09 (C1/A-G14-14)

-DATA FIFØ READY [-DFRDY] (P1A-20) — CRP 4.0-05 (C1/A-C10-11)

-REQUEST STACK READY [-RQSTKRDY] (P1A-23) — CRP 4.0-07 (C1/A-C13-14)

-GENERAL STATUS WØRD SHIFT 1 [-GSWS1] — CRP 4.1-03 (C1/B-E02-16)

-GENERAL STATUS WØRD SHIFT 0 [-GSWS0] — CRP 4.1-03 (C1/B-D02-12)

-CØNTRØL READY 2 [-CTLRDY2] — CRP 4.1-00 (C1/B-B13/B-16)

-CØNTRØL READY 1 [-CTLRDY1] — CRP 4.1-00 (C1/B-B13/B-15)

-END ØF TRANSFER [-EØT] (P2A-35) — CRP 4.0-09 (C1/A-F12/B-11)

END ØF TRANSMISSIØN

12164 CO9/CO9

MUX

-AD3 -AD2 -AD1 -AD0

LØØP ADDRESS

-ADDRESS BIT 4 [-AD4] (P1B-19) — CRP 4.2-03 (C1/C-B06-06)

-ADDRESS BIT 3 [-AD3] (P1B-20) — CRP 4.2-03 (C1/C-B06-08)

-ADDRESS BIT 2 [-AD2] (P1B-17) — CRP 4.2-03 (C1/C-B06-12)

-ADDRESS BIT 1 [-AD1] (P1B-15) — CRP 4.2-03 (C1/C-B06-14)

-ADDRESS BIT 0 [-AD0] (P1B-14) — CRP 4.2-03 (C1/C-B06-16)

-DIAGNØSTIC MØDE [-DIAG] (P1B-13) — CRP 4.2-03 (C1/C-A06-12)

12151 BIØ/BIØ

-CLØCK 16

-AD4 -AD3 -AD2 -AD1 -AD0

-ADDRESS BITS 0-4 [-ADDR] — CRP 4.1-01 (C1/B-D14)

[-DIAG] — CRP 4.1-00 (C1/B-B13/A-20.23)

12101 F10/F10-A/B

-CLØCK [-SYSCLK1] (P1C-109) — CRP 4.2-06 (C1/C-G11/B-05)

12102 EO6/EO6-B/B

12131 F09/F09

-DATA RGTR SHIFT [-DRSHFT] — CRP 4.1-03 (C1/B-F01-14)

-CLEAR EMPTY PACKET [-CEPKT]

-CLEAR CRP [-CLRCRP] — CRP 4.1-03 (C1/B-D11-05)

RGTR

-CLEAR EMPTY PACKET

TP23

-GENERAL STATUS WØRD [-GSW] — CRP 4.1-01 (C1/B-E13-19)

-EMPTY PACKET [-LPKT] (P2A-29) — CRP 4.0-09 (C1/A-G14-07)

12101 C10/C10-B/C

-DISABLE AUTØ INACTIVE [-DAI] — CRP 4.1-03 (C1/B-D11-11)

-READ [-RD] — CRP 4.1-00 (C1/B-B13/A-04)

TP26

12101 C10/C10-A/C

-AD2 -AD1

TP29

12101 C10/C10-C/C

-AD4 -AD3 -AD1

+DIAGNØSTIC MØDE [-NDIAG]

-WRITE 1 [-WRT1] — CRP 4.1-00 (C1/B-B13/A-05)

CRP 4.1-00 (C1/B-B13/A-01)

12101 F10/F10-B/B

TP25

CLØCK FANØUT -(1-8)

12112 G09/G09

12112 G10/G10

TP41

-(9) -(10) -(11) -(12) -(13) -(14) -(15)

-CLØCKS 1-15 [-CLK1-15]

12112 G05/G05

-CLØCK 1 [-CLK1] — CRP 4.1-01 (C1/B-E14-20)

-CLØCK 2 [-CLK2] — CRP 4.1-01 (C1/B-B01-20)

-CLØCK 3 [-CLK3] — CRP 4.1-01 (C1/B-D01-20)

-CLØCK 4 [-CLK4] — CRP 4.1-02 (C1/B-F06-20)

-CLØCK 5 [-CLK5] — CRP 4.1-02 (C1/B-E08-20)

-CLØCK 6 [-CLK6] — CRP 4.1-02 (C1/B-F03-20)

-CLØCK 7 [-CLK7] — CRP 4.1-03 (C1/B-F01-24)

-CLØCK 8 [-CLK8] — CRP 4.1-03 (C1/B-E02-24)

-CLØCK 9 [-CLK9] — CRP 4.1-03 (C1/B-E03-23)

-CLØCK 10 [-CLK10] — CRP 4.1-03 (C1/B-E10-20)

-CLØCK 11 [-CLK11] — CRP 4.1-03 (C1/B-C11-23)

-CLØCK 12 [-CLK12] — CRP 4.1-03 (C1/B-G12-23)

-CLØCK 13 [-CLK13] — CRP 4.1-03 (C1/B-F12-20)

-CLØCK 14 [-CLK14] — CRP 4.1-00 (C1/B-C13-20)

-CLØCK 15 [-CLK15] — CRP 4.1-03 (C1/B-F02-24)

-CLØCK 17 [-CLK17] — CRP 4.1-00 (C1/B-C14/A-20)

12102 CO8/CO8

TP20

TP21

+DATA FIFØ READY [-NDFRDY] — CRP 4.1-00 (C1/B-C12/C-02)

-CLEAR CRPRP [-CLRCPR1] (P1A-13) — CRP 4.0-05 (C1/A-C09-18)

+PACKET READY [-NPKRDY] (P2A-27) — CRP 4.0-09 (C1/A-F13/A-18)

TP22

-PACKET READY [-PKTRDY] — CRP 4.1-00 (C1/B-B11/A-06)

-CLEAR END ØF TRANSFER [-CEØT] (P1B-12) — CRP 4.2-06 (C1/C-B12/B-02)

-DATA FIFØ READY [-DFRD] — CRP 4.1-00 (C1/B-C12/C-05)

+DATA FIFØ READY [-NDFRD] (P1A-31) — CRP 4.0-09 (C1/A-F14/A-04)

-ENABLE CØNTRØL RGTR/DATA RGTR [-ENCR/DR] — CRP 4.1-01 (C1/B-C02-03)

+CØNTRØL RGTR/DATA RGTR [-NCR/DR] — CRP 4.1-01 (C1/B-C02-19)

12151 A12/A12

-RING ADDRESS 4 [-RAD4/AD4] (P1A-24) — CRP 4.0-05 (C1/A-B11/C-02)

+DIAGNØSTIC MØDE [-NDM/NDIAG] (P1A-07) — CRP 4.0-07 (C1/A-A14-02)

-DIAGNØSTIC MØDE [-DM] (P1A-08) — NU

[-LSH1] — CRP 4.1-00 (C1/B-A13-01)

[-LSH] -RING STØP [-RSTP] — CRP 4.1-00 (C1/B-C12/B-11); CRP 4.1-02 (C1/B-G05-12)

+RING STØP [-NRNGS]

-CLØCK 16

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM	CODE IDENT NO.	DRG NO. 60461830 REV A
DEVELOPMENT DIVISION	CRP CØNTRØL BØARD GENERAL STATUS WØRD, CLØCK FANØUT, EØT, LØØP ADDRESS DB-CICRC-C1/B	SHEET CRP 4.1-04	PAGE III-1-31

FRØM CYBER CHANNEL

-DB(0-11)
[-DATA(0-11)]

-CØNTRØL (0-8)

-CØNTRØL (0-6)

-HØLDING RGTR DATA (0-15)
[-HRR(0-15/ID(0-15)]

[-LATCH1]
[-FNCFLL]
[-CR(0-11)]
[-HR(0-11)]
[-LATCH2]
[-CHCLK]
[+NC4CLK]

12/16 BIT CØNVERSIØN NETWØRK

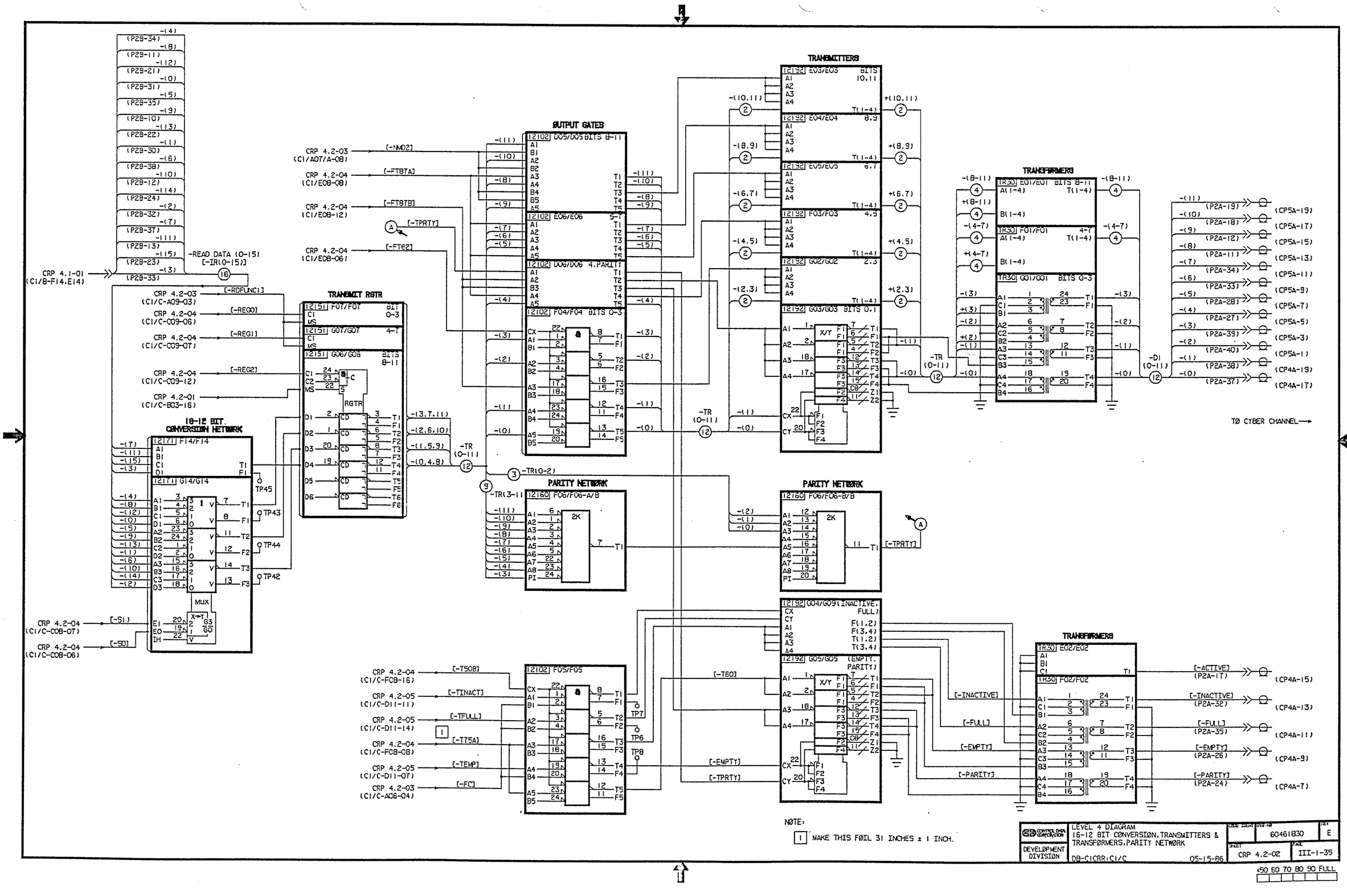
18 BIT HØLDING RGTR

CATCHING RGTR

HØLDING RGTR

RGTR

MUX


TRANSMITTERS
OUTPUT GATES
TRANSMIT RGTR
16-12 BIT CONVERSION NETWORK
PARITY NETWORK
PARITY NETWORK
TRANSFORMERS
TRANSFORMERS
CRP 4.1-01 (C1/B-F14,E14)
-READ DATA (0-15) [-IR(0-15)]
[-RDFUNC1]
CRP 4.2-03 (C1/C-A09-03)
CRP 4.2-04 (C1/C-C09-06)
[-REG0]
CRP 4.2-04 (C1/C-C09-07)
[-REG1]
CRP 4.2-04 (C1/C-C09-12)
[-REG2]
CRP 4.2-01 (C1/C-B03-16)
CRP 4.2-04 (C1/C-C08-07)
[-S1]
CRP 4.2-04 (C1/C-C08-06)
[-S0]
CRP 4.2-03 (C1/A07/A-08)
[-NMO2]
CRP 4.2-04 (C1/E08-08)
[-FT87A]
CRP 4.2-04 (C1/E08-12)
[-FT87B]
[-TPRTY]
CRP 4.2-04 (C1/E08-06)
[-FT62]
-TR (0-11)
-TR10-2
-TR13-11
[-T50B]
[-TINACT]
[-TFULL]
[-T75A]
[-TEMP]
[-FC]
[-T60]
[-EMPTY]
[-TPRTY]
[-INACTIVE]
[-FULL]
[-EMPTY]
[-PARITY]
-DI (0-11)
TØ CYBER CHANNEL
[-ACTIVE] (P2A-17)
[-INACTIVE] (P2A-32)
[-FULL] (P2A-35)
[-EMPTY] (P2A-26)
[-PARITY] (P2A-24)
(CP4A-15)
(CP4A-13)
(CP4A-11)
(CP4A-9)
(CP4A-7)
NØTE:
1 MAKE THIS FØIL 31 INCHES ± 1 INCH.
LEVEL 4 DIAGRAM
16-12 BIT CØNVERSIØN, TRANSMITTERS & TRANSFØRMERS, PARITY NETWØRK
DB-C1CRR:C1/C
05-15-86
60461830
E
CRP 4.2-02
III-1-35

PARITY CHECKER

12160 B07/B07-A/B BITS 4-11

12160 B07/B07-B/B BITS 0-3

MODE DECODE

12170 A07/A07-B/B

12170 A07/A07-A/B

FUNCTION RGTR

12151 A06/A06 BITS 6-11

12151 B06/B06 BITS 0-5

12112 A09/A09

12102 D08/D08-A/B

12102 D08/D08-B/B

12102 B08/B08

12102 C12/C12-B/C

12102 C12/C12-A/C

12131 B12/B12-A/B

12131 A03/A03-B/B

12131 A08/A08-B/C

12102 C11/C11

CRP TIME OUT

12136 B11/B11

12136 B10/B10

12136 B09/B09

12136 A12/A12

12136 A11/A11

12136 A10/A10

16CNTR/SR-4

NOTES:

1. NOT USED UNLESS LONGER DELAY IS NEEDED. IF USED, IT WILL GO TO (C1/C-P1C-158).
2. CAN BE USED TO DISABLE PARITY IF NEED BE DURING CHECKOUT.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM PARITY CHECKER.FUNCTION RGTR. MODE DECODE CRP TIMEOUT	CODE IDENT. DWG NO. 60461830	REV E
DEVELOPMENT DIVISION	DB-C1CRR:C1/C 05-15-86	SHEET CRP 4.2-03	PAGE III-1-37

<50 60 TO 80 90 FULL

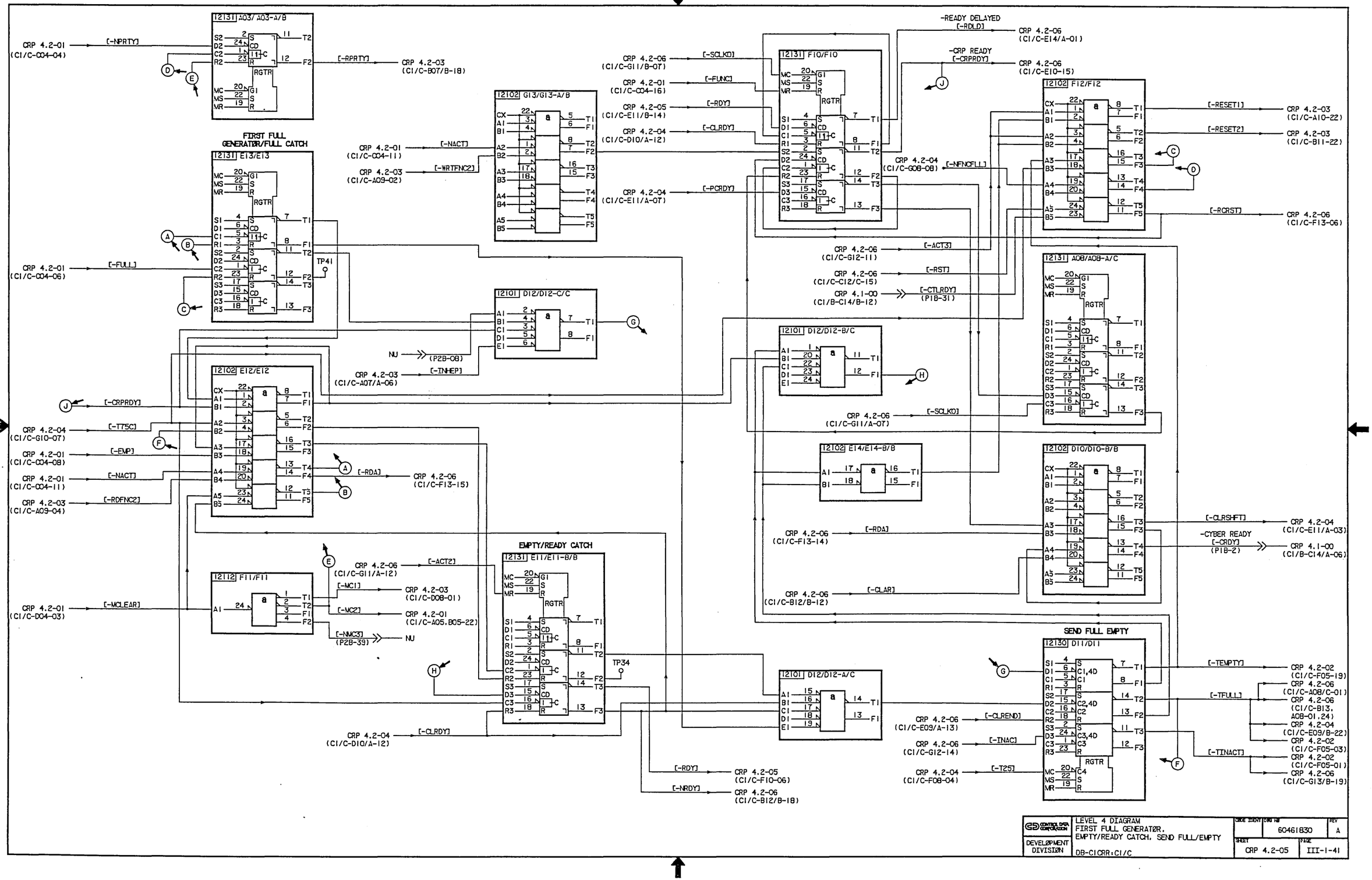
PULSE GENERATOR

CHANNEL CLOCK DISTRIBUTION

CHANNEL CLOCK DISTRIBUTION

NOTE:
1 FOIL LENGTH FROM F08-16 TO F08-20 SHOULD BE 38.2 INCHES ± 1 INCH. ALL OTHER LOCATIONS FOLLOW F08-20.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM	CODE IDENT	DWG NO
	CHANNEL CLOCK DISTRIBUTION		60461830
DEVELOPMENT DIVISION	PULSE GENERATOR ZIF BOARD.	SHEET	PAGE
	DB-C1CRR:C1/C	CRP 4.2-04	III-1-39


12131 A03/A03-A/B
CRP 4.2-01 (C1/C-C04-04)
[-NPRTY]
[-RPRTY]
CRP 4.2-03 (C1/C-B07/B-18)
FIRST FULL GENERATOR/FULL CATCH
12131 E13/E13
CRP 4.2-01 (C1/C-C04-06)
[-FULL]
TP41
12102 G13/G13-A/B
CRP 4.2-01 (C1/C-C04-11)
[-NACT]
CRP 4.2-03 (C1/C-A09-02)
[-WRTFNC2]
12131 F10/F10
CRP 4.2-06 (C1/C-G11/B-07)
[-SCLKD]
CRP 4.2-01 (C1/C-C04-16)
[-FUNC]
CRP 4.2-05 (C1/C-E11/B-14)
[-RDY]
CRP 4.2-04 (C1/C-D10/A-12)
[-CLRDY]
CRP 4.2-04 (C1/C-E11/A-07)
[-PCRDY]
-READY DELAYED
[-RDLD]
CRP 4.2-06 (C1/C-E14/A-01)
-CRP READY
[-CRPRDY]
CRP 4.2-06 (C1/C-E10-15)
CRP 4.2-04 (C1/C-G08-08)
[-NFNCFLL]
12102 F12/F12
[-RESET1]
CRP 4.2-03 (C1/C-A10-22)
[-RESET2]
CRP 4.2-03 (C1/C-B11-22)
[-RCRST]
CRP 4.2-06 (C1/C-F13-06)
CRP 4.2-06 (C1/C-G12-11)
[-ACT3]
CRP 4.2-06 (C1/C-C12/C-15)
[-RST]
CRP 4.1-00 (C1/B-C14/B-12)
[-CTLRDY] (P1B-31)
12131 A08/A08-A/C
12101 D12/D12-C/C
NU (P2B-08)
CRP 4.2-03 (C1/C-A07/A-06)
[-INHEP]
12101 D12/D12-B/C
CRP 4.2-06 (C1/C-G11/A-07)
[-SCLKD]
12102 E12/E12
CRP 4.2-04 (C1/C-G10-07)
[-T75C]
CRP 4.2-01 (C1/C-C04-08)
[-EMP]
CRP 4.2-01 (C1/C-C04-11)
[-NACT]
CRP 4.2-03 (C1/C-A09-04)
[-RDFNC2]
[-RDA]
CRP 4.2-06 (C1/C-F13-15)
12102 E14/E14-B/B
CRP 4.2-06 (C1/C-F13-14)
[-RDA]
12102 D10/D10-B/B
[-CLRSHFT]
CRP 4.2-04 (C1/C-E11/A-03)
-CYBER READY
[-CRDY] (P1B-2)
CRP 4.1-00 (C1/B-C14/A-06)
CRP 4.2-06 (C1/C-B12/B-12)
[-CLAR]
EMPTY/READY CATCH
12131 E11/E11-B/B
12112 F11/F11
CRP 4.2-01 (C1/C-D04-03)
[-MCLEAR]
CRP 4.2-06 (C1/C-G11/A-12)
[-ACT2]
[-MC1]
CRP 4.2-03 (C1/C-D08-01)
[-MC2]
CRP 4.2-01 (C1/C-A05,B05-22)
[-NMC3] (P2B-39)
NU
TP34
12101 D12/D12-A/C
SEND FULL EMPTY
12130 D11/D11
[-TEMPTY]
CRP 4.2-02 (C1/C-F05-19)
CRP 4.2-06 (C1/C-A08/C-01)
[-TFULL]
CRP 4.2-06 (C1/C-B13, A08-01,24)
CRP 4.2-04 (C1/C-E09/B-22)
CRP 4.2-02 (C1/C-F05-03)
[-TINACT]
CRP 4.2-02 (C1/C-F05-01)
CRP 4.2-06 (C1/C-G13/B-19)
CRP 4.2-06 (C1/C-E09/A-13)
[-CLREND]
CRP 4.2-06 (C1/C-G12-14)
[-INAC]
CRP 4.2-04 (C1/C-F08-04)
[-T25]
[-RDY]
CRP 4.2-05 (C1/C-F10-06)
[-NRDY]
CRP 4.2-06 (C1/C-B12/B-18)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
FIRST FULL GENERATOR, EMPTY/READY CATCH, SEND FULL/EMPTY
DB-C1CRR:C1/C
CAGE IDENT
DWG NO
60461830
REV
A
SHEET
CRP 4.2-05
PAGE
III-1-41

CRP 4.2-05 (C1/C-F10-07) [-RDLD]
CRP 4.2-03 (C1/C-A09-18) [-WRTFNC3]
CRP 4.2-03 (C1/C-A09-16) [-RDFNC3]
12102 E14/E14-A/B
[-NRDYD] → CRP 4.2-04 (C1/C-D08-18)
CRP 4.1-04 (C1/B-C10/B-12) [-CEØT] (P1B-12)
CRP 4.2-04 (C1/C-D10/A-11) [-CLKW]
CRP 4.2-05 (C1/C-E11/B-13) [-NRDY]
CRP 4.2-03 (C1/C-A07/A-05) [-NMD1]
CRP 4.2-05 (C1/C-F10-11) [-CRPRDY]
CRP 4.2-04 (C1/C-C10/A-14) [-CLRCRDY]
CRP 4.2-04 (C1/C-C10/B-08) [-TC1]
12131 B12/B12-B/B
12102 C12/C12-C/C
[-RST] → CRP 4.2-05 (C1/C-F12-24)
[-NACT3] (P1B-01) → CRP 4.1-00 (C1/B-A14-19)
[-CLAR] → CRP 4.2-05 (C1/C-D10/B-20)
[-NCRDY] → CRP 4.2-04 (C1/C-D09/B,C-D08-20)
12101 E10/E10-A/C
12102 G13/G13-B/B
CRP 4.2-05 (C1/C-D11-11) [-TINACT]
CRP 4.2-04 (C1/C-F08-16) [-T50B]
12131 A08/A08-C/C
12112 G11/G11-B/B
CLK 4.0-00 (A2-K02/C-33) [-SYSCLK] (P1C-149)
[-SCLK0] → CRP 4.2-03 (C1/C-A03/B-05)
[-SCLK0] → CRP 4.2-05 (C1/C-F10-08)
[-SCLK1] (P1C-141) → CRP 4.1-04 (C1/B-E06/B-20)
[-SCLK2] (P1C-138) → CRP 4.0-08 (C1/A-F11-20,23)
12131 B13/B13
CRP 4.2-01 (C1/C-C04-16) [-FUNC]
CRP 4.2-04 (C1/C-F08-07) [-NT75A]
CRP 4.2-05 (C1/C-D11-14) [TFULL]
CRP 4.2-04 (C1/C-C08-12) [-MN]
12151 B14/B14
12131 F13/F13
CRP 4.2-05 (C1/C-F12-11) [-RCRST]
CRP 4.2-04 (C1/C-E07-08) [-RF13]
CRP 4.2-03 (C1/C-C04-08) [-EMP]
CRP 4.2-05 (C1/C-E12-14) [-RDA]
[-RDA] → CRP 4.2-05 (C1/C-D10/B-18)
12101 E09/E09-A/C
[-CLREND] (P2A-21) → CRP 4.0-09 (C1/A-F14/B-02)
[+CLREND] → CRP 4.2-05 (C1/C-D11-18)
12101 E10/E10-C/C
CRP 4.2-01 (C1/C-C04-14) [-INACT]
CRP 4.2-01 (C1/C-D04-03) [-MCLEAR]
ACTIVE F/F INACTIVE CONDITION
12131 G12/G12
CRP 4.2-01 (C1/C-C04-12) [-ACTIVE]
12112 G11/G11-A/B
TP39
[-CLKA] → CRP 4.2-04 (C1/C-D09/A,C-17,05)
[-NCLKB] (P1C-145) → NU
[-NCLKC] (P1C-142) → NU
[-SCLK0] → CRP 4.2-05 (C1/C-A08/A-16); CRP 4.2-03 (C1/C-A03/B-05)
[-ACT1] → CRP 4.2-04 (C1/C-C08, C09-22)
[-ACT2] → CRP 4.2-04 (C1/C-E11/A-19); CRP 4.2-05 (C1/C-E11/B-19)
12101 E10/E10-B/C
CRP 4.2-03 (C1/C-C12/A-08) [-NDWT]
[-ACT3] → CRP 4.2-05 (C1/C-F12-03)
[-INAC] → CRP 4.2-05 (C1/C-D11-24)

NØTE:
1 THIS FØIL SHØULD BE 14.5 INCHES ± 1 INCH.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM SYSTEM CLØCK, ACTIVE, INACTIVE	CAGE IDENT	DRG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-C1CRR:C1/C	SHEET CRP 4.2-06	PAGE III-1-43

IV. CYBERPLUS BASE PROCESSOR

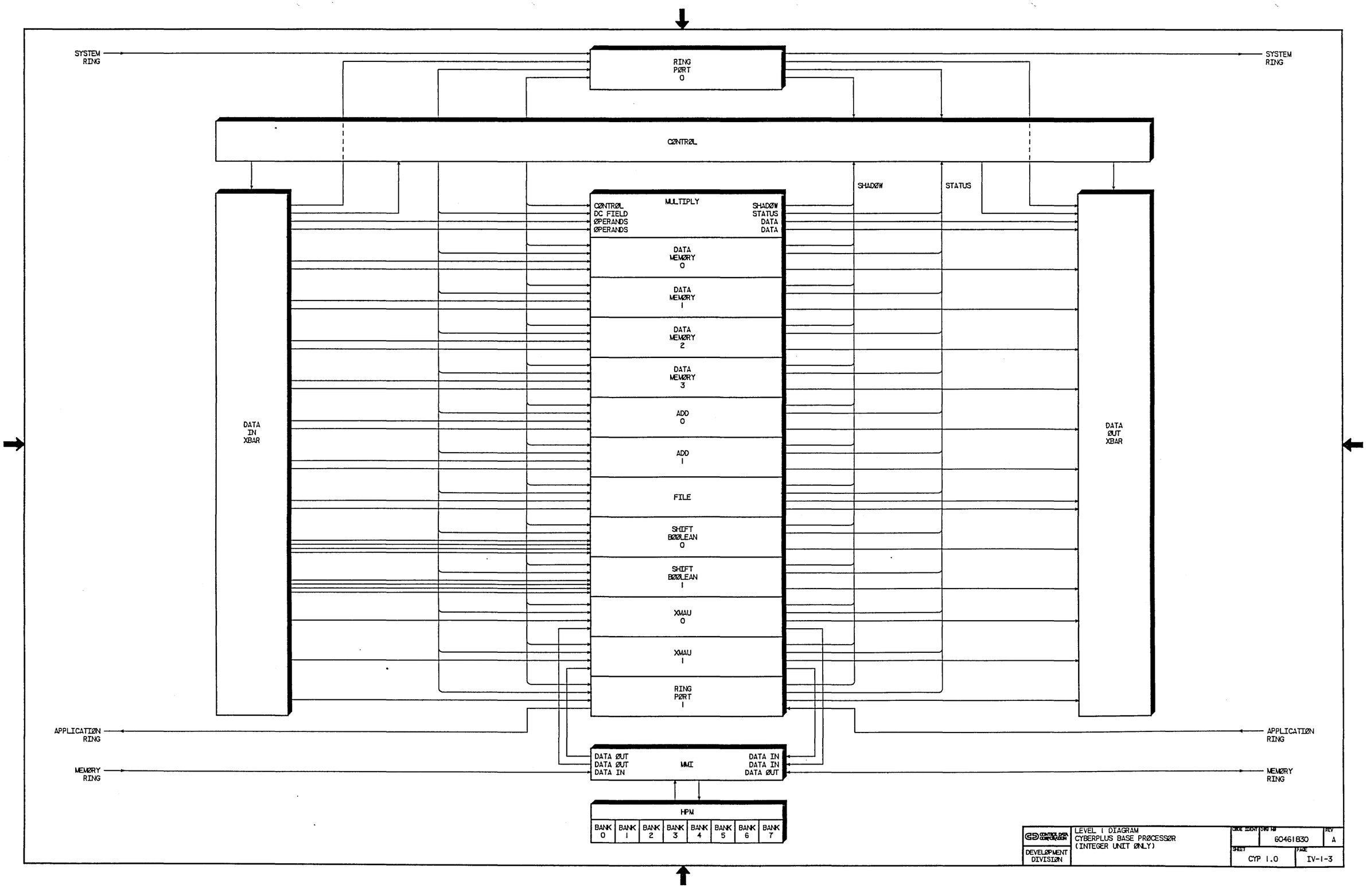
1. CYBERPLUS BASE PROCESSOR (CYP)

SYSTEM FUNCTION

The CYBERPLUS base processor is capable of processing scientific and business data at very high computational rates because of its parallel architecture, its multi-function program control (provided by the 200-bit instruction word), and its cycle time of 21 nanoseconds. The base processor can programmatically be arranged to function simultaneously as one or more pipeline processors by activating several routes through the functional units of the processor. In addition, the base processor can be reconfigured to provide different configurations of pipeline processing by program instruction during the same application.

GENERAL DESCRIPTION

The basic building block of CYBERPLUS is the 16-bit base processor. The processor is made up of a crossbar switch and 15 functional units consisting of one program control unit, nine I/O and memory units, and five integer/boolean units. Each unit has its inputs and outputs connected to the 16-input, 18-output crossbar switch, which is capable of routing each of the crossbar inputs to any or all of the crossbar outputs each clock cycle with minimal conflicts. Each of the functional units can be initiated every clock cycle, which is 21 nanoseconds. The base processor has three types of addressable memories: the 200-bit by 4096-word memory in the control unit, which holds the base processor program instructions; the four independent 16-bit by 4096-word data memory units, which provide temporary storage of variables, intermediate operands, and or results, and the file unit with two independent memories of 16-bit by 16-word file memories used to coordinate timing between functional units. Through the external memory unit, there is access to 256K (or 512K) words of 64-bit high performance memory.


SYSTEM RING
RING PØRT 0
CØNTRØL
SHADØW
STATUS
SYSTEM RING
MULTIPLY
CØNTRØL
DC FIELD ØPERANDS
ØPERANDS
SHADØW
STATUS DATA
DATA
DATA MEMØRY 0
DATA MEMØRY 1
DATA MEMØRY 2
DATA MEMØRY 3
ADD 0
ADD 1
FILE
SHIFT BØØLEAN 0
SHIFT BØØLEAN 1
XMAU 0
XMAU 1
RING PØRT 1
DATA IN XBAR
DATA ØUT XBAR
APPLICATIØN RING
MEMØRY RING
DATA ØUT
DATA ØUT
DATA IN
MMI
DATA IN
DATA IN
DATA ØUT
HPM
BANK 0
BANK 1
BANK 2
BANK 3
BANK 4
BANK 5
BANK 6
BANK 7
APPLICATIØN RING
MEMØRY RING
CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 1 DIAGRAM
CYBERPLUS BASE PRØCESSØR
(INTEGER UNIT ØNLY)
CODE IDENT
DWG NO
60461830
REV
A
SHEET
CYP 1.0
PAGE
IV-1-3

2. INTEGER ADDER (ADD)

SYSTEM FUNCTION

The integer adder unit, which is located in the base processor, performs arithmetic or logical operations on operands taken from the crossbar and returns the results to the crossbar.

GENERAL DESCRIPTION

There are two integer adders in the base processor. Each performs 1's or 2's complement arithmetic operations using 8-bit or 16-bit operands. The two adders can be linked together to perform a single 1's or 2's complement 32-bit operation. Each integer adder also compares the result of an adder operation against the contents of a compare register.

LOCATION

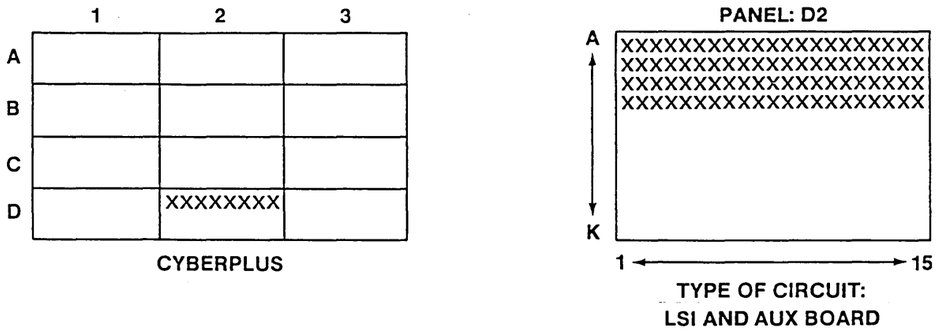


Figure IV-2-1. Location of Integer Adder Unit Logic Circuits

FUNCTIONAL DESCRIPTION

The discussion in the following paragraphs refers to the simplified block diagram of the adder unit (as shown in figure IV-2-2 and the level 2 diagram ADD 2.0). The control register receives the 12-bit operation code from the 16-bit dynamic control field of the instruction word. The bits of the operation code determine what function the adder will perform.

The A and B operand registers receive data from the crossbar when enabled by the A and B clocks, respectively. The A and B clocks are set by the program into the clock control field of the instruction word, bits 19 through 22. Bits 19 and 21, when set, gate the A operands for adder 0 and 1, respectively. Bits 20 and 22, when set, gate the B operands for adder 0 and 1, respectively. The clock bits gate the data at time 0 of clock cycle one when they are set. If the clock bits are clear, the contents of the operand registers are not changed.

The adder network performs all arithmetic instructions in either 1's or 2's complement mode on 8-, 16-, or 32-bit operands: all increment and decrement instructions in 2's complement mode only on 8-, 16-, or 32-bit operands; and logical instructions on 8-, 16-, 32-bit operands. All results from the adder network are available from the output register at time 0 of clock cycle two, and from the output of the crossbar or the comparison circuit at time 0 of the fourth clock cycle.

The outputs of the status register are available as follows: at the start of cycle two, the negative sign bit, 8-bits not zero, carry and overflow status bits are available, when applicable. At the start of the fourth cycle, the compared-equal or compared-greater-than status bits are available.

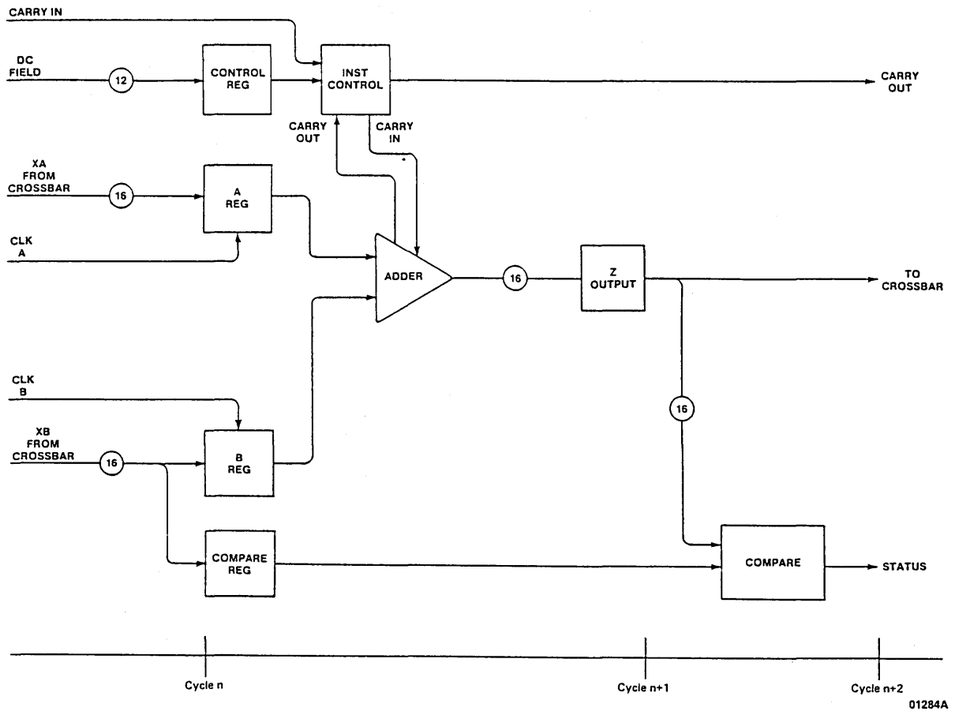


Figure IV-2-2. Integer Adder Unit Block Diagram

TIMING

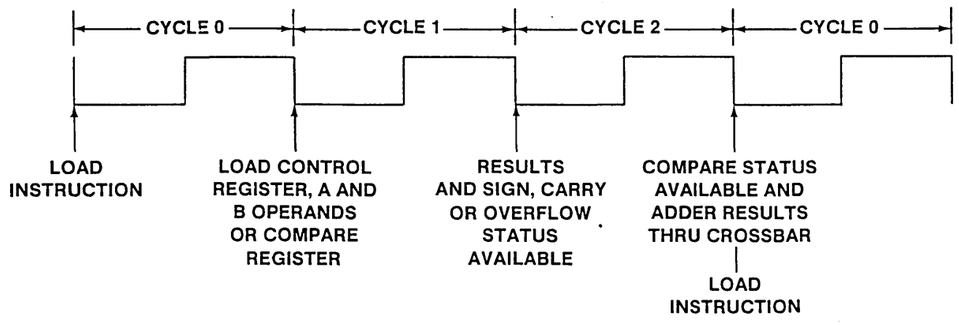
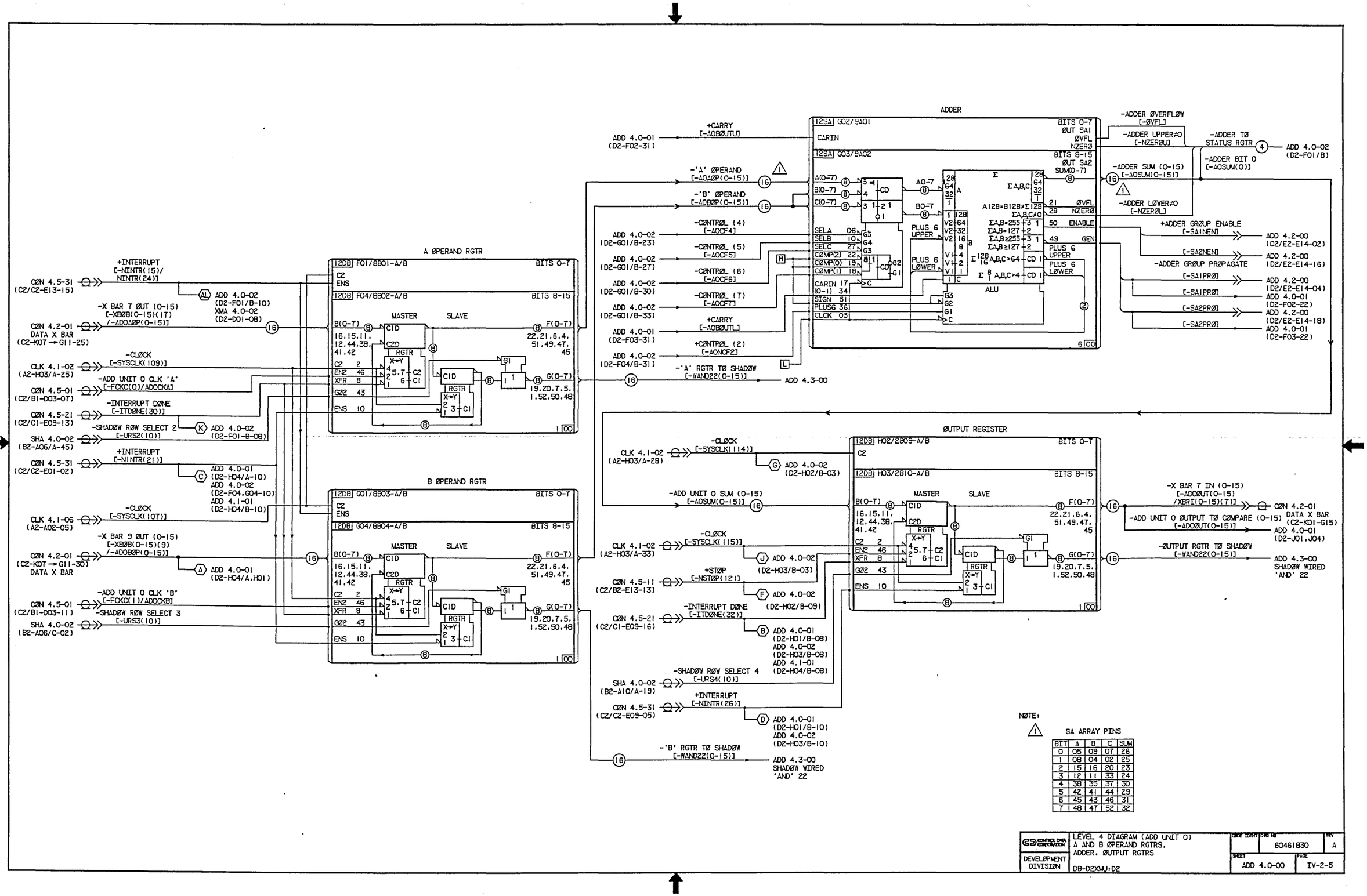
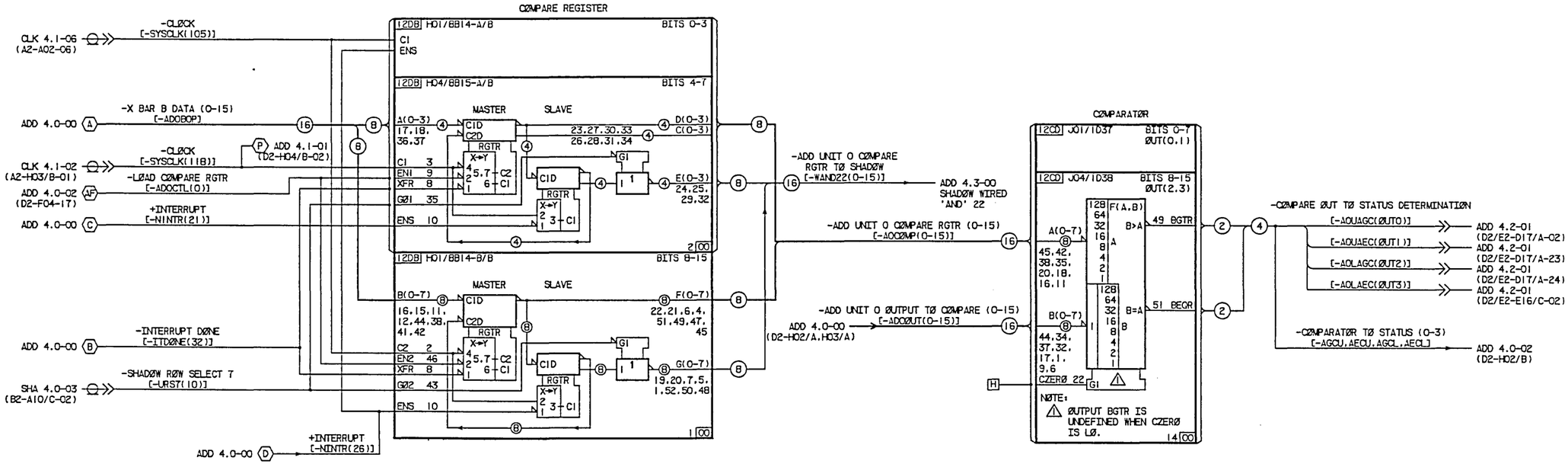

CYCLE 0
CYCLE 1
CYCLE 2
CYCLE 0
LOAD INSTRUCTION
LOAD CONTROL REGISTER, A AND B OPERANDS OR COMPARE REGISTER
RESULTS AND SIGN, CARRY OR OVERFLOW STATUS AVAILABLE
COMPARE STATUS AVAILABLE AND ADDER RESULTS THRU CROSSBAR
LOAD INSTRUCTION

Figure IV-2-3. Integer Adder Unit Instructions Timing

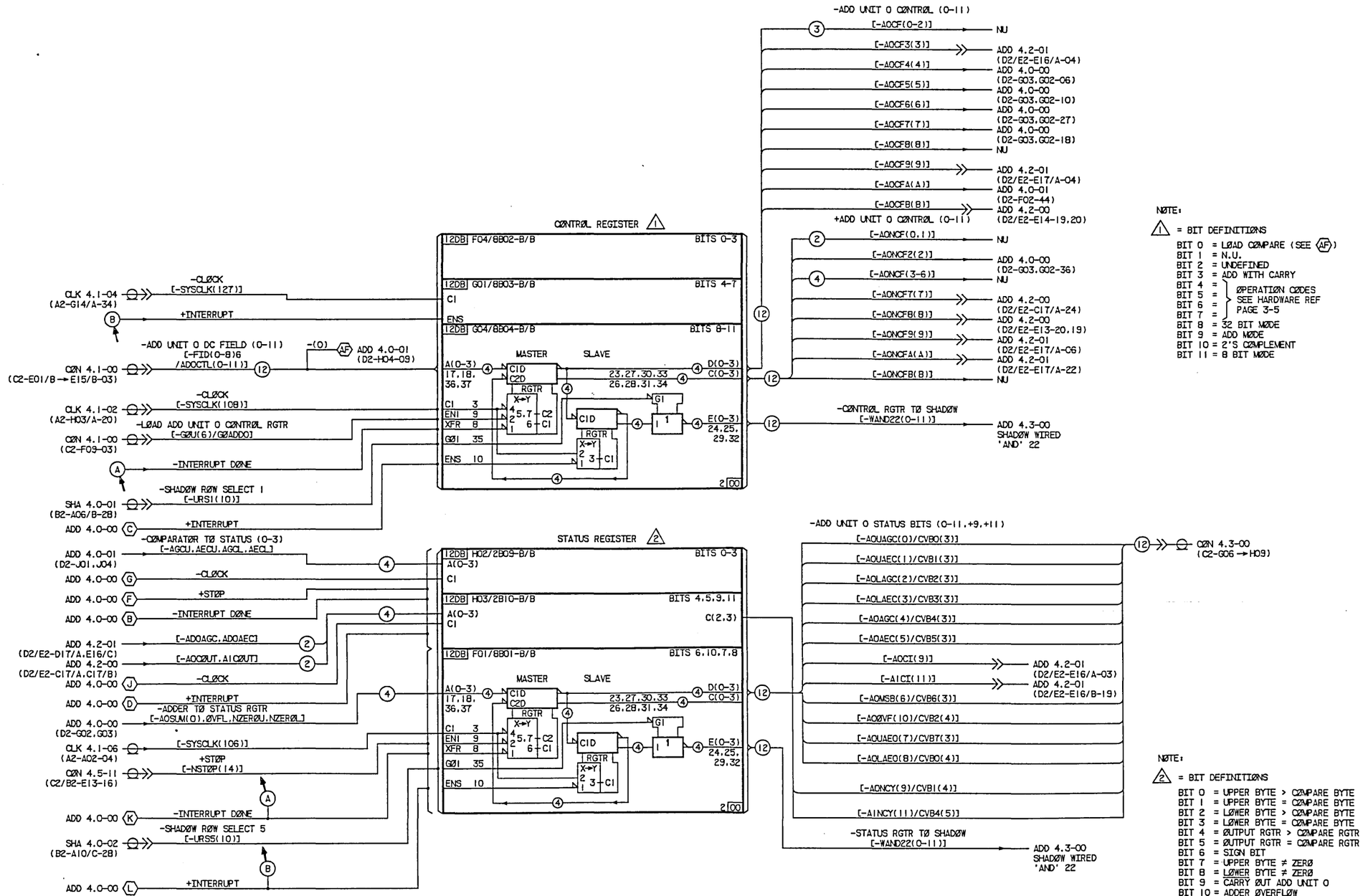
C0N 2.0 DATA X BAR
-X BAR 'B' DATA
C0N 2.0 CL0CK BITS FAN0UT
-'B' CLK
'B' 0PERAND RGTR ADD 4.0-00
-SHAD0W
C0N 2.0 DATA X BAR
-X BAR 'A' DATA
C0N 2.0 CL0CK BITS FAN0UT
-'A' CLK
'A' 0PERAND RGTR ADD 4.0-00
-SHAD0W
C0N 2.0 DC FIELDS FAN0UT
-DYNAMIC C0NTR0L
C0N 2.0 CL0CK BITS FAN0UT
-L0AD C0NTR0L
C0NTR0L RGTR ADD 4.0-02
-SHAD0W
C0MPARE RGTR ADD 4.0-01
-SHAD0W
ADDER ADD 4.0-00
ADD CARRY NETW0RK ADD 4.0-01
C0MPARAT0R ADD 4.0-01
SHAD0W WIRED 'AND' 22 ⚠1 ADD 4.3-00
C0N 2.0
0UTPUT RGTR ADD 4.0-00
-ADD UNIT 0 0UTPUT T0 X BAR
C0N 2.0 DATA X BAR
SHAD0W
STATUS RGTR ADD 4.0-02
-ADD UNIT 0 STATUS T0 C0NDITI0N VECT0R
C0N 2.0 C0NDITI0N VECT0R
-SHAD0W
ADD UNIT 0
AUX BRD E2
CARRY/STATUS DETERMINATI0N ADD 4.2-00
CARRY/STATUS DETERMINATI0N ADD 4.2-01
ADD UNIT 1
C0N 2.0 DC FIELDS FAN0UT
-DYNAMIC C0NTR0L
C0N 2.0 CL0CK BITS FAN0UT
-L0AD C0NTR0L
C0NTR0L RGTR ADD 4.1-02
-SHAD0W
C0N 2.0 DATA X BAR
-X BAR 'A' DATA
C0N 2.0 CL0CK BITS FAN0UT
-'A' CLK
'A' 0PERAND RGTR ADD 4.1-00
-SHAD0W
C0N 2.0 DATA X BAR
-X BAR 'B' DATA
C0N 2.0 CL0CK BITS FAN0UT
-'B' CLK
'B' 0PERAND RGTR ADD 4.1-00
-SHAD0W
ADD CARRY NETW0RK ADD 4.1-01
ADDER ADD 4.1-00
C0MPARE RGTR ADD 4.1-01
-SHAD0W
C0MPARAT0R ADD 4.1-01
SHAD0W WIRED 'AND' 23 ⚠1 ADD 4.3-00
C0N 2.0
STATUS RGTR ADD 4.1-02
-ADD UNIT 1 STATUS T0 C0NDITI0N VECT0R
C0N 2.0 C0NDITI0N VECT0R
-SHAD0W
0UTPUT RGTR ADD 4.1-00
-ADD UNIT 1 0UTPUT T0 X BAR
C0N 2.0 DATA X BAR
-SHAD0W
ADD UNIT 1
N0TE:
⚠1 SHAD0W RGTR AND WIRED 'AND' DUPLICATED 0N SHA 2.0.

CONTROL DATA CORPORATION	LEVEL 2 DIAGRAM ADD UNIT 0 AND 1	CODE IDENT / DWG NO	REV
		60461830	A
DEVELOPMENT DIVISION		SHEET ADD 2.0	PAGE IV-2-3


A ØPERAND RGTR
B ØPERAND RGTR
ADDER
ØUTPUT REGISTER
ALU
MASTER
SLAVE
RGTR
+INTERRUPT [-NINTR(15)/ NINTR(24)]
-X BAR 7 ØUT (0-15) [-XBØB(0-15)(17) /-ADOA2P(0-15)]
-CLØCK [-SYSCLK(109)]
-ADD UNIT 0 CLK 'A' [-FCKC(0)/ADOCKA]
-INTERRUPT DØNE [-ITDØNE(30)]
-SHADØW RØW SELECT 2 [-URS2(10)]
+INTERRUPT [-NINTR(21)]
-CLØCK [-SYSCLK(107)]
-X BAR 9 ØUT (0-15) [-XBØB(0-15)(9) /-ADOB2P(0-15)]
-ADD UNIT 0 CLK 'B' [-FCKC(1)/ADOCKB]
-SHADØW RØW SELECT 3 [-URS3(10)]
+CARRY [-AOBØUTU]
-'A' ØPERAND [-AOA2P(0-15)]
-'B' ØPERAND [-AOB2P(0-15)]
-CØNTRØL (4) [-AOCF4]
-CØNTRØL (5) [-AOCF5]
-CØNTRØL (6) [-AOCF6]
-CØNTRØL (7) [-AOCF7]
+CARRY [-AOBØUTL]
+CØNTRØL (2) [-AONCF2]
-'A' RGTR TØ SHADØW [-WAND22(0-15)]
-ADDER ØVERFLØW [-ØVFL]
-ADDER UPPER≠0 [-NZERØU]
-ADDER LØWER≠0 [-NZERØL]
-ADDER SUM (0-15) [-AOSUM(0-15)]
-ADDER BIT 0 [-AOSUM(0)]
-ADDER TØ STATUS RGTR
+ADDER GRØUP ENABLE [-SAINEN]
-ADDER GRØUP PRØPAGATE [-SAIPRØ]
[-SA2NEN]
[-SA1PRØ]
[-SA2PRØ]
-CLØCK [-SYSCLK(114)]
-ADD UNIT 0 SUM (0-15) [-AOSUM(0-15)]
-CLØCK [-SYSCLK(115)]
+STØP [-NSTØP(12)]
-INTERRUPT DØNE [-ITDØNE(32)]
-SHADØW RØW SELECT 4 [-URS4(10)]
+INTERRUPT [-NINTR(26)]
-'B' RGTR TØ SHADØW [-WAND22(0-15)]
-X BAR 7 IN (0-15) [-ADOØUT(0-15) /XBRI(0-15)(7)]
-ADD UNIT 0 ØUTPUT TØ CØMPARE (0-15) [-ADOØUT(0-15)]
-ØUTPUT RGTR TØ SHADØW [-WAND22(0-15)]
ADD 4.0-02 (D2-F01/B-10) XMA 4.0-02 (D2-D01-08)
ADD 4.0-02 (D2-F01-B-08)
ADD 4.0-01 (D2-H04/A-10) ADD 4.0-02 (D2-F04,G04-10) ADD 4.1-01 (D2-H04/B-10)
ADD 4.0-01 (D2-H04/A,H01)
ADD 4.0-02 (D2-H02/B-03)
ADD 4.0-02 (D2-H03/B-03)
ADD 4.0-02 (D2-H02/B-09)
ADD 4.0-01 (D2-H01/B-08) ADD 4.0-02 (D2-H03/B-08) ADD 4.1-01 (D2-H04/B-08)
ADD 4.0-01 (D2-H01/B-10) ADD 4.0-02 (D2-H03/B-10)
ADD 4.3-00 SHADØW WIRED 'AND' 22
ADD 4.2-00 (D2/E2-E14-02)
ADD 4.2-00 (D2/E2-E14-16)
ADD 4.2-00 (D2/E2-E14-04)
ADD 4.0-01 (D2-F02-22)
ADD 4.2-00 (D2/E2-E14-18)
ADD 4.0-01 (D2-F03-22)
ADD 4.0-02 (D2-F01/B)
ADD 4.0-01 (D2-J01,J04)
ADD 4.3-00 SHADØW WIRED 'AND' 22
ADD 4.3-00
CØN 4.2-01 DATA X BAR (C2-K01-G15)
CØN 4.5-31 (C2/C2-E13-15)
CØN 4.2-01 DATA X BAR (C2-K07→G11-25)
CLK 4.1-02 (A2-H03/A-25)
CØN 4.5-01 (C2/B1-D03-07)
CØN 4.5-21 (C2/C1-E09-13)
SHA 4.0-02 (B2-A06/A-45)
CØN 4.5-31 (C2/C2-E01-02)
CLK 4.1-06 (A2-A02-05)
CØN 4.2-01 (C2-K07→G11-30) DATA X BAR
CØN 4.5-01 (C2/B1-D03-11)
SHA 4.0-02 (B2-A06/C-02)
ADD 4.0-01 (D2-F02-31)
ADD 4.0-02 (D2-G01/B-23)
ADD 4.0-02 (D2-G01/B-27)
ADD 4.0-02 (D2-G01/B-30)
ADD 4.0-02 (D2-G01/B-33)
ADD 4.0-01 (D2-F03-31)
ADD 4.0-02 (D2-F04/B-31)
CLK 4.1-02 (A2-H03/A-28)
CLK 4.1-02 (A2-H03/A-33)
CØN 4.5-11 (C2/B2-E13-13)
CØN 4.5-21 (C2/C1-E09-16)
SHA 4.0-02 (B2-A10/A-19)
CØN 4.5-31 (C2/C2-E09-05)
CØN 4.2-01 DATA X BAR (C2-K01→G15)
12DB F01/8B01-A/B
12DB F04/8B02-A/B
12DB G01/8B03-A/B
12DB G04/8B04-A/B
12SA G02/9A01
12SA G03/9A02
12DB H02/2B09-A/B
12DB H03/2B10-A/B
BITS 0-7
BITS 8-15
C2
ENS
EN2
XFR
G02
SELA
SELB
SELC
CØMP(2)
CØMP(0)
CØMP(1)
CARIN
SIGN
PLUS6
CLCK
BITS 0-7 ØUT SA1 ØVFL NZERØ
BITS 8-15 ØUT SA2 SUM(0-7)
A0-7
B0-7
PLUS 6 UPPER
PLUS 6 LØWER
ENABLE
GEN
NOTE:
SA ARRAY PINS
BIT A B C SUM
0 05 09 07 26
1 08 04 02 25
2 15 16 20 23
3 12 11 33 24
4 38 35 37 30
5 42 41 44 29
6 45 43 46 31
7 48 47 52 32
LEVEL 4 DIAGRAM (ADD UNIT 0)
A AND B ØPERAND RGTRS, ADDER, ØUTPUT RGTRS
DB-D2XMU:D2
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
60461830
REV A
SHEET ADD 4.0-00
SIZE IV-2-5



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	LEVEL 4 DIAGRAM (ADD UNIT 0) ADDER CARRY NETWØRK, COMPARE REGISTER, COMPARATØR DB-D2XMU;D2	CODE IDENT / DWG NO: 60461830	REV: A
		SHEET: ADD 4.0-01	PAGE: IV-2-7



NØTE:

△1 = BIT DEFINITIØNS

BIT 0 = LØAD CØMPARE (SEE AF)
BIT 1 = N.U.
BIT 2 = UNDEFINED
BIT 3 = ADD WITH CARRY
BIT 4 = } ØPERATIØN CØDES
BIT 5 = } SEE HARDWARE REF
BIT 6 = } PAGE 3-5
BIT 7 = }
BIT 8 = 32 BIT MØDE
BIT 9 = ADD MØDE
BIT 10 = 2'S CØMPLEMENT
BIT 11 = 8 BIT MØDE

NØTE:

△2 = BIT DEFINITIØNS

BIT 0 = UPPER BYTE > CØMPARE BYTE
BIT 1 = UPPER BYTE = CØMPARE BYTE
BIT 2 = LØWER BYTE > CØMPARE BYTE
BIT 3 = LØWER BYTE = CØMPARE BYTE
BIT 4 = ØUTPUT RGTR > CØMPARE RGTR
BIT 5 = ØUTPUT RGTR = CØMPARE RGTR
BIT 6 = SIGN BIT
BIT 7 = UPPER BYTE ≠ ZERØ
BIT 8 = LØWER BYTE ≠ ZERØ
BIT 9 = CARRY ØUT ADD UNIT 0
BIT 10 = ADDER ØVERFLØW
BIT 11 = CARRY ØUT ADD UNIT 1

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM (ADD UNIT 0)
CØNTRØL RGTR, STATUS RGTR

DB-D2XMU.D2

CODE IDENT | DWG NO 60461830 | REV A
SHEET ADD 4.0-02 | PAGE IV-2-9

A ØPERAND RGTR

B ØPERAND RGTR

ADDER

ØUTPUT REGISTER

ALU

MASTER SLAVE

RGTR

+INTERRUPT [-NINTR(25)]

-X BAR 'A' DATA [-XBØB(0-15)(10)/ -ADIAØP(0-15)]

-CLØCK [-SYSCLK(113)]

-ADD UNIT 1 CLK 'A' [-FCKC(2)/-ADICKA]

-INTERRUPT DØNE [-ITDØNE(31)]

-SHADØW RØW SELECT 2 [-URS2(11)]

+INTERRUPT [-NINTR(23)]

-CLØCK [-SYSCLK(111)]

-X BAR 'B' DATA [-XBØB(0-15)(8)/ -ADIBØP(0-15)]

-ADD UNIT 1 CKL 'B' [-FCKC(3)/-ADICKB]

-SHADØW RØW SELECT 3 [-URS3(11)]

+CARRY UPPER [-AIBØUTU]

'A' ØPERAND [-AIAOP(0-15)]

'B' ØPERAND [-AIBOP(0-15)]

-CØNTRØL (4) [-AICF4]

-CØNTRØL (5) [-AICF5]

-CØNTRØL (6) [-AICF6]

-CØNTRØL (7) [-AICF7]

+CARRY LØWER [-AIBØUTL]

+CØNTRØL (2) [-AINCF2]

-ADDER ØVERFLØW [-ØVFL]

-ADDER UPPER≠0 [-NZERØU]

-ADDER TØ STATUS RGTR

-ADDER BIT 0 [-AISUM(0)]

-ADDER SUN (0-15) [-AISUM(0-15)]

-ADDER LØWER≠0 [-NZERØL]

+GRØUP ENABLES [-SA3NEN(0-7)] [-SA4NEN(8-15)]

-GRØUP GENERATES [-SA3PRØ(0-7)] [-SA4PRØ(8-15)] [-SA4PRØ(8-15)]

-'A' RGTR TØ SHADØW [-WAND23(0-15)]

-'B' RGTR TØ SHADØW [-WAND23(0-15)]

-ADD UNIT 1 SUM (0-15) [-AISUM(0-15)]

-CLØCK [-SYSCLK(116)]

-CLØCK [-SYSCLK(117)]

+STØP [-NSTØP(13)]

-INTERRUPT DØNE [-ITDØNE(33)]

-SHADØW RØW SELECT 4 [-URS4(11)]

-X BAR 8 IN (0-15) [-ADIØUT(0-15)/ -XBRI(0-15)(8)]

-ADD UNIT 1 ØUTPUT TØ CØMPARATØR

-ØUTPUT RGTR TØ SHADØW [-WAND23(0-15)]

NØTE:

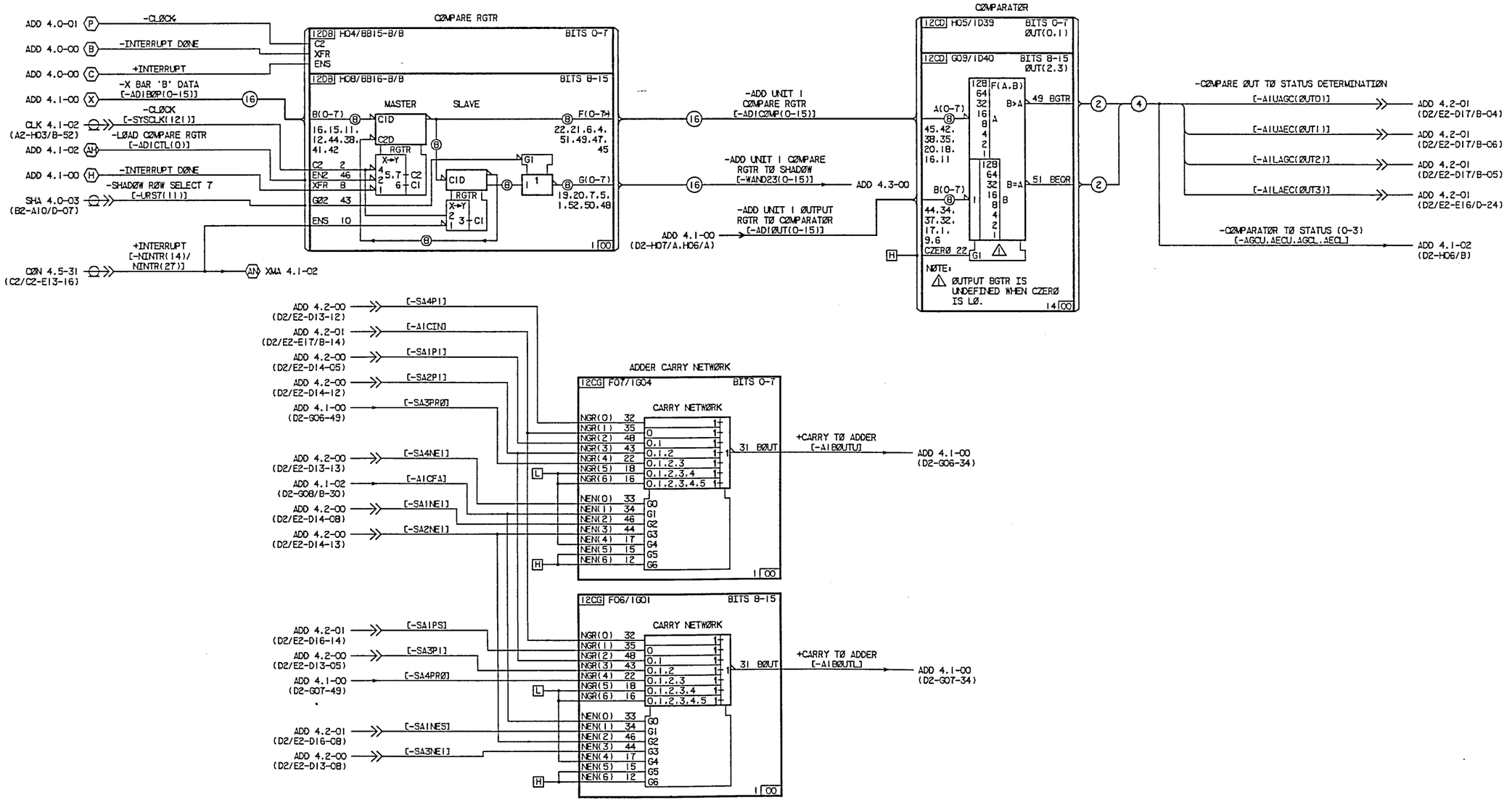
1. SA ARRAY PINS

BIT	A	B	C	SUM
0	05	09	07	26
1	08	04	02	25
2	15	16	20	23
3	12	11	33	24
4	38	35	37	30
5	42	41	44	29
6	45	43	46	31
7	48	47	52	32

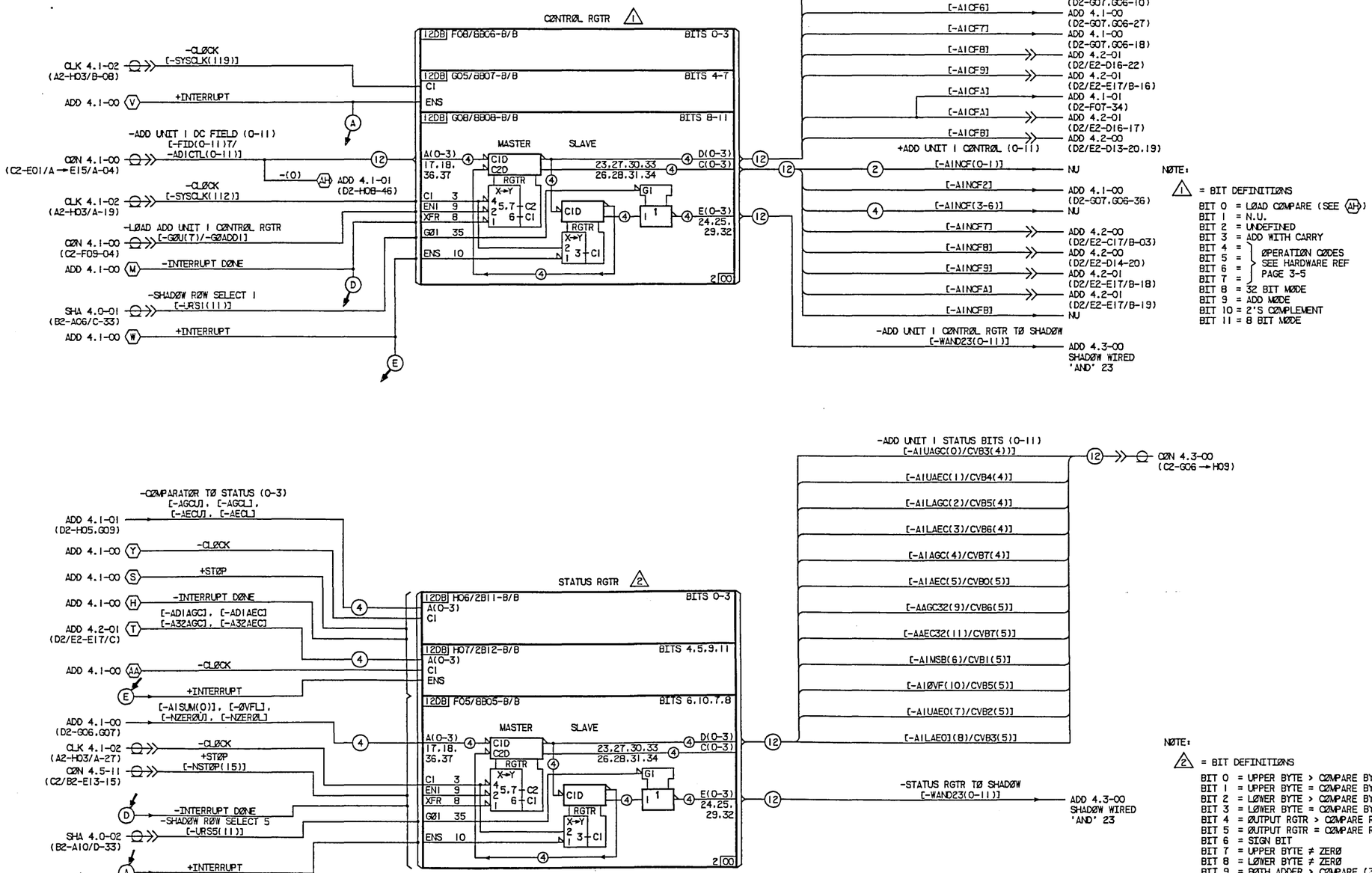
LEVEL 4 DIAGRAM (ADD UNIT 1)
A AND B ØPERAND RGTRS.
ADDER, ØUTPUT RGTR
DB-D2XMU-D2

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

CODE IDENT 60461830 REV A
SHEET ADD 4.1-00 PAGE IV-2-11



CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM (ADD UNIT 1) ADDER CARRY NETWØRK, C2MPARE REGISTER, C2MPARATØR	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-D2XMU:D2	SHEET ADD 4.1-01	PAGE IV-2-13



CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM (ADD UNIT I) CØNTRØL RGTR, STATUS RGTR	CODE IDENT	DRG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-D2XMU-D2	SHEET ADD 4.1-02	PAGE IV-2-15

12135 D14/D14

-ADD UNIT 1 CARRY NET
[-SA1NE1] (11-16) (D2-E04-42) → ADD 4.1-01 (D2-F07-46)
[-SA1P1] (11-07) (D2-E04-33) → ADD 4.1-01 (D2-F07-48)
[-SA2NE1] (11-10) (D2-E04-36) → ADD 4.1-01 (D2-F07-44)
[-SA2P1] (11-17) (D2-E04-43) → ADD 4.1-01 (D2-F07-43)

ADD 4.2-01 (D2/E2-D16-01)
ADD 4.2-01 (D2/EE-D16-03)

ADD 4.1-02 (D2-G08/B-26) → +ADD UNIT 1 CONTROL (8) [-A1NCF8] (11-03) (D2-E04-29)

-ADD UNIT 0 PROPAGATE'S AND + ENABLES

12135 E14/E14

ADD 4.0-00 (D2-G02-50) → [-SA1NEN] (11-06) (D2-E04-32)
ADD 4.0-00 (D2-G02-49) → [-SA1PRØ] (11-08) (D2-E04-34)
ADD 4.0-00 (D2-G03-50) → [-SA2NEN] (11-05) (D2-E04-31)
ADD 4.0-00 (D2-G03-49) → [-SA2PRØ] (11-04) (D2-E04-30)

-ADD UNIT 0 CONTROL (11)
ADD 4.0-02 (D2-G04/B-33) → [-A0CF8] (11-01) (D2-E04-27)

-ADD UNIT 0 CARRY NET
[-SA1NE0] (11-21) (D2-E04-47) → ADD 4.0-01 (D2-F03-44)
[-SA1P0] (11-09) (D2-E04-35) → ADD 4.0-01 (D2-F03-43)
[-SA2NE0] (11-15) (D2-E04-41) → ADD 4.0-01 (D2-F02-33)
[-SA2P0] (11-13) (D2-E04-45) → ADD 4.0-01 (D2-F02-32)

ADD 4.0-02 (D2-G01/B-34) → +ADD UNIT 0 CONTROL (7) [-A0NCF7] (13-07) (D2-E02-33)

12107 C17/C17- A/B

-ADD UNIT 0 CARRY OUT [-A0C2OUT] (12-24) (D2-E03-50) → [-A0C2OUT], [-A1C2OUT] → 24.26 ADD 4.0-02 (D2-H03/B-36.37)

12107 C17/C17- B/B

ADD 4.1-02 (D2-G05/B-34) → +ADD UNIT 1 CONTROL (7) [-A1NCF7] (13-22) (D2-E02-48)

-ADD UNIT 1 CARRY OUT [-A1C2OUT] (12-06) (D2-E03-32)

12118 E15/E15

ADD 4.2-01 (D2/E2-E17/A-08) → [-AXCIN]

TP89

12135 E13/E13

ADD 4.0-02 (D2-G04/B-26) → +ADD UNIT 0 CONTROL (8) [-A0NCF8] (11-26) (D2-E04-52)

-ADD UNIT 1 PROPAGATES AND + ENABLES

ADD 4.1-00 (D2-G06-50) → [-SA3NEN] (10-03) (D2-E05-29)
ADD 4.1-00 (D2-G06-49) → [-SA3PRØ] (10-08) (D2-E05-34)
ADD 4.1-00 (D2-G07-50) → [-SA4NEN] (10-07) (D2-E05-33)
ADD 4.1-00 (D2-G07-49) → [-SA4PRØ] (10-01) (D2-E05-27)

-ADD UNIT 0 CARRY ACT
[-SA3NE0] (10-19) (D2-E05-45) → ADD 4.0-01 (D2-F02-34)
[-SA3P0] (10-10) (D2-E05-36) → ADD 4.0-01 (D2-F02-35)
[-SA4NE0] (10-16) (D2-E05-42) → ADD 4.0-01 (D2-F02-46)
[-SA4P0] (10-21) (D2-E05-47) → ADD 4.0-01 (D2-F02-48)

12118 D15/D15

ADD 4.2-01 (D2/E2-E17/B-13) → [-AYCIN]

TP87

12135 D13/D13

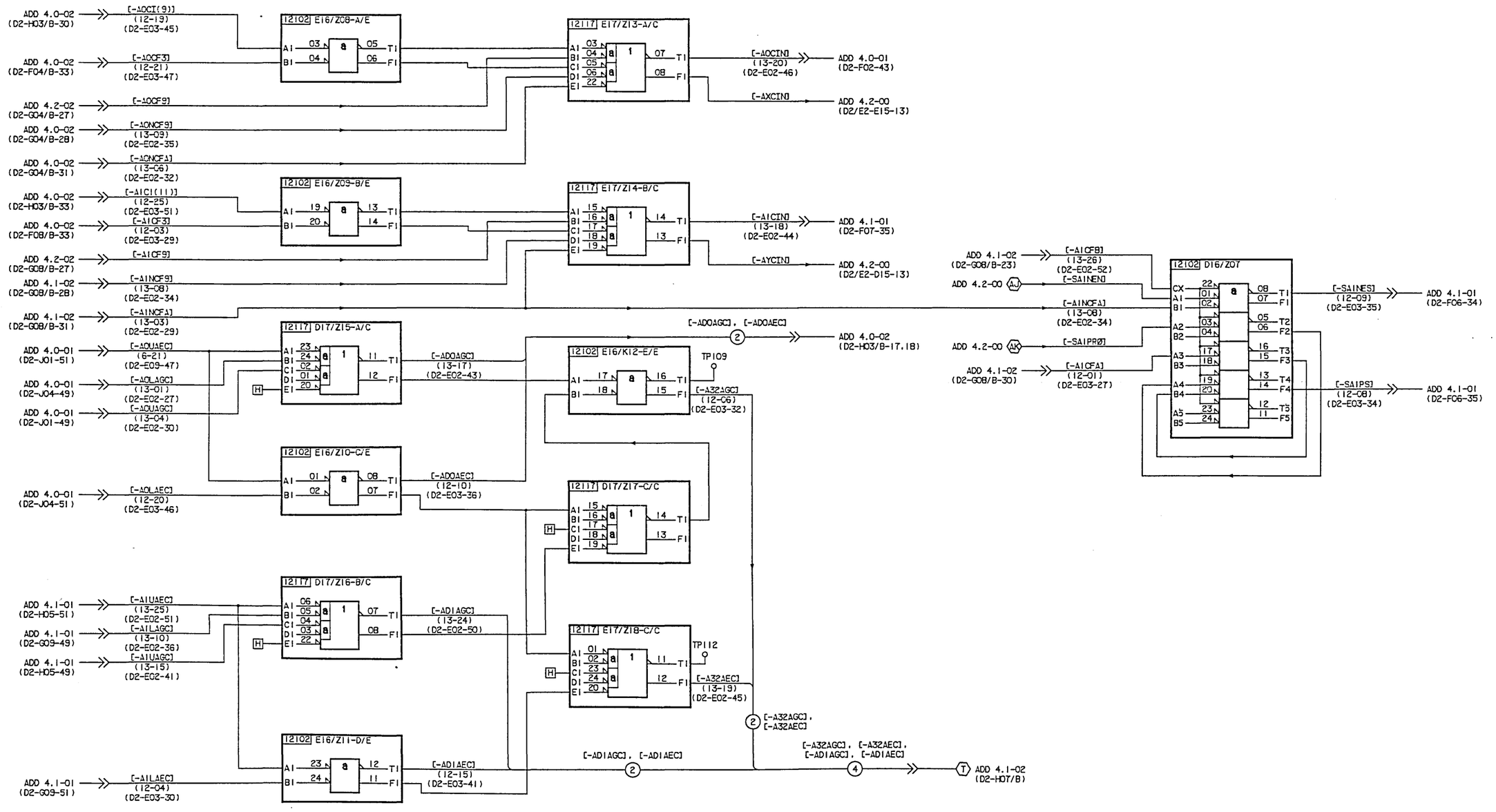
ADD 4.1-02 (D2-G08/B-33) → -ADD UNIT 1 CONTROL (11) [-A1CF8] (10-02) (D2-E05-28)

-ADD UNIT 1 CARRY NET
[-SA3NE1] (10-20) (D2-E05-46) → ADD 4.1-01 (D2-F06-44)
[-SA3P1] (10-09) (D2-E05-35) → ADD 4.1-01 (D2-F06-43)
[-SA4NE1] (10-15) (D2-E05-41) → ADD 4.1-01 (D2-F07-33)
[-SA4P1] (10-17) (D2-E05-43) → ADD 4.1-01 (D2-F07-32)

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM (ADD UNIT 0 AND 1)
CARRY DETERMINATION/STATUS DETERMINATION (AUXILIARY BOARD)
DB-D2XMA;D2/E2

DRAWING NUMBER 60461830 REV A
SHEET ADD 4.2-00 PAGE IV-2-17



CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM (ADD UNIT 0 AND 1) STATUS DETERMINATION/CARRY DETERMINATION (AUXILIARY BOARD)	CODE IDENT / DWG NO: 60461830	REV: A
DEVELOPMENT DIVISION	DB-D2XMA:D2/E2	SHEET: ADD 4.2-01	PAGE: IV-2-19

SHADØW WIRED 'AND' 22

-A ØPERAND RGTR TØ SHADØW (0-15) [-WAND22(0-15)]

ADD 4.0-00 A ØPERAND (D2-F01/A,F04/A)

16

a 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

-ADD UNIT 0 TØ SHADØW (0-15) [-WAND22(0-15)] 16 → C2N 4.4-01 SHADØW WIRED 'AND' 22

-B ØPERAND RGTR TØ SHADØW (0-15) [-WAND22(0-15)] 16
ADD 4.0-00 B ØPERAND (D2-G01/A,G04/A)

-ØUTPUT RGTR TØ SHADØW (0-15) [-WAND22(0-15)] 16
ADD 4.0-00 ØUTPUT RGTR (D2-H02/A,H03/A)

-C2MPARE RGTR TØ SHADØW (0-15) [-WAND22(0-15)] 16
ADD 4.0-01 C2MPARE RGTR (D2-H01 → H04/A)

-C2NTRØL RGTR TØ SHADØW (0-11) [-WAND22(0-11)] 12
ADD 4.0-02 C2NTRØL RGTR (D2-F04/B → G04/B)

-STATUS RGTR TØ SHADØW (0-11) [-WAND22(0-11)] 12
ADD 4.0-02 STATUS RGTR (D2-F01/B → H02/B)

ADD UNIT '0'

SHADØW WIRED 'AND' 23

-A ØPERAND RGTR TØ SHADØW (0-15) [-WAND23(0-15)]

ADD 4.1-00 A ØPERAND (D2-F05/A,F08/A)

16

a 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

-ADD UNIT 1 TØ SHADØW (0-15) [-WAND23(0-15)] 16 → C2N 4.4-01 SHADØW WIRED 'AND' 23

-B ØPERAND RGTR TØ SHADØW (0-15) [-WAND23(0-15)] 16
ADD 4.1-00 B ØPERAND (D2-G05/A,G08/A)

-ØUTPUT RGTR TØ SHADØW (0-15) [-WAND23(0-15)] 16
ADD 4.1-00 ØUTPUT RGTR (D2-H06/A,H07/A)

-C2MPARE RGTR TØ SHADØW (0-15) [-WAND23(0-15)] 16
ADD 4.1-01 C2MPARE RGTR (D2-H04/B,H08/B)

-C2NTRØL RGTR TØ SHADØW (0-11) [-WAND23(0-11)] 12
ADD 4.1-02 C2NTRØL RGTR (D2-F08/B → G08/B)

-STATUS RGTR TØ SHADØW (0-11) [-WAND23(0-11)] 12
ADD 4.1-02 STATUS RGTR (D2-F05/B → H06/B)

ADD UNIT '1'

CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
ADD UNIT 0 & 1
SHADØW WIRED 'AND'

DB-D2XMU:D2

CAGE IDENT | DWG NO 60461830 | REV A

SHEET ADD 4.3-00 | PAGE IV-2-21

3. CONTROL UNIT (CON)

SYSTEM FUNCTION

The control unit, which is located in the base processor, controls four areas of the base processor. These four areas are: the 4096-word by 200-bit instruction memory, the crossbar switch, the interrupt logic, and the branch logic. In addition, the control unit distributes control codes and signals throughout the base processor.

GENERAL DESCRIPTION

There is one control unit in the base processor. It consists of the instruction memory and the related control circuits such as the program address register (P register), crossbar switch and related control logic, and the interrupt and branch logic.

LOCATION

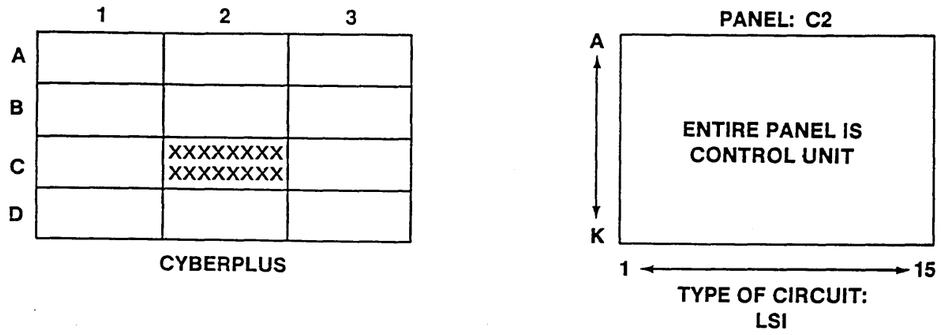


Figure IV-3-1. Location of Control Unit Logic Circuits

FUNCTIONAL DESCRIPTION

The discussion in the following paragraphs refers to the simplified block diagram of the control unit as shown in figure IV-3-2 and the level 2 diagram CON 2.0. The 4,096-word by 200-bit processor instruction memory, once loaded, contains all the instructions required to control machine operations. The memory is loaded via XMAU 0. During each clock cycle the instruction memory fetches one 200-bit instruction word and loads the instruction register. Then it separates the instruction into its appropriate parts and issues one instruction to at least one and not more than four functional units. The instruction word is divided as follows: the 48 clock bits, which are divided into variable-size groups to fit the individual functional unit requirements; the 64 dynamic control bits, which are divided into four groups of 16-bits; the 72 crossbar outputenable bits, which are divided into 18 groups of 4-bits each; and a 16-bit constant field.

The P register holds the address of the location to be read from the instruction memory. The P register is loaded from the P-stack, which is a 16-word by 16-bit memory, or from the branch adder. The P register can also increment itself by one or be set to zero when a master clear is issued by ring port 0. The P register does not have a shadow register, but, if an interrupt occurs, the contents of the P register is automatically saved in the P-stack.

The P +1 adder is used to increment the P register value by one before storing it in the P-stack during a jump (branch) instruction, if the next instruction is inhibited. The P +1 adder can also be used to form the P +2 sum, when required by a jump instruction that does not inhibit the next instruction.

The 16-word P-stack memory is used for storing program addresses for subroutines and return jumps. It is written during the first half of a clock cycle and read during the last half.

The breakpoint register is a 12-bit register loaded from ring port 0. The contents of the breakpoint register and the P register are compared every clock cycle. When the contents are the same and the breakpoint enable is set, the instruction, located at the address which equals the breakpoint register value, is loaded into the instruction register but is not executed, and the ring port control register "run" bit is cleared, stopping the processor. The processor can be restarted from this point by using the ring port 0 instruction SCRb (b=14 for run, or b=13 for step). When the contents are the same and the breakpoint interrupt enable is set, a breakpoint interrupt is requested. In every case when the registers compare equal, a sync pulse is sent to test point C2,B1-TP68 for troubleshooting purposes.

Data from the crossbar is latched into the 16-bit control crossbar register by clock A. The A clock is set by the program into the clock control field of the instruction word, bit 0. The clock bit, when set, gates the data at time 0 of clock cycle one.

The status registers in the various functional units provide inputs to the condition vector logic at the end of each clock cycle. Any of these conditions can be tested by the condition vector logic, which is a 128-to-1 multiplexer for each dynamic control field. The condition vectors tested are those which were valid at the same time the existing instruction was clocked into the instruction register.

Since the control unit can be addressed from any (or all) of the four dynamic control fields, up to four separate tests of the condition vectors can occur at the same time. To handle this situation, one set of condition vector address bits (bits 5--11) from each dynamic control field is provided to the condition vector mux, and one output line for each dynamic control field selection is provided to the branch condition detector. The condition vector multiplexer also provides, from an intermediate stage, the control crossbar selector with all 16 status conditions of the two sectors called for in dynamic control fields 0 and 1.

The branch condition and jump logic is controlled by the branch instruction operation code from the dynamic control field of the instruction word. It looks for the presence or absence of the condition vector bit according to the operation specified in the code. If the desired condition is found to exist, a jump is executed if enabled by clock B (bit 1 of the clock control field, which is also known as the "push bit"). Multiple jumps are possible because of the four separate testing possibilities, however, only one jump will take place at a time.

Some branch (jump) instructions jump to locations specified by the sum of two numbers, which is the resulting output from the branch adder. Inputs to the branch adder are selected by two 16-bit multiplexers, A and B. The A multiplexer selects from the P register, the control crossbar register, the P-stack, or zeros. The B multiplexer selects from the control crossbar register, the ring port on a load P instruction, the instruction K (constant) field, or the interrupt logic.

The interrupt logic processes seven different types of interrupts provided that the interrupt enables have all been set. The processor interrupt enable, bit 16 in the processor control register of ring port 0, must be set to allow any interrupt processing. The indirect interrupt enable, bit 18 in the processor control register, must be set to allow any indirect interrupts to reach the processor interrupt logic; and the breakpoint interrupt enable, bit 9 in the processor control register, must be set to allow a breakpoint interrupt to be generated.

When an interrupt is received by the interrupt priority encoder and logic network, it is recognized if all the proper enables have been set and it is encoded into a three-bit instruction memory address, called the interrupt trap address. When the processor recognizes an interrupt, no instruction execution occurs for two clock cycles while the processor enters the interrupt mode and sets up the control unit for the interrupt processing. During the two clock cycles, the following occurs: the shadow registers contents are frozen for the remainder of the interrupt with the in-process values, the P register contents are written into the P-stack, most of the clock signals are blocked, and the interrupt trap address is loaded into the P register. The processor then restarts, fetches the instruction word located at the trap address, and commences the interrupt processing. The interrupt processing stops when a control unit instruction with the Ji and Fi clocks set (bits 3 and 4, respectively) is executed.

The control crossbar selector inputs one of three 16-bit values to the crossbar, either the K field constant, the 16 condition vectors, or the output of the P-stack.

The crossbar is a giant multiplexing switch that can simultaneously provide each of the sixteen 16-bit inputs to any one of the eighteen 16-bit outputs every clock cycle. The routing of data through the crossbar is controlled by the values placed into the proper 4-bit subfields of the 72-bit crossbar control field. The eighteen 4-bit subfields are each assigned to one of the 18 crossbar outputs (functional unit inputs). The values placed into the 4-bit subfields designate which crossbar input (functional unit output) is to supply the data.

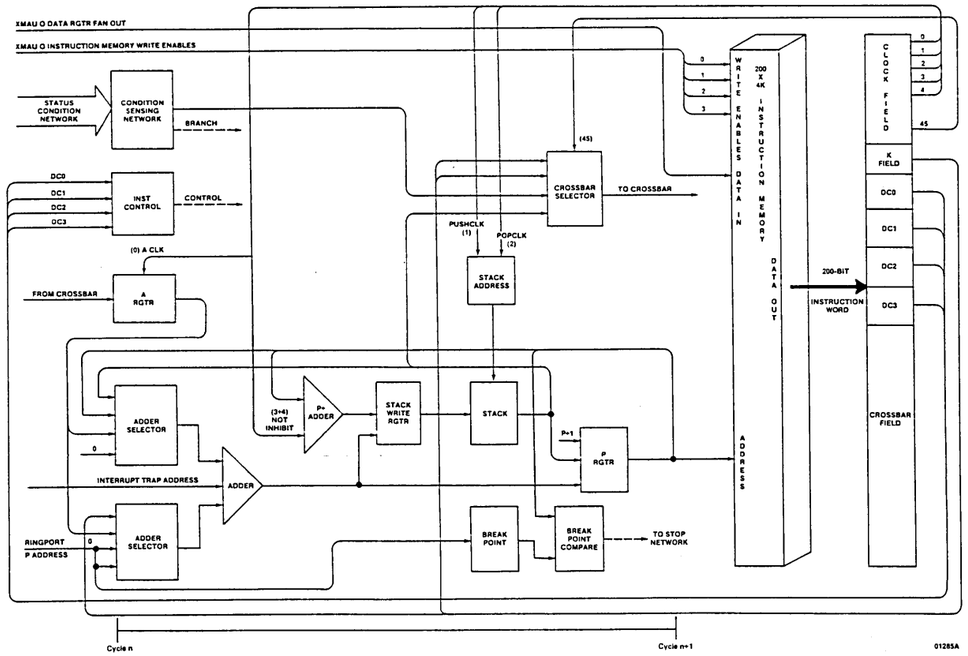


Figure IV-3-2. Control Unit Block Diagram

TIMING

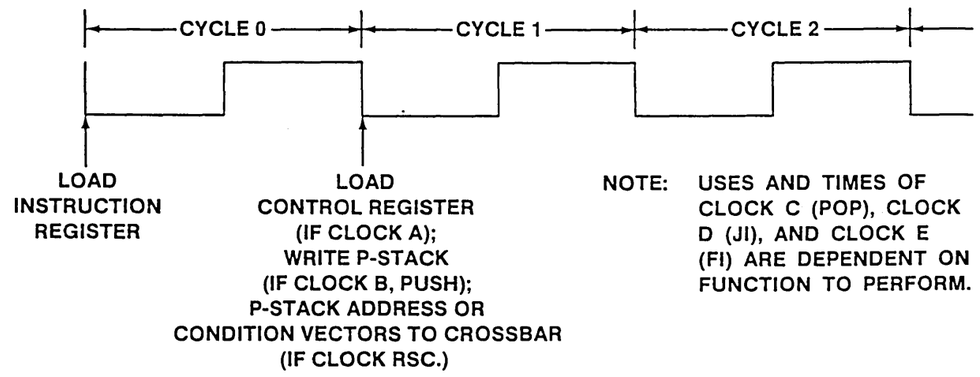

CYCLE 0
CYCLE 1
CYCLE 2
LOAD INSTRUCTION REGISTER
LOAD CONTROL REGISTER (IF CLOCK A); WRITE P-STACK (IF CLOCK B, PUSH); P-STACK ADDRESS OR CONDITION VECTORS TO CROSSBAR (IF CLOCK RSC.)
NOTE: USES AND TIMES OF CLOCK C (POP), CLOCK D (JI), AND CLOCK E (FI) ARE DEPENDENT ON FUNCTION TO PERFORM.

Figure IV-3-3. Control Unit Instructions Timing

ADDRESS FANØUT CØN 4.0-01

INSTRUCTIØN MEMØRY CØN 4.5-00 CØN 4.5-10 CØN 4.5-20 CØN 4.5-30

XMU 2.0 → 64

SBU 2.0 → 7X16
SBU 2.1 → 7X16
FGU 2.0 → 7X16
MUL 2.0 → 2X16
ADD 2.0 → 2X16

200

SHADØW WIRED 'AND'S 0 THRU 30 CØN 4.4-01 ⚠1

4X16 → DMU 2.0
16 → RPU 2.0
6X16 → SHA 2.0
16 → RPU 2.1

INSTRUCTIØN REGISTER CØN 4.4-00

48
4X16
72
16

CLØCK BITS FANØUT CØN 4.1-00

34

TØ ALL UNITS
7 → NU
5 → TØ CØNTRØL UNIT
12 → MUL 2.0 CØNTRØL RGTR
12 → DMU 2.0 MICRØINSTRUCTIØN CØNTRØL
12 → DMU 2.0 MICRØINSTRUCTIØN CØNTRØL
12 → DMU 2.0 MICRØINSTRUCTIØN CØNTRØL
12 → DMU 2.0 MICRØINSTRUCTIØN CØNTRØL
12 → ADD 2.0 CØNTRØL RGTR
12 → ADD 2.0 CØNTRØL RGTR
12 → FGU 2.0 FILE CØNTRØL
12 → FPC 2.0
12 → SBU 2.0 CØNTRØL RGTR
12 → SBU 2.1 CØNTRØL RGTR
12 → XMA 2.0 CØNTRØL RGTR
12 → XMA 2.0 CØNTRØL RGTR
12 → RPU 2.0 CØNTRØL RGTR
12 → RPU 2.1 CØNTRØL RGTR

DC FIELDS FANØUT

4X12

4X7

4X4

CØN 4.1-00

P+1

P REGISTER AND CØUNTER CØN 4.0-00

16 → 4 → 16 → JUMP P + 1 ADDER CØN 4.0-00

NØT INHIBIT

12 → SHA 2.0 SHADØW WIRED 'AND' 33 ⚠1

STACK SELECT CØN 4.0-00

P-STACK CØN 4.5-00

X BAR ADRS CØN 4.2-00

BREAK PØINT REGISTER CØN 4.0-00

RPU 2.0 RING DATA GATE → 12

MULTIPLEXER A CØN 4.0-00

H

STACK ADRS CØUNTER CØN 4.0-01

4 4

8

72

A B C

CØNTRØL UNIT DATA X BAR REGISTER (A REGISTER) CØN 4.0-01

16 → FGU 2.0 SHADØW WIRED 'AND' 12 ⚠1

MULTIPLEXER B CØN 4.0-00

BRANCH ADDER CØN 4.0-00

DATA X BAR

MUL 2.0 ØUTPUT RGTR U → 0
MUL 2.0 ØUTPUT RGTR L → 1
DMU 2.0 ØUTPUT DATA RGTR → 2
DMU 2.0 ØUTPUT DATA RGTR → 3
DMU 2.0 ØUTPUT DATA RGTR → 4
DMU 2.0 ØUTPUT DATA RGTR → 5
DMU 2.0 ØUTPUT DATA RGTR → 6
ADD 2.0 ØUTPUT RGTR → 7
ADD 2.0 ØUTPUT RGTR → 8
FGU 2.0 F ØUTPUT RGTR → 9
FGU 2.0 G ØUTPUT RGTR → 10
SBU 2.0 ØUTPUT RGTR → 11
SBU 2.1 ØUTPUT RGTR → 12
XMA 2.0 A/D DATA RGTR → 13
XMA 2.0 A/D DATA RGTR → 14
RPU 2.1 X BAR DATA → 15

CØN 4.2-01

0 → MUL 2.0 A ØPERAND
1 → MUL 2.0 B ØPERAND
2 → DMU 2.0 INPUT DATA RGTR
3 → SBU 2.1 CØMPARE AND BØØLEAN RGTRS
4 → DMU 2.0 INPUT DATA RGTR
5 → DMU 2.0 INPUT DATA RGTR
6 → DMU 2.0 INPUT DATA RGTR
7 → ADD 2.0 A ØPERAND RGTR
8 → ADD 2.0 B ØPERAND RGTR
9 → ADD 2.0 B ØPERAND RGTR
10 → ADD 2.0 A ØPERAND RGTR
11 → FGU 2.0 F DATA RGTR
12 → FGU 2.0 F DATA RGTR
13 → SBU 2.0 SHIFT ØPERAND RGTR
14 → 16
15 → 16
16 → SBU 2.0 CØMPARE AND BØØLEAN RGTR
17 → SBU 2.1 SHIFT ØPERAND RGTR

X BAR FANØUT CØN 4.2-00

14 → XMA 2.0 SEG AND ADRS CØMP RGTR
14 → XMA 2.0 A/D DATA RGTR
14 → RPU 2.0 X BAR RGTR
14 → XMA 2.0 SEG AND ADRS RGTR
15 → SBU 2.1 DØUBLE SHIFT RGTR
15 → RPU 2.0 A RGTR
15 → XMA 2.0 SEG AND ADRS CØMP RGTR
15 → XMA 2.0 A/D DATA RGTR
15 → RPU 2.1 X BAR RGTR
15 → XMA 2.0 SEG AND ADRS RGTR
14 → SBU 2.0 DØUBLE SHIFT RGTR
14 → RPU 2.1 A RGTR

FRØM CØNTRØL → 3
MUL 2.0 STATUS RGTR → 6
DMU 2.0 STATUS RGTR → 9
DMU 2.0 STATUS RGTR → 9
DMU 2.0 STATUS RGTR → 9
DMU 2.0 STATUS RGTR → 9
ADD 2.0 STATUS RGTR → 12
ADD 2.0 STATUS RGTR → 12
FGU 2.0 → 2
FP X.X → 11
SBU 2.0 STATUS RGTR → 7
SBU 2.1 STATUS RGTR → 7
XMU 2.0 ADRS CØMP RGTR → 11
XMU 2.0 ADRS CØMP RGTR → 3
EQUIP CØDE SWITCHES → EQ SW 8
RPU 2.0 → 4
RPU 2.0 → 4

16X8

CØNTRØL X BAR SELECTØR CØN 4.0-01

A → KFLD

B

4X4

4X3

CØNDITIØN VECTØR STAGE 1 CØN 4.3-00

CØNDITIØN VECTØR STAGE 2 CØN 4.3-00

32 32

16

4

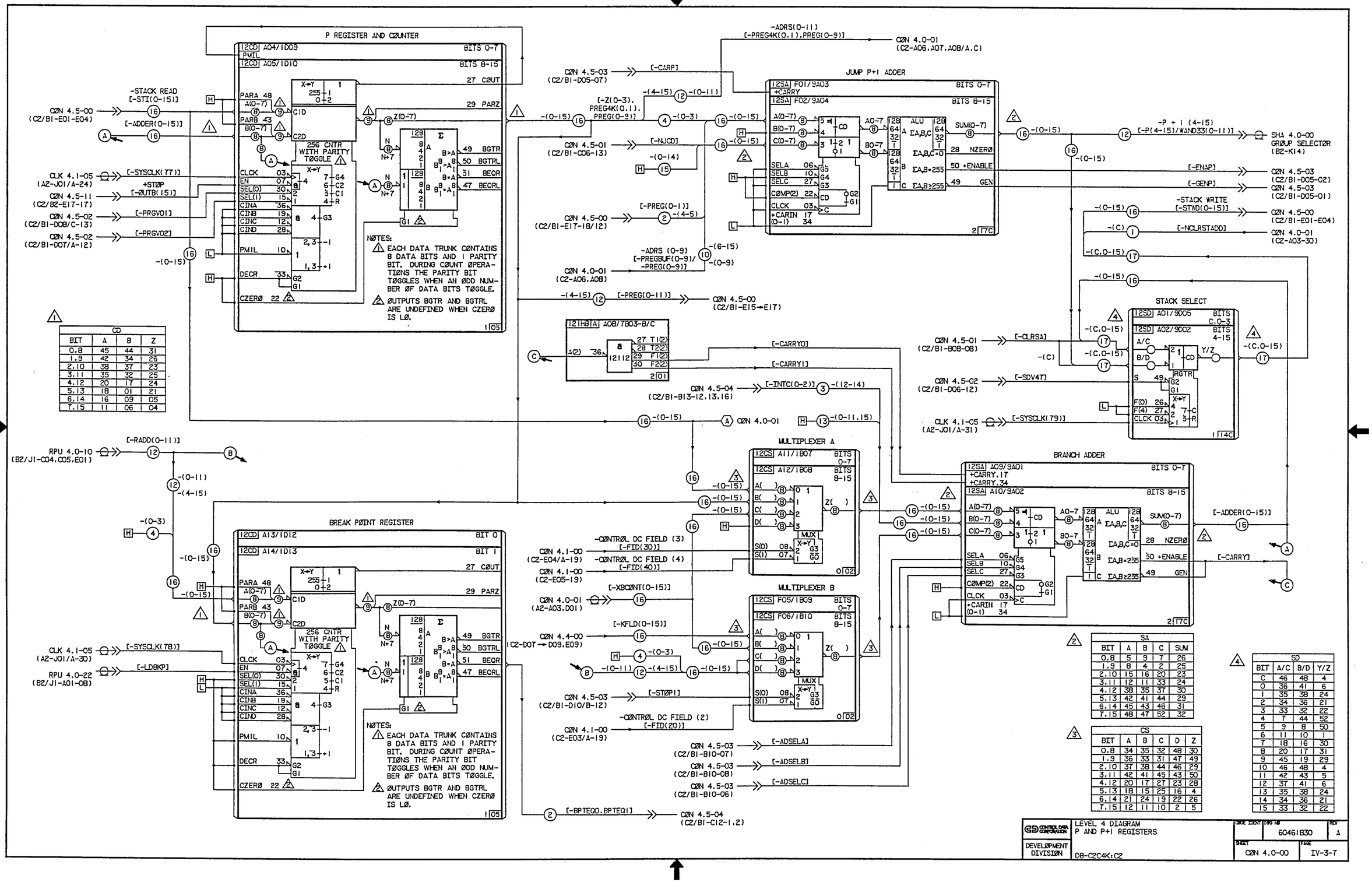
BRANCH CØNDITIØN LØGIC CØN 4.5-02

NØTE: ⚠1 SHADØW RGTR AND WIRED 'AND' DUPLICATED ØN SHA 2.0.

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 2 DIAGRAM
CØNTRØL UNIT
C2

CAGE IDENT | DWG NO 60461830 | REV A
SHEET CØN 2.0 | PAGE IV-3-5

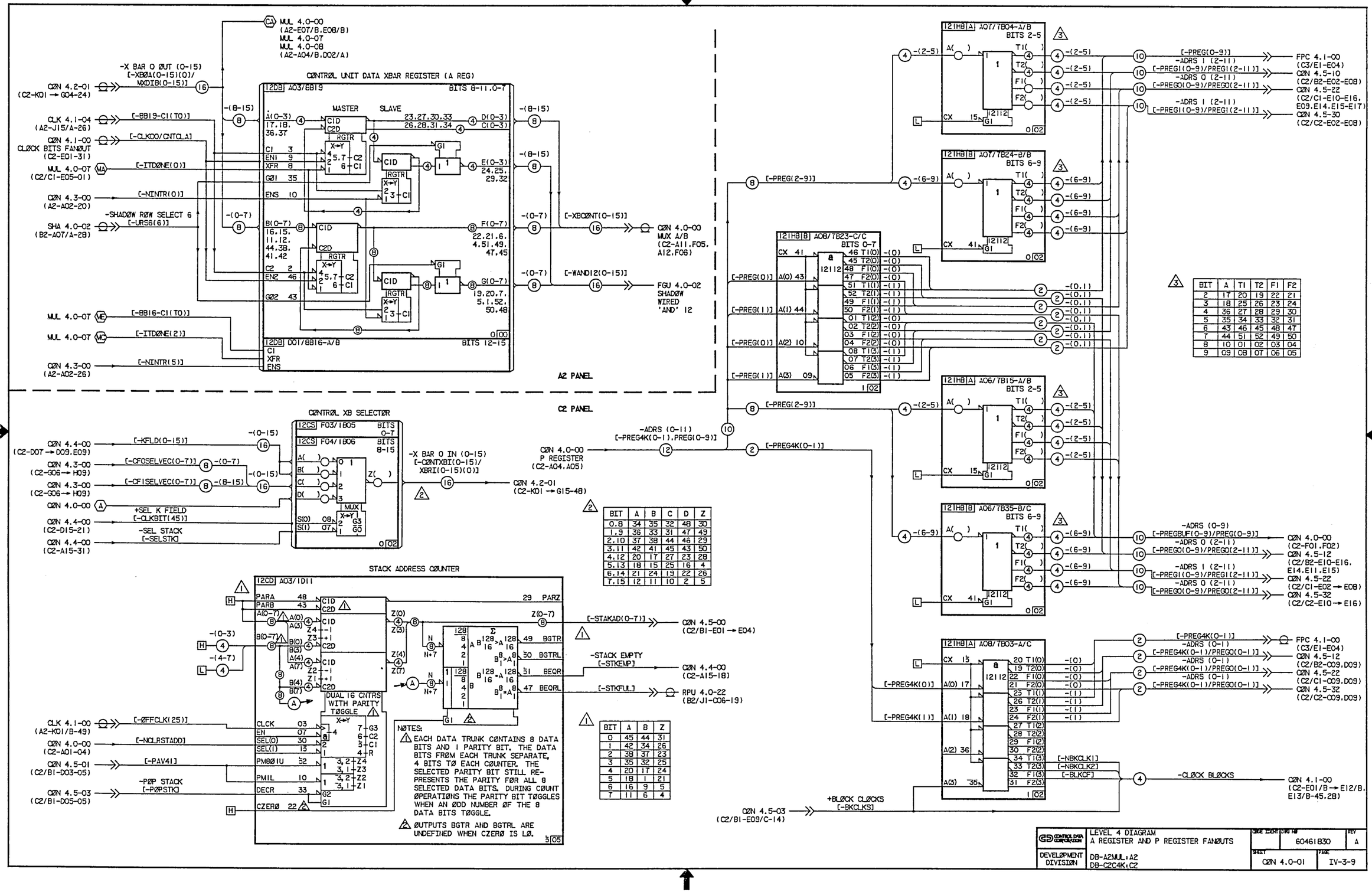


CD			
BIT	A	B	Z
0,8	45	44	31
1,9	42	34	26
2,10	38	37	23
3,11	35	32	25
4,12	20	17	24
5,13	18	01	21
6,14	16	09	05
7,15	11	06	04

SA				
BIT	A	B	C	SUM
0,8	5	9	7	26
1,9	8	4	2	25
2,10	15	16	20	23
3,11	12	11	33	24
4,12	38	35	37	30
5,13	42	41	44	29
6,14	45	43	46	31
7,15	48	47	52	32

SD			
BIT	A/C	B/D	Y/Z
C	46	48	4
0	38	41	6
1	35	38	24
2	34	36	21
3	33	32	22
4	7	44	52
5	9	8	50
6	11	10	1
7	18	16	30
8	20	17	31
9	45	19	29
10	46	48	4
11	42	43	5
12	37	41	6
13	35	38	24
14	34	36	21
15	33	32	22

CS					
BIT	A	B	C	D	Z
0,8	34	35	32	48	30
1,9	36	33	31	47	49
2,10	37	38	44	46	29
3,11	42	41	45	43	50
4,12	20	17	27	23	28
5,13	18	15	25	16	4
6,14	21	24	19	22	26
7,15	12	11	10	2	5



BIT	A	TI	T2	FI	F2
2	17	20	19	22	21
3	18	25	26	23	24
4	36	27	28	29	30
5	35	34	33	32	31
6	43	46	45	48	47
7	44	51	52	49	50
8	10	01	02	03	04
9	09	08	07	06	05

BIT	A	B	C	D	Z
0,8	34	35	32	48	30
1,9	36	33	31	47	49
2,10	37	38	44	46	29
3,11	42	41	45	43	50
4,12	20	17	27	23	28
5,13	18	15	25	16	4
6,14	21	24	19	22	26
7,15	12	11	10	2	5

BIT	A	B	Z
0	45	44	31
1	42	34	26
2	39	37	23
3	35	32	25
4	20	17	24
5	18	1	21
6	16	9	5
7	11	6	4

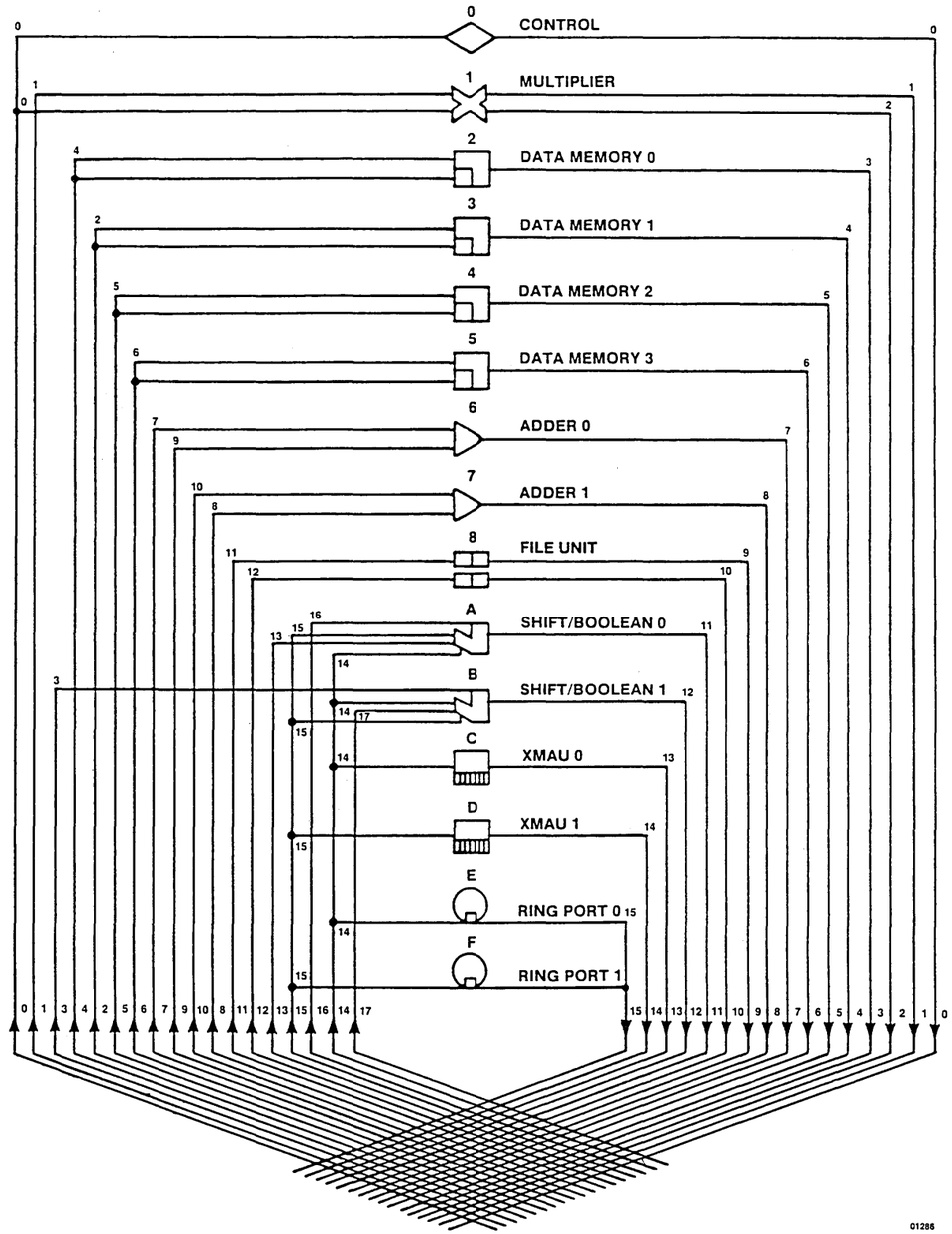


Figure IV-3-4. Crossbar Switch Configuration

12DC F09/2C13 BITS 0-15
CØN 4.4-00 (C2-D07) [-CF0(12-15)]
CØN 4.4-00 (C2-D08) [-CF1(12-15)]
CØN 4.4-00 (C2-E09) [-CF2(12-15)]
CØN 4.4-00 (C2-E09) [-CF3(12-15)]
+BLØCK UMEM [-BLØCMM/BLØCUA]
CØN 4.5-03 (C2/B1-E09/A-07)
A(0-3) 17.20.16.15
B(0-3) 8.9.11.12
C(0-3) 35.34.41.42
D(0-3) 46.43.39.37
G 7
DA 18
DB 10
DC 44
DD 36
DEMUX
U(0-15) 19.22.5.6. 21.24.3.4. 23.26.1.2. 25.52.27.51
(16) (0-15)
-LØAD RING PØRT 1 CØNTRØL RGTR (0) [-GØU(15)/GØRP1] RPU 4.1-01 (B2-G09-09.46)
-LØAD RING PØRT 0 CØNTRØL RGTR (1) [-GØU(14)/GØRP0] RPU 4.0-01 (B2-G07-09.46)
-LØAD XMAU 1 CØNTRØL RGTR (2) [-GØU(13)/GØXM1] XMA 4.1-00 (D2-F11-09.46)
-LØAD XMAU 0 CØNTRØL RGTR (3) [-GØU(12)/GØXM0] XMA 4.0-00 (D2-D11-46)
-LØAD SHIFT BØØLEAN 1 CØNTRØL RGTR (4) [-GØU(11)/GØSB1] SBU 4.1-03 (A2-K09/A.GØ8/A.K14/A-09)
-LØAD SHIFT BØØLEAN 0 CØNTRØL RGTR (5) [-GØU(10)/GØSB0] SBU 4.0-03 (A2-K07/A→J02/A-09)
-LØAD FLØATING PØINT CØNTRØL RGTR (6) [-GØU(9)/] FPC 4.0-03 (C3-A14-40.46.48.07.09)
-LØAD FILE CØNTRØL RGTR (7) [-GØU(8)/GØFIG] FGU 4.0-00 (A2-H08/A→J14/A-09)
-LØAD ADD UNIT 1 CØNTRØL RGTR (8) [-GØU(7)/GØADD1] ADD 4.1-02 (D2-F08/B.G05/B.G08/B-09)
-LØAD ADD UNIT 0 CØNTRØL RGTR (9) [-GØU(6)/GØADD0] ADD 4.0-02 (D2-F04/B.G01/B.G04/B-09)
-LØAD DATA MEM 3 CØNTRØL RGTR (10) [-GØU(5)/GØDM3] DMU 4.3-00 (B2-D04-09.46)
-LØAD DATA MEM 2 CØNTRØL RGTR (11) [-GØU(4)/GØDM2] DMU 4.2-00 (B2-A03-09.46)
-LØAD DATA MEM 1 CØNTRØL RGTR (12) [-GØU(3)/GØDM1] DMU 4.1-00 (B2-D15-09.46)
-LØAD DATA MEM 0 CØNTRØL RGTR (13) [-GØU(2)/GØDM0] DMU 4.0-00 (B2-C13-46)
-LØAD MULTIPLY CØNTRØL RGTR (14) [-GØU(1)/GØMAX] MUL 4.0-07 (A2-E05/A→A06/A-09)
-LØAD CØNTRØL CØNTRØL RGTR (15) [-GØU(0)] CØN 4.5-02 (C2/B1-D06-22)
CØN 4.0-01 (C2-A08) -CLØCK BLØCKS (4) [-CLKCF]
12DC E13/2C10-B/B
F 45 H 28 J 29 K 49 L 48 M 31 N 30 R 32 P 33 T 50 V 47
[-FPBCK(0)] NU
12DC E14/2C11-B/B
-(0) -(0)
[-NFABCK] FPA 4.0-12 (D3-B03/B-41)
[-NFWBCK] FPM 4.2-00 (B3-G01/A.K01-15.17)
12DC E15/2C12-B/B
-(6) -(7) -(0) -(0)
-CØNTRØL DC FIELD (0) (-U(0)) [-FID00] CØN 4.5-02 (C2/B1-D06-23)
CØNTRØL DC FIELD (1) (-U(0)) [-FID10] CØN 4.5-01 (C2/B1-C11/B-22)
-CØNTRØL DC FIELD (2) (-U(0)) [-FID20] CØN 4.0-00 (C2-F05,F06-07) CØN 4.5-03 (C2/B1-C04/B-20)
-CØNTRØL DC FIELD (3) (-U(0)) [-FID30] CØN 4.0-00 (C2-A11,A12-08) CØN 4.5-03 (C2/B1-C04/B-23)
-CØNTRØL DC FIELD (4) (-U(0)) [-FID40] CØN 4.0-00 (C2-A11,A12-07)
-CØNTRØL DC FIELD (5-11) (-U(0) T) [-FID(50-80)] CØN 4.5-03 (C2/B1-C04/B-01) NU
DC FIELDS FANOUT
12DC E01/2C01-A/B BIT 0
12DC E02/2C02-A/B 1
12DC E03/2C03-A/B 2
12DC E04/2C04-A/B 3
12DC E05/2C05-A/B 4
12DC E06/2C06-A/B 5
12DC E10/2C07-A/B 6
12DC E11/2C08-A/B 7
12DC E12/2C09-A/B 8
12DC E13/2C10-A/B 9
12DC E14/2C11-A/B 10
12DC E15/2C12-A/B BIT 11
CØN 4.4-00 (C2-E07) [-CF0D(12-15)]
CØN 4.4-00 (C2-E07) [-CF1D(12-15)]
CØN 4.4-00 (C2-E08) [-CF2D(12-15)]
CØN 4.4-00 (C2-E08) [-CF3D(12-15)]
CØN 4.4-00 (C2-D07) [-CF0(12-15)]
CØN 4.4-00 (C2-D08) [-CF1(12-15)]
CØN 4.4-00 (C2-D09) [-CF2(12-15)]
CØN 4.4-00 (C2-E09) [-CF3(12-15)]
CØN 4.4-00 (C2-D01,D05,D12) [-CF0(0-11)]
CØN 4.4-00 (C2-D02,D06,D13) [-CF1(0-11)]
CØN 4.4-00 (C2-D03,D10,D14) [-CF2(0-11)]
CØN 4.4-00 (C2-D04,D11,D15) [-CF3(0-11)]
A(0-3) 17.20.16.15
B(0-3) 8.9.11.12
C(0-3) 35.34.41.42
D(0-3) 46,43,39,37
G 7
DA 18
DB 10
DC 44
DD 36
DEMUX
U(0-15) 19.22.5.6. 21.24.3.4. 23.26.1.2. 25.52.27.51
[-FID(0-8) (0-15)] 16X12
-MULT DC FIELD (0-11) (-U(1) [-FID(0-8)1/MXØPC0(0-11)]) (6,7)
-DATA MEM 0 DC FIELD (0-11) (-U(2) [-FID(0-8)2/DMØMIN]) MUL 4.0-07 (A2-A06/A.E05/A.E07/A)
-DATA MEM 1 DC FIELD (0-11) (-U(3) [-FID(0-8)3/DM1MIN]) DMU 4.0-00 (B2-C13)
-DATA MEM 2 DC FIELD (0-11) (-U(4) [-FID(0-8)4/DM2MIN]) DMU 4.1-00 (B2-D15)
-DATA MEM 3 DC FIELD (0-11) (-U(5) [-FID(0-8)5/DM3MIN]) DMU 4.2-00 (B2-A03)
-ADD UNIT 0 DC FIELD (0-11) (-U(6) [-FID(0-8)6/ADØCTL(0-11)]) DMU 4.3-00 (B2-D04)
-ADD UNIT 1 DC FIELD (0-11) (-U(7) [-FID(0-8)7/ADICTL(0-11)]) (-0)
-FILE DC FIELD (0-11) (-U(8) [-FID(0-8)8/FILEØP]) ADD 4.0-02 (D2-F04/B.G01/B.G04/B)
-FLØATING PØINT DC FIELD (0-11) (-U(9) [-FID(0-8)9/]) (-0)
-SHIFT/BØØLEAN 0 DC FIELD (0-11) (-U(10) [-FID(0-8)10/SBØØPC(0-11)]) ADD 4.1-02 (D2-F08/B.G05/B.G08/B)
-SHIFT/BØØLEAN 1 DC FIELD (0-11) (-U(11) [-FID(0-8)11/SB1ØPC(0-11)]) FGU 4.0-00 (A2-H08/A→J14/A)
-XMAU 0 DC FIELD (0-11) (-U(12) [-FID(0-8)12/XMØCTL]) FPC 4.0-03 (C3-D15,A15)
-XMAU 1 DC FIELD (0-11) (-U(13) [-FID(0-8)13/XM1CTL]) (-0)
-RING PØRT 0 DC FIELD (0-11) (-U(14) [-FID(0-8)14/RPØCTL(0-11)]) SBU 4.0-03 CØNTRØL REGISTER (A2-K07/A→J02/A)
-RING PØRT 1 DC FIELD (0-11) (-U(15) [-FID(0-8)15/RP1CTL(0-11)]) (-0)
SBU 4.1-03 CØNTRØL REGISTER (C2-K09/A,G08/A,K14/A)
XMA 4.0-00 (D2-C12)
XMA 4.1-00 (D2-F11)
RPU 4.0-01 (B2-G07)
RPU 4.1-01 (B2-G09)
CØN 4.4-00 (C2-D01→D15) -CØNTRØL CLØCK BITS [-CLK(XX)] (34)
NU (-34,38)
[-BKCLKS] [-NBKCLK1] [-NBKCLK2] (36)
CLØCK BITS FANOUT
12DC E01/2C01-B/B BITS 0,5-7
12DC E02/2C02-B/B 8,10-11,13
12DC E03/2C03-B/B 14,16-17,21
12DC E04/2C04-B/B 22-25
12DC E05/2C05-B/B 26-29
12DC E06/2C06-B/B 30-32,35
12DC E10/2C07-B/B 34-36,39
12DC E11/2C08-B/B 38-41
12DC E12/2C09-B/B 42-44,47
A(0-3) 28.29. 49.48
T(0-3) 31.32. 50.47
F(0-1) 30.33
G1
45
-(34) [-NFCBLK] FPC 4.0-04 (C3-B08/B.C,D)
-(38) [-NFDBLK/] FPD 4.2-01 (A3-F04/A-15)
[-CLK00/CNTCLA] CØN 4.0-01 CØNTRØL UNIT DATA XB RGTR (A2-A03-09.46)
-MULTIPLY CLØCK A [-CLK05/NXCLA] MUL 4.0-00 (A2-E04/B.E03/B-46)
-MULTIPLY CLØCK B [-CLK06/NXCLB] MUL 4.0-07 (A2-D01/B.D02/B-46)
[-CLK07/DMØCLA] DMU 4.0-00 (B2-C08-09.46)
[-CLK08/DMØCLB] DMU 4.0-01 (B2-C11/B.C12/B-46)
[-CLK10/DM1CLA] DMU 4.1-00 (B2-D09-09.46)
[-CLK11/DM1CLB] DMU 4.1-01 (B2-D11/B.D12/B-46)
[-CLK13/DM2CLA] DMU 4.2-00 (B2-A08-09.46)
[-CLK14/DM2CLB] DMU 4.2-01 (B2-A04/B.A05/B-46)
[-CLK16/DM3CLA] DMU 4.3-00 (B2-D08-09.46)
[-CLK17/DM3CLB] DMU 4.3-01 (B2-D05/B.D06/B-46)
[-CLK19/FCLC(0)] CØN 4.5-01 (C2/B1-D03-01)
[-CLK20/FCLC(1)] CØN 4.5-01 (C2/B1-D03-22)
[-CLK21/FCLC(2)] CØN 4.5-01 (C2/B1-D03-19)
[-CLK22/FCLC(3)] CØN 4.5-01 (C2/B1-D03-17)
[-CLK23/FCLC(4)] CØN 4.5-01 (C2/B1-D02-02)
[-CLK24/FCLC(5)] CØN 4.5-01 (C2/B1-D02-01)
[-CLK25/SBOCLA] SBU 4.0-00 (A2-K05,K06/A-09)
[-CLK26/SBOCLB] SBU 4.0-00 (A2-K03/A.K04-09)
[-CLK27/FCLC(6)] CØN 4.5-01 (C2/B1-D02-22)
[-CLK28/SBOCLD] SBU 4.0-03 (A2-G07/B-46)
[-CLK29/SB1CLA] SBU 4.1-00 (A2-K10/A.K11-09)
[-CLK30/SB1CLB] SBU 4.1-00 (A2-K12.K13/A-09)
[-CLK31/FCLC(7)] CØN 4.5-01 (C2/B1-D02-19)
[-CLK32/SB1CLD] SBU 4.1-03 (A2-G08/B-46)
[-CLK35/CLKD] XMA 4.10-04 (D2/E1-B15-22)
[-CLK36/CLKE1] XMA 4.10-05 (D2/E1-A04-19)
[-CLK39/CLKD] XMA 4.11-04 (D2/E2-D02-03)
[-CLK40/CLKE] XMA 4.11-05 (D2/E2-B08-19)
[-CLK41/RPOCA] RPU 4.0-01 (B2-H08-19.42)
[-CLK42/RPOCB] RPU 4.0-21 (B2/J1-A04/B-22)
[-CLK43/RP1CA] RPU 4.1-01 (B2-H04-19.42)
[-CLK44/RP1CB] RPU 4.1-21 (B2/J2-A04/B-22)
-CLØCK BIT 47 [-CLK47/FICLKC] FGU 4.0-00 (A2-H08/A→J14/A-17)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
CØNTRØL X BAR AND CLØCK BIT FANOUT.
DB-C2C4K-C2
05-15-86
CODE IDENTIFICATION 60461830
REV E
SHEET CØN 4.1-00
PAGE IV-3-11
450 60 70 80 90 FULL

X BAR ADRS

121H8[A] GC5/7B11-A/B BITS 0-3
121H8[A] HC5/7B12-A/B 8-11
121H8[A] JC5/7B13-A/B 16-19
121H8[A] F10/7BC8-A/B 24-27
121H8[A] F11/7B09-A/B 32-35
121H8[A] F12/7B10-A/B 40-43
121H8[A] F13/7B05-A/B 48-51
121H8[A] F14/7BC6-A/B 56-59
121H8[A] F15/7B07-A/B BITS 64-67

121H8[B] GC5/7B31-B/B BITS 4-7
121H8[B] HC5/7B32-B/B 12-15
121H8[B] JC5/7B33-B/B 20-23
121H8[B] F10/7B28-B/B 28-31
121H8[B] F11/7B29-B/B 36-39
121H8[B] F12/7B30-B/B 44-47
121H8[B] F13/7B25-B/B 52-55
121H8[B] F14/7B26-B/B 60-63
121H8[B] F15/7B27-B/B BITS 68-71

A( ) 4: 17,18, 36,35 — TI( ) 4: 20,25,27,34 — T2( ) 4: 19,26,28,33 — FI( ) 4: 22,23,29,32 — F2( ) 4: 21,24,30,31
CX 15 — I2112 GI — 002

A( ) 4: 43,44, 10,9 — TI( ) 4: 46,51,1,8 — T2( ) 4: 45,52,2,7 — FI( ) 4: 48,49,3,6 — F2( ) 4: 47,50,4,5
CX 41 — I2112 GI — 000

C2N 4.4-00 (C2-D01 → D15) [-XBAD0(0-71)] → 72 -(0-71) → 36

T2 [-XBA0(0-71)]
T2 [-XBA1(0-71)]
T2 [-NXBA0(0-71)]
T2 [-NXBA1(0-71)]

C2N 4.2-01 (C2-K01 → G15)

C2 PANEL

X BAR FANØUT

121H8[A] AC6/7BC5-A/B BITS 0-3
121H8[A] AC7/7B07-A/B 8-11
121H8[A] A10/7B01-A/B 0-3
121H8[A] A11/7B03-A/B BITS 8-11

121H8[B] AC6/7BC6-B/B BITS 4-7
121H8[B] AC7/7BC8-B/B 12-15
121H8[B] A10/7B02-B/B 4-7
121H8[B] A11/7B04-B/B BITS 12-15

121H8[A] FC9/7B40-A/B BITS 0-3
121H8[A] F10/7B42-A/B 8-11
121H8[A] AC4/7B09-A/B 0-3
121H8[A] AC5/7B11-A/B BITS 8-11

121H8[B] FC9/7B41-B/B BITS 4-7
121H8[B] F10/7B43-B/B 12-15
121H8[B] AC4/7B10-B/B 4-7
121H8[B] AC5/7B12-B/B BITS 12-15

-X BAR 14 ØUT (0-15) [-XBØC(0-15)(14) /XMØXBI(0-15)] — C2N 4.2-01 (C2-K12 → G15-30) — 16 -(0-15) → 8 -(4-7, 12-15)
-X BAR 15 ØUT (0-15) [-XBØC(0-15)(15) /XMIXBI(0-15)] — C2N 4.2-01 (C2-K12 → G15-04) — 16 -(0-15) → 8 -(4-7, 12-15)
-(0-3, 8-11)

A( ) 4: 17,18, 36,35 — TI( ) 4: 20,25,27,34 — T2( ) 4: 19,26,28,33 — FI( ) 4: 22,23,29,32 — F2( ) 4: 21,24,30,31
CX 15 — I2112 GI — 002

A( ) 4: 43,44, 10,9 — TI( ) 4: 46,51,1,8 — T2( ) 4: 45,52,2,7 — FI( ) 4: 48,49,3,6 — F2( ) 4: 47,50,4,5
CX 41 — I2112 GI — 000

-(4-7, 12-15) → 16:

- -DATA Ø [-XBRFØ2(0-15)] → XMA 4.0-01 SEG AND ADRS COMP (D2-B13)
- [-XBRFØ3(0-15)] → XMA 4.0-01 A/D DATA (D2-D03)
- -X BAR TO RPO [-RPOXBR(0-15)/ RPOXBI(0-15)] → RPU 4.0-01 X BAR RGTR (B2-H08)
- [-XBRFØ1(0-15)] → XMA 4.0-00 SEG AND ADRS (D2-C13)
- -DBL SHIFT INPUT [-NSBIXB(0-15)/ SBIDIB(0-15)] → SBU 4.1-00 (A2-K12,K13/A) DBL SHIFT INPUT (A2-K12,K13)
- -X BAR TØ RPO A RGTR [-NRPOXB(0-15)/ ØFDO(0-15)] → RPU 4.2-00 A RGTR RPO (B2/F2-C14 → C16)
- -DATA 1 [-XBRF02(0-15)] → XMA 4.1-01 SEG AND ADRS COMP (D2-G11)
- [-XBRF03(0-15)] → XMA 4.1-01 A/D DATA (D2-K09)
- -X BAR TØ RPI [-RPIXBR(0-15) RPIXBI(0-15)] → RPU 4.1-01 X BAR RGTR (B2-H04)
- [-XBRF01(0-15)] → XMA 4.1-00 SEG AND ADRS (D2-H13)
- -DBL SHIFT INPUT (0-15) [-NSBOXB(0-15)/ SBØDIB(0-15)] → SBU 4.0-00 DØUBLE SHIFT RGTR (A2-K04,K03/A)
- -X BAR TØ RPI A RGTR [-NRPIXB(0-15)/ ØFDI1(0-15)] → RPU 4.2-01 A RGTR RPI (B2/F2-C02,C04)

D2 PANEL

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM DATA X BAR ADRS AND X BAR FANØUT	CODE IDENT	DRG NO 60461830 REV A
DEVELØPMENT DIVISION	DB-C2C4K:C2 DB-D2XMJ:D2	SHEET C2N 4.2-00	PAGE IV-3-13

X BAR ØUTPUT/FUNCTIØNAL UNIT INPUT

INST BIT	128					151	152					175	176					199
XBA BIT	0					23	24					47	48					71
XBA NØ.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	CTRL MULB	MULA	DM1	SB1B	DMØ	DM2	DM3	ADØA	AD1B	ADØB	AD1A	F	G	SBØS	XMØ RPØ SBØSC SB1D	XM1 RP1 SBØD SB1SC	SBØB	SB1S

X BAR INPUT/FUNCTIØNAL UNIT ØUTPUT

0	CØNTRØL UNIT	8	ADDER 1
1	MULTIPLIER HIGHER	9	FILE F
2	MULTIPLIER LØWER	A	FILE G
3	DATA MEMØRY 0	B	SHIFT BØØLEAN 0
4	DATA MEMØRY 1	C	SHIFT BØØLEAN 1
5	DATA MEMØRY 2	D	XMAU 0
6	DATA MEMØRY 3	E	XMAU 1
7	ADDER 0	F	RING PØRT 0/RING PØRT 1

DATA X BAR

12DA	K01/8A03	BIT 0
12DA	J01/8A06	1
12DA	H01/8A09	2
12DA	G01/8A12	3
12DA	K02/8A15	4
12DA	J02/8A18	5
12DA	H02/8A21	6
12DA	G02/8A24	7
12DA	K03/8A27	8
12DA	J03/8A30	9
12DA	H03/8A33	10
12DA	G03/8A36	11
12DA	K04/8A39	12
12DA	J04/8A42	13
12DA	H04/8A45	14
12DA	G04/8A48	15
12DA	K07/8A02	0
12DA	J07/8A05	1
12DA	K06/8A08	2
12DA	J06/8A11	3
12DA	K09/8A14	4
12DA	J09/8A17	5
12DA	K08/8A20	6
12DA	J08/8A23	7
12DA	K10/8A26	8
12DA	J10/8A29	9
12DA	H10/8A32	10
12DA	G10/8A35	11
12DA	K11/8A38	12
12DA	J11/8A41	13
12DA	H11/8A44	14
12DA	G11/8A47	15
12DA	K12/8A01	0
12DA	J12/8A04	1
12DA	H12/8A07	2
12DA	G12/8A10	3
12DA	K13/8A13	4
12DA	J13/8A16	5
12DA	H13/8A19	6
12DA	G13/8A22	7
12DA	K14/8A25	8
12DA	J14/8A28	9
12DA	H14/8A31	10
12DA	G14/8A34	11
12DA	K15/8A37	12
12DA	J15/8A40	13
12DA	H15/8A43	14
12DA	G15/8A46	BIT 15

-X BAR 0 ØUT (0-15) [-XBØA(0-15)(0)/AXDIB(0-15)] → CØN 4.0-01 (A2-A03,D01)

-X BAR 1 ØUT (0-15) [-XBØA(0-15)(1)/AXDIA(0-15)] → MUL 4.0-07 A ØPERAND (A2-E11/B,E10/B)

-X BAR 2 ØUT (0-15) [-XBØA(0-15)(2)/DM1XBI(0-15)] → DMU 4.1-01 INPUT DATA RGTR (B2-D11/B,D12/B,C06/B,D01/B)

-X BAR 3 ØUT (0-15) [-XBØA(0-15)(3)/SB1BLN] → SBU 4.1-02 CØMPARE/BØØLEAN (A2-K09/B,K13/B,K10/B,K14/B)

-X BAR 4 ØUT (0-15) [-XBØA(0-15)(4)/DMØXBI(0-15)] → DMU 4.0-01 INPUT DATA RGTR (B2-C11/B,C12/B,C04/B,C01/B)

-X BAR 5 ØUT (0-15) [-XBØA(0-15)(5)/DM2XBI(0-15)] → DMU 4.2-01 INPUT DATA RGTR (B2-A04/B,A05/B,A12/B,A15/B)

-X BAR 6 ØUT (0-15) [-XBØB(0-15)(6)/DM3XBI(0-15)] → DMU 4.3-01 INPUT DATA RGTR (B2-D05/B,D06/B,D10/B,C14/B)

-X BAR 7 ØUT (0-15) [-XBØB(0-15)(7)/ADDAØP(0-15)] → ADD 4.0-00 A ØPERAND (D2-F01/A,F04/A)

-X BAR 8 ØUT (0-15) [-XBØB(0-15)(8)/ADIBØP(0-15)] → ADD 4.1-00 B ØPERAND (D2-G05/A,G08/A)

-X BAR 9 ØUT (0-15) [-XBØB(0-15)(9)/ADØBØP(0-15)] → ADD 4.0-00 B ØPERAND (D2-G01/A,G04/A)

-X BAR 10 ØUT (0-15) [-XBØB(0-15)(10)/ADIAØP(0-15)] → ADD 4.1-00 A ØPERAND (D2-F05/A,F08/A)

-X BAR 11 ØUT (0-15) [-XBØB(0-15)(11)/FDATA] → FGU 4.0-00 F DATA RGTR (A2-H08/B,J08/B)

-X BAR 12 ØUT (0-15) [-XBØC(0-15)(12)/GDATA] → FGU 4.0-00 G DATA RGTR (A2-H14/B,J14/B)

-X BAR 13 ØUT (0-15) [-XBØC(0-15)(13)/SBØDIA(0-15)] → SBU 4.0-00 SHIFT ØPERAND (A2-K05,K06/A)

-X BAR 14 ØUT (0-15) [-XBØC(0-15)(14)/XMØXBI(0-15)] → CØN 4.2-00 X BAR FANØUT (D2-A06 → A11)

-X BAR 15 ØUT (0-15) [-XBØC(0-15)(15)/XM1XBI(0-15)] → CØN 4.2-00 X BAR FANØUT (D2-F09,F10,A04,A05)

-X BAR 16 ØUT (0-15) [-XBØC(0-15)(16)/SBØBLN(0-15)] → SBU 4.0-02 CØMPARE/BØØLEAN RGTRS (A2-K07/B,K03/B,K06/B,J02/B)

-X BAR 17 ØUT (0-15) [-XBØC(0-15)(17)/SB1DIA(0-15)] → SBU 4.1-00 SHIFT ØPERAND (A2-K10/A,K11)

CØN 4.2-00 (C2-G05 → F15)

[-XBAØ(0-7)] → -(48-71)
[-XBA1(0-7)] → -(48-71)
[-NXBAØ(0-7)] → +(48-71)
[-NXBA1(0-7)] → -(48-71)

S(X)

+(48-51) SØ(0-3) 18,15,20,16
+(52-55) S1(0-3) 26,23,28,27
+(56-59) S2(0-3) 37,38,34,36
+(60-63) S3(0-3) 11,9,10,12
+(64-67) S4(0-3) 3,46,2,51
+(68-71) S5(0-3) 42,41,43,44

X→Y AI5 AØØ
X→Y BI5 BØØ
X→Y CI5 CØØ
X→Y DI5 DØØ
X→Y EI5 EØØ
X→Y FI5 FØØ

MUX

DI(0-15) 48,49,45,52, 7,6,8,5, 35,33,32,29, 22,19,21,17

A	24 DØ(0)
B	25 DØ(1)
C	30 DØ(2)
D	04 DØ(3)
E	01 DØ(4)
F	50 DØ(5)

0 03

256 → -(24-47)
256 → +(24-47)
256 → -(48-71)
256 → -(48-71)
256 → +(48-71)
256 → -(48-71)

-X BAR 0-15 IN (0-15) [-XBRI(0-15)(0-15)] → 256

-X BAR 0 IN (0-15) [-CØNTXBI(0-15)/XBRI(0-15)(0)] → CØN 4.0-01 (C2-F03,F04)

-X BAR 1 IN (0-15) [-VXØUTU(0-15)/XBRI(0-15)(1)] → MUL 4.0-08 ØUTPUT RGTR U (A2-A15/B,E15/B)

-X BAR 2 IN (0-15) [-VXØUTL(0-15)/XBRI(0-15)(2)] → MUL4.0-08 ØUTPUT RGTR L (A2-A06/B,E05/B)

-X BAR 3 IN (0-15) [-DMCØUT/XBRI(0-15)(3)] → DMU 4.0-01 ØUTPUT DATA RGTR (B2-C02/B,C03/B)

-X BAR 4 IN (0-15) [-DM1ØUT/XBRI(0-15)(4)] → DMU 4.1-01 ØUTPUT DATA RGTR (B2-D02/B,D03/B)

-X BAR 5 IN (0-15) [-DM2ØUT/XBRI(0-15)(5)] → DMU 4.2-01 ØUTPUT DATA RGTR (B2-A13/B,A14/B)

-X BAR 6 IN (0-15) [-DM3ØUT/XBRI(0-15)(6)] → DMU 4.3-01 ØUTPUT DATA RGTR (B2-D13/B,D14/B)

-X BAR 7 IN (0-15) [-ADØØUT(0-15)/XBRI(0-15)(7)] → ADD 4.0-00 ØUTPUT RGTR (D2-H02/A,H03/A)

-X BAR 8 IN (0-15) [-AD1ØUT(0-15)/XBRI(0-15)(8)] → ADD 4.1-00 ØUTPUT RGTR (D2-H06/A,H07/A)

-X BAR 9 IN (0-15) [-FØUT(0-15)/XBRI(0-15)(9)] → FGU 4.0-01 F FILE DATA ØUTPUT RGTR (A2-K08,G15/A)

-X BAR 10 IN (0-15) [-GØUT(0-15)/XBRI(0-15)(10)] → FGU 4.0-01 G FILE DATA ØUTPUT RGTR (A2-G15/B,H15/B)

-X BAR 11 IN (0-15) [-SBØØUT(0-15)/XBRI(0-15)(11)] → SBU 4.0-02 STATUS AND ØUTPUT RGTRS (A2-G06,G02)

-X BAR 12 IN (0-15) [-SB1ØUT(0-15)/XBRI(0-15)(12)] → SBU 4.1-02 STATUS AND ØUTPUT RGTRS (A2-G09,G13)

-X BAR 13 IN (0-15) [-XMØXBØ/XBRI(0-15)(13)] → XMA 4.0-01 (D2-B06,B07)

-X BAR 14 IN (0-15) [-XM1XBØ/XBRI(0-15(14)] → XMA 4.1-01 (D02-J05,J06)

-X BAR 15 IN (0-15) [-STRI(0-15)/XBRI(0-15(15)] → RPU 4.1-13 X BAR DATA SELECT (B2/J2-A10 → C11)

BITS (0-7/8-15)

S(X) CØDE	DI PIN NØ	BITS 0-7 IN X BAR NØ	BITS 8-15 IN X BAR NØ
0	48	0	15
1	49	1	14
2	45	2	13
3	52	3	12
4	7	4	11
5	6	5	10
6	8	6	9
7	5	7	8
8	35	8	7
9	33	9	6
A	32	10	5
B	29	11	4
C	22	12	3
D	19	13	2
E	21	14	1
F	17	15	0

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
DATA X BAR
DB-C2C4K:C2

CODE IDENT NO. 60461830
REV A
SHEET CØN 4.2-01
PAGE IV-3-15

TABLE IV-3-1. CYBERPLUS CONDITION VECTORS

CONTROL UNIT	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
		CON 4.5-03	CON 4.3-00	
		C2/B1-E14-08 -INTPRS	C2-G08-48 -CVB2(0)	CU.IP
		CON 4.4-00	CON 4.3-00	
		C2-A15-27 -STKEMP	C2-H06-17 -CVB4(0)	CU.EMP

RING PORT	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
		RPU 4.0-01	CON 4.3-00	
0	0	B2-H10-28 -OFFULO	C2-G06-49 -CVB0(1)	IO.FUL
		RPU 4.0-21	CON 4.3-00	
0	1	B2/J1-D07-12 -ANYCOM	C2-G07-49 -CVB1(1)	IO.ANY
0	2	B2/J1-D07-16 -ALCMP	C2-G08-49 -CVB2(1)	IO.ALL
		RPU 4.2-01	CON 4.3-00	
0	3	B2/F2-C10-11 -STRGO	C2-G09-49 -CVB3(1)	IO.STP
		RPU 4.1-01	CON 4.3-00	
1	4	B2-H07-28 -OFFUL1	C2-H06-21 -CVB4(1)	I1.FUL
		RPU 4.1-21	CON 4.3-00	
1	5	B2/J2-D07-12 -ANYCM1	C2-H07-21 -CVB5(1)	I1.ANY
1	6	B2/J2-D07-16 -ALCMP1	C2-H08-21 -CVB6(1)	I1.ALL
		RPU 4.2-01	CON 4.3-00	
1	7	B2/F2-C06-11 -STRG1	C2-H09-21 -CVB7(1)	I1.STP
		RPU 4.0-22	CON 4.3-00	
0		B2/J1-C07-14 -SKFULL	C2-G09-48 -CVB3(0)	CU.FUL

FILE UNIT	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
		FGU 4.0-01	CON 4.3-00	
F		A2-H15-23 -FSTAT(0)	C2-G06-21 -CVB0(14)	FO.NG
G		A2-H15-27 -GSTAT(0)	C2-G07-21 -CVB1(14)	GO.NG

MULTIPLY UNIT	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
		MUL 4.0-08	CON 4.3-00	
	0	A2-E15-23 -MXSTAT(0)	C2-G06-45 -CVB0(2)	MO.EQ.CH
	1	A2-E15-27 -MXSTAT(1)	C2-G07-45 -CVB1(2)	MO.EQ.CL
	2	A2-E15-30 -MXSTAT(2)	C2-G08-45 -CVB2(2)	MO.GT.CH
	3	A2-E15-33 -MXSTAT(3)	C2-G09-45 -CVB3(2)	MO.GT.CL
	4	A2-A15-23 -MXSTAT(4)	C2-H06-19 -CVB4(2)	MO.NGH
	5	A2-A15-27 -MXSTAT(5)	C2-H07-19 -CVB5(2)	MO.NGL

ADDER	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
		ADD 4.0-02	CON 4.3-00	
0	0	D2-H02-23 -AOUAGC(0)	C2-G06-52 -CVB0(3)	AO.GT.CU
0	1	D2-H02-27 -AOUAEC(1)	C2-G07-52 -CVB1(3)	AO.EQ.CU
0	2	D2-H02-30 -AOLAGC(2)	C2-G08-52 -CVB2(3)	AO.GT.CL
0	3	D2-H02-33 -AOLAEC(3)	C2-G09-52 -CVB3(3)	AO.EQ.CL
0	4	D2-H03-23 -AOAGC(4)	C2-H06-52 -CVB4(3)	AO.GT.C
0	5	D2-H03-27 -AOAEC(5)	C2-H07-52 -CVB5(3)	AO.EQ.C
0	6	D2-F01-23 -AOMSB(6)	C2-H08-52 -CVB6(3)	AO.NG
0	7	D2-F01-30 -AOUAEO(7)	C2-H09-52 -CVB7(3)	AO.NE.ZRU
0	8	D2-F01-33 -AOLAEO(8)	C2-G06-07 -CVB0(4)	AO.NE.ZRL
0	9	D2-H03-31 -AONCY(9)	C2-G07-07 -CVB1(4)	AO.NCY
0	10	D2-F01-27 -AOOVF(10)	C2-G08-07 -CVB2(4)	AO.OV
0	11	D2-H03-34 -A1NCY(11)	C2-H06-32 -CVB4(5)	A1.NCY
		ADD 4.1-02	CON 4.3-00	
1	0	D2-H06-23 -A1UAGC(0)	C2-G09-07 -CVB3(4)	A1.GT.CU
1	1	D2-H06-27 -A1UAEC(1)	C2-H06-29 -CVB4(4)	A1.EQ.CU
1	2	D2-H06-30 -A1LAGC(2)	C2-H07-29 -CVB5(4)	A1.GT.CL
1	3	D2-H06-33 -A1LAEC(3)	C2-H08-29 -CVB6(4)	A1.EQ.CL
1	4	D2-H07-23 -A1AGC(4)	C2-H09-29 -CVB7(4)	A1.GT.C
1	5	D2-H07-27 -A1AEC(5)	C2-G06-06 -CVB0(5)	A1.EQ.C
1	6	D2-F05-23 -A1MSB(6)	C2-G07-06 -CVB1(5)	A1.NG
1	7	D2-F05-30 -A1UAEO(7)	C2-G08-06 -CVB2(5)	A1.NE.ZRU
1	8	D2-F05-33 -A1LAEO(8)	C2-G09-06 -CVB3(5)	A1.NE.ZRL
1	9	D2-H07-30 -AAGC32(9)	C2-H08-32 -CVB6(5)	A01.GT.C
1	10	D2-F05-27 -A1OVF(10)	C2-H07-32 -CVB5(5)	A1.OV
1	11	D2-H07-33 -AAEC32(11)	C2-H09-32 -CVB7(5)	A01.EQ.C

SHIFT BOOLEAN	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
		SBU 4.0-02	CON 4.3-00	
0	0	A2-G06-23 -SBOSTA(0)	C2-G06-08 -CVB0(6)	BO.EQ.CU
0	1	A2-G06-27 -SBOSTA(1)	C2-G07-08 -CVB1(6)	BO.EQ.CL
0	2	A2-G06-30 -SBOSTA(2)	C2-G08-08 -CVB2(6)	BO.GT.CU
0	3	A2-G06-33 -SBOSTA(3)	C2-G09-08 -CVB3(6)	BO.GT.CL
0	4	A2-G02-23 -SBOSTA(4)	C2-H06-33 -CVB4(6)	BO.EQ.C
0	5	A2-G02-27 -SBOSTA(5)	C2-H07-33 -CVB5(6)	BO.GT.C
0	6	A2-G02-30 -SBOSTA(6)	C2-H08-33 -CVB6(6)	BO.NG
		SBU 4.1-02	CON 4.3-00	
1	0	A2-G09-23 -SB1STA(0)	C2-G06-05 -CVB0(7)	B1.EQ.CU
1	1	A2-G09-27 -SB1STA(1)	C2-G07-05 -CVB1(7)	B1.EQ.CL
1	2	A2-G09-30 -SB1STA(2)	C2-G08-05 -CVB2(7)	B1.GT.CU
1	3	A2-G09-33 -SB1STA(3)	C2-G09-05 -CVB3(7)	B1.GT.CL
1	4	A2-G13-23 -SB1STA(4)	C2-H06-35 -CVB4(7)	B1.EQ.C
1	5	A2-G13-27 -SB1STA(5)	C2-H07-35 -CVB5(7)	B1.GT.C
1	6	A2-G13-30 -SB1STA(6)	C2-H08-35 -CVB6(7)	B1.NG

DATA MEMORY	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
		DMU 4.0-01	CON 4.3-00	
0	0	B2-C03-23 -DMOSTS(0)	C2-G06-35 -CVB0(8)	DO.EQ.CA
0	1	B2-C03-27 -DMOSTS(1)	C2-G07-35 -CVB1(8)	DO.GT.CA
0	2	B2-C01-23 -DMOSTS(2)	C2-G08-35 -CVB2(8)	DO.EQ.CD
0	3	B2-C02-23 -DMOSTS(3)	C2-G09-35 -CVB3(8)	DO.EQ.CDU
0	4	B2-C02-27 -DMOSTS(4)	C2-H06-05 -CVB4(8)	DO.EQ.CDL
0	5	B2-C02-30 -DMOSTS(5)	C2-H07-05 -CVB5(8)	DO.GT.CDU
0	6	B2-C02-33 -DMOSTS(6)	C2-H08-05 -CVB6(8)	DO.GT.COL
0	7	B2-C03-22 -DMOSTS(7)	C2-H09-05 -CVB7(8)	DO.NG
0	8	B2-C01-27 -DMOSTS(8)	C2-H06-49 -CVB4(14)	DO.GT.CD
		DMU 4.1-01	CON 4.3-00	
1	0	B2-D03-23 -DM1STS(0)	C2-G06-33 -CVB0(9)	D1.EQ.CA
1	1	B2-D03-27 -DM1STS(1)	C2-G07-33 -CVB1(9)	D1.GT.CA
1	2	B2-D01-23 -DM1STS(2)	C2-G08-33 -CVB2(9)	D1.EQ.CD
1	3	B2-D02-23 -DM1STS(3)	C2-G09-33 -CVB3(9)	D1.EQ.CDU
1	4	B2-D02-27 -DM1STS(4)	C2-H06-08 -CVB4(9)	D1.EQ.CDL
1	5	B2-D02-30 -DM1STS(5)	C2-H07-08 -CVB5(9)	D1.GT.CDU
1	6	B2-D02-33 -DM1STS(6)	C2-H08-08 -CVB6(9)	D1.GT.CDL
1	7	B2-D03-22 -DM1STS(7)	C2-H09-08 -CVB7(9)	D1.NG
1	8	B2-D01-27 -DM1STS(8)	C2-H07-49 -CVB5(14)	D1.GT.CD
		DMU 4.2-01	CON 4.3-00	
2	0	B2-A13-23 -DM2STS(0)	C2-G06-32 -CVB0(10)	D2.EQ.CA
2	1	B2-A13-27 -DM2STS(1)	C2-G07-32 -CVB1(10)	D2.GT.CA
2	2	B2-A15-23 -DM2STS(2)	C2-G08-32 -CVB2(10)	D2.EQ.CD
2	3	B2-A14-23 -DM2STS(3)	C2-G09-32 -CVB3(10)	D2.EQ.CDU
2	4	B2-A14-27 -DM2STS(4)	C2-H06-06 -CVB4(10)	D2.EQ.CDL
2	5	B2-A14-30 -DM2STS(5)	C2-H07-06 -CVB5(10)	D2.GT.CDU
2	6	B2-A14-33 -DM2STS(6)	C2-H08-06 -CVB6(10)	D2.GT.CDL
2	7	B2-A13-22 -DM2STS(7)	C2-H09-06 -CVB7(10)	D2.NG
2	8	B2-A15-27 -DM2STS(8)	C2-H08-49 -CVB6(14)	D2.GT.CD
		DMU 4.3-01	CON 4.3-00	
3	0	B2-D13-23 -DM3STS(0)	C2-G06-29 -CVB0(11)	D3.EQ.CA
3	1	B2-D13-27 -DM3STS(1)	C2-G07-29 -CVB1(11)	D3.GT.CA
3	2	B2-D14-23 -DM3STS(2)	C2-G08-29 -CVB2(11)	D3.EQ.CD
3	3	B2-D14-23 -DM3STS(3)	C2-G09-29 -CVB3(11)	D3.EQ.CDU
3	4	B2-D14-27 -DM3STS(4)	C2-H06-07 -CVB4(11)	D3.EQ.CDL
3	5	B2-D14-30 -DM3STS(5)	C2-H07-07 -CVB5(11)	D3.GT.CDU
3	6	B2-D14-33 -DM3STS(6)	C2-H08-07 -CVB6(11)	D3.GT.CDL
3	7	B2-D13-22 -DM3STS(7)	C2-H09-07 -CVB7(11)	D3.NG
3	8	B2-D14-27 -DM3STS(8)	C2-H09-49 -CVB8(14)	D3.GT.CD

FLOATING POINT	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
		FPU 4.0-	CON 4.3-00	
		OVFFL	C2-H07-17 -CVB5(0)	FP.OV
		UNFFL	C2-H08-17 -CVB6(0)	FP.UN
		INOFL	C2-H09-17 -CVB7(0)	FP.IND
		ACOMFL	C2-H08-19 -CVB6(2)	FA.ANY
		MCOMFL	C2-H09-19 -CVB7(2)	FM.ANY
		DCOMFL	C2-H09-33 -CVB7(6)	FD.ANY
		COMFL	C2-H09-35 -CVB7(7)	FS.ANY
		DFOUNR	C2-H09-52 -CVB7(12)	FP.DIVF
		AAGTBL	C2-H09-45 -CVB7(13)	FA.GT
		AAEQB	C2-G08-21 -CVB2(14)	FA.EQ
		AALTB	C2-G09-21 -CVB3(14)	FA.LT

XMAU	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
		XMA 4.0-03	CON 4.3-00	
0		D2-G10-21 -XOAEQC	C2-G06-22 -CVB0(12)	XO.EQ.CA
0		D2-G10-22 -XOAGTC	C2-G07-22 -CVB1(12)	XO.GT.CA
0		D2-G10-51 -XOMSBU	C2-G08-22 -CVB2(12)	XO.NGU
0		D2-G10-47 -XOMSBL	C2-G09-22 -CVB3(12)	XO.NGL
		XMA4.10-03	CON 4.3-00	
0		D2/E1-C17-11 -XODRFC	C2-H06-52 -CVB4(12)	XO.DRF
0		D2/E1-D08-14 -XOOBFC	C2-H07-52 -CVB5(12)	XO.DBF
0		D2/E1-D08-08 -XORSFC	C2-H08-52 -CVB6(12)	XO.RSF
		XMA 4.0-03	CON 4.3-00	
1		D2-G10-06 -X1AEQC	C2-G06-19 -CVB0(13)	X1.EQ.CA
1		D2-G10-04 -X1AGTC	C2-G07-19 -CVB1(13)	X1.GT.CA
1		D2-G10-49 -X1MSBU	C2-G08-19 -CVB2(13)	X1.NGU
1		D2-G10-45 -X1MSBL	C2-G09-19 -CVB3(13)	X1.NGL
		XMA 4.11-03	CON 4.3-00	
1		D2/E2-B04-07 -X1DRFC	C2-H06-45 -CVB4(13)	X1.DRF
1		D2/E2-C02-14 -X1OBFC	C2-H07-45 -CVB5(13)	X1.OBF
1		D2/E2-C02-16 -X1RSFC	C2-H08-45 -CVB6(13)	X1.RSF

EQUIPM. SWITCH	STATUS BIT	FROM NAME	TO NAME	CONDITION IF TRUE
1	0	P10- 1 HWCSO(0)	C2-G06-17 -CVB0(15)	EQUIP
2	1	P10- 3 HWCSO(1)	C2-G07-17 -CVB1(15)	
3	2	P10- 5 HWCSO(2)	C2-G08-17 -CVB2(15)	
4	3	P10- 7 HWCSO(3)	C2-G09-17 -CVB3(15)	
5	4	P10- 9 HWCSO(4)	C2-H06-48 -CVB4(15)	
6	5	P10-11 HWCSO(5)	C2-H07-48 -CVB5(15)	
7	6	P10-13 HWCSO(6)	C2-H08-48 -CVB6(15)	
8	7	P10-15 HWCSO(7)	C2-H09-48 -CVB7(15)	

C2N 4.5-04 (C2/B1-E14/A-08) [-INTPRS/CVB2(0)] -(2)
RPU 4.0-22 (B2/J1-C07-14) [-SKFULL] -(3)
C2N 4.4-00 (C2-A15-27) [-STKEMP] -(4)
FPC 4.0-03 (C3-A01) -(0-10) -(2,1,3) -(5,6,7)
RPU 4.0-01 (B2-H10-28) [-ØFFULO] -(0)
RPU 4.2-01 (B2/F2-C10/A-11) [-STRGØ] -(3)
RPU 4.0-21 (B2/J1-D07-12) [-ANYC2M/ -ANYCMP] -(1)
RPU 4.0-21 (B2/J1-D07-16) [-ALCMP] -(2)
RPU 4.1-01 (B2-H07-28) [-ØFFUL1] -(4)
RPU 4.2-01 (B2/F2-C06/A-11) [-STRG1] -(7)
RPU 4.1-21 (B2/J2-D07-12) [-ANYCM1] -(5)
RPU 4.1-21 (B2/J2-D07-16) [-ALCMP1] -(6)
MUL 4.0-08 STATUS RGTR (A2-A15/E15) -MULT STATUS
ADD 4.0-02 STATUS RGTR (D2-H02/B,H03/B,F01/B) -ADD UNIT 0 STATUS BITS
ADD 4.1-02 STATUS RGTR (D2-H06/B,H07/B,F05/B) -ADD UNIT 1 STATUS BITS
SBU 4.0-02 STATUS AND ØUTPUT RGTRS (A2-G02,G06) [-SBOSTA(0-6)]
SBU 4.1-02 STATUS AND ØUTPUT RGTRS (A2-G13,G09) [-SBISTA(0-6)]
DMU 4.0-01 (B2-C03/B-22) [-DMOSTS(7)] -DATA MEM 0 STATUS [-DMOSTS(0-6,8)]
DMU 4.0-01 DATA MEM 0 STATUS RGTR (B2-C01/A→C02/A)
DMU 4.1-01 (B2-D03/B-22) [-DM1STS(7)] -DATA MEM 1 STATUS [-DM1STS(0-6,8)]
DMU 4.1-01 DATA MEM 1 STATUS RGTR (B2-D01/A→D03/A)
DMU 4.2-01 (B2-A13/B-22) [-DM2STS(7)] -DATA MEM 2 STATUS [-DM2STS(0-6,8)]
DMU 4.2-01 DATA MEM 2 STATUS RGTR (B2-A14/A→A15/A)
DMU 4.3-01 (B2-D13/B-22) [-DM3STS(7)] -DATA MEM 3 STATUS [-DM3STS(0-6,8)]
DMU 4.3-01 DATA MEM 3 STATUS RGTR (B2-C14/A→D14/A)
XMA 4.0-03 (D2-G10) [-CVB(0-3)12] -(0-3)
XMA 4.10-03 (D2/E1-C17-11) [-XØDRFC/CVB4-12] -(4)
XMA 4.10-03 (D2/E1-D08-14) [-XØØBFC/CVB5-12] -(5)
XMA 4.10-03 (D2/E1-D08-08) [-XØRSFC/CVB6-12] -(6)
XMA 4.0-03 (D2-G10) [-CVB(0-3)13] -(0-3)
XMA 4.11-03 (D2/E2-B04-07) [-X1DRFC/CVB4-13] -(4)
XMA 4.11-03 (D2/E2-C02-14) [-X1ØBFC/CVB5-13] -(5)
XMA 4.11-03 (D2/E2-C02-16) [-X1RSFC/CVB6-13] -(6)
FGU 4.0-01 G FILE DATA ØUTPUT RGTR (A2-H15/A-23,27) -F STAT G STAT [-FSTAT(0)/CVB0(14)] [-GSTAT(0)/CVB1(14)]
C0N 4.6-00 A1(REAR)-SW1

C2N 4.4-00 (C2-D12) [-CF0(8-11)]
C2N 4.4-00 (C2-D13) [-CF1(8-11)]
C2N 4.4-00 (C2-D14) [-CF2(8-11)]
C2N 4.4-00 (C2-D15) [-CF3(8-11)]
C2N 4.4-00 (C2-D12) [-NCF0(8-11)]
C2N 4.4-00 (C2-D13) [-NCF1(8-11)]
C2N 4.4-00 (C2-D14) [-NCF2(8-11)]
C2N 4.4-00 (C2-D15) [-NCF3(8-11)]

BITS (0-3)/4-7

[-CVB(0-7)(0)] DI(0/15)
[-CVB(0-7)(1)] DI(1/14)
[-CVB(0-7)(2)] DI(2/13)
[-CVB(0-7)(3)] DI(3/12)
[-CVB(0-7)(4)] DI(4/11)
[-CVB(0-7)(5)] DI(5/10)
[-CVB(0-7)(6)] DI(6/9)
[-CVB(0-7)(7)] DI(7/8)
[-CVB(0-7)(8)] DI(8/7)
[-CVB(0-7)(9)] DI(9/6)
[-CVB(0-7)(10)] DI(10/5)
[-CVB(0-7)(11)] DI(11/4)
[-CVB(0-7)(12)] DI(12/3)
[-CVB(0-7)(13)] DI(13/2)
[-CVB(0-7)(14)] DI(14/1)
[-CVB(0-7)(15)] DI(15/0)

CONDITION VECTOR STAGE 1

12DA GC6/8A49 BIT 0
12DA GC7/8A50 BIT 1
12DA GC8/8A51 BIT 2
12DA GC9/8A52 BIT 3
12DA HC6/8A53 BIT 4
12DA HC7/8A54 BIT 5
12DA HC8/8A55 BIT 6
12DA HC9/8A56 BIT 7

S0(0-3) 18,15,20,16
S1(0-3) 26,23,28,27
S2(0-3) 37,38,34,36
S3(0-3) 11,9,10,12
S4(0-3) 3,46,2,51
S5(0-3) 42,41,43,44
DI(0-15) 48,49,45,52, 7,6,8,5, 35,33,32,29, 22,19,21,17

X→Y A15 A00 / B15 B00 / C15 C00 / D15 D00 / E15 E00 / F15 F00
MUX A,B,C,D,E,F
24 DØ(0) 25 DØ(1) 30 DØ(2) 04 DØ(3) 01 DØ(4) 50 DØ(5)
0 03

[-CFOSELVEC(0-7)] C2N 4.0-01 (C2-F03,F04)
[-CF1SELVEC(0-7)] C2N 4.0-01 (C2-F03,F04)
[-CFOSELVEC(0-7)]
[-CF1SELVEC(0-7)]
[-CF2SELVEC(0-7)]
[-CF3SELVEC(0-7)]

C2 PANEL

A2 PANEL

C2N 4.5-31 (C2/C2-E05-03) [-NINTR(0)]

121HB A A02/A02
CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35
12112
20 T1(0) 19 T2(0) 22 F1(0) 21 F2(0) 25 T1(1) 26 T2(1) 23 F1(1) 24 F2(1) 27 T1(2) 28 T2(2) 29 F1(2) 30 F2(2) 34 T1(3) 33 T2(3) 32 F1(3) 31 F2(3)
1 02

+INTERRUPT
[-NINTR(0)] MUL 4.0-08 C2MPARE LØWER (A2-A04/B-10)
[-NINTR(4)] MUL 4.0-07 A ØPERAND (A2-E10/B,E11/B-10)
[-NINTR(1)] MUL 4.0-08 ØUTPUT RGTR LØWER (A2-A06/B-10)
[-NINTR(5)] MUL 4.0-07 B ØPERAND 2 (A2-D01/B,D02/B-10)
[-NINTR(2)] MUL 4.0-06 AH (A2-A11-10)
[-NINTR(6)] MUL 4.0-08 C2MPARE UPPER (A2-E08/A,E09/A-10)
[-NINTR(3)] MUL 4.0-08 C2MPARE LØWER (A2-E04/A-10)
[-NINTR(7)] MUL 4.0-08 STATUS RGTR (A2-A15-10)
MUL 4.0-06 BH (A2-A13/A-10)

C2N 4.5-31 (C2/C2-E09-14) [-NINTR(28)]

121HB A H10/H10
CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35
12112
20 T1(0) 19 T2(0) 22 F1(0) 21 F2(0) 25 T1(1) 26 T2(1) 23 F1(1) 24 F2(1) 27 T1(2) 28 T2(2) 29 F1(2) 30 F2(2) 34 T1(3) 33 T2(3) 32 F1(3) 31 F2(3)
1 02

[-NINTR(8)] SBU 4.0-02 STATUS AND ØUTPUT RGTRS (A2-G02-10)
[-NINTR(12)] SBU 4.0-03 CØNTRØL REGISTER (A2-J02/A-10)
[-NINTR(9)] SBU 4.1-02 STATUS AND ØUTPUT RGTRS (A2-G09-10)
[-NINTR(13)] FGU 4.0-00 FILE CØNTRØL (A2-H08-10)
[-NINTR(10)] SBU 4.0-00 SHIFT ØPERAND (A2-K05-10)
[-NINTR(14)] SBU 4.0-00 DØUBLE SHIFT RGTR (A2-K04,K03/A-10)
[-NINTR(11)] SBU 4.1-00 SHIFT ØPERAND (A2-K11-10)
[-NINTR(15)] SBU 4.1-03 CØNTRØL REGISTER (A2-K09/A-10)
SBU 4.0-00 SHIFT ØPERAND (A2-K06/A-10)
SBU 4.0-03 CØNTRØL REGISTER (A2-K07/A-10)
FGU 4.0-01 F FILE DATA ØUTPUT RGTR (A2-K08-10)
SBU 4.1-00 DØUBLE SHIFT RGTR (A2-K12-10)
SBU 4.1-03 CØNTRØL RGTR (A2-K14/A-10)
SBU 4.0-02 STATUS AND ØUTPUT RGTRS (A2-G06-10)
SBU 4.0-03 CØNTRØL RGTR (A2-G07/A-10)
SBU 4.1-03 CØNTRØL RGTR (A2-G08/A-10)
SBU 4.1-02 STATUS AND ØUTPUT RGTRS (A2-G13-10)
FGU 4.0-00 FILE CØNTRØL (A2-H14-10)

C2N 4.4-00 (C2-D05) [-CF0(5-7)]
C2N 4.4-00 (C2-D06) [-CF1(5-7)]
C2N 4.4-00 (C2-D10) [-CF2(5-7)]
C2N 4.4-00 (C2-D11) [-CF3(5-7)]

CONDITION VECTOR STAGE 2

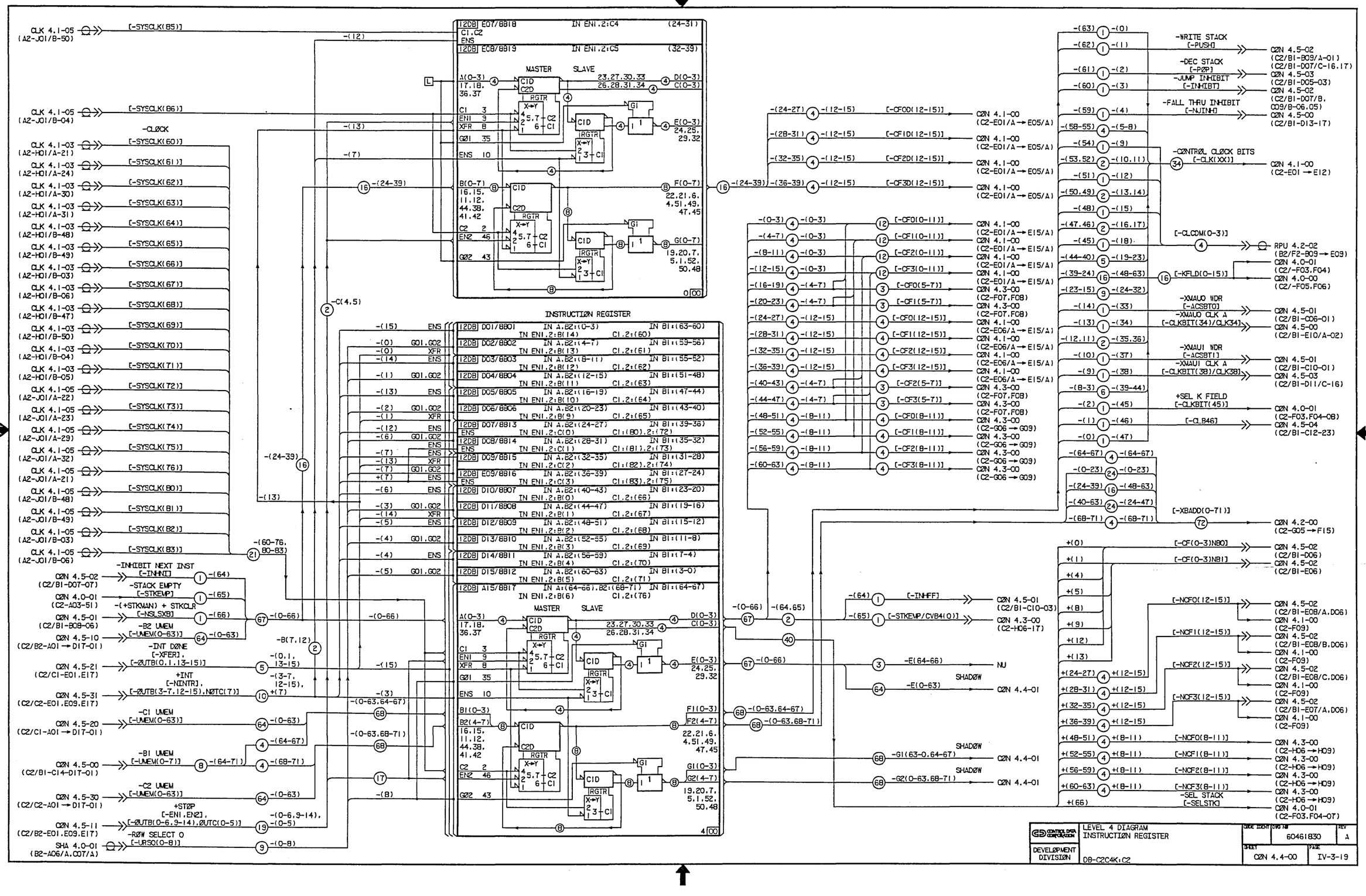
12DA FC7/8A57 BITS 0,1
SO
S1
12DA FC8/HA58 BITS 2,3
S0(0-3) 18,15,20,16
S1(0-3) 26,23,28,27
S2(0-3) 37,38,34,36
S3(0-3) 11,9,10,12
S4(0-3) 3,46,2,51
S5(0-3) 42,41,43,44
DI(0-15) 48,49,45,52, 7,6,8,5, 35,33,32,29, 22,19,21,17

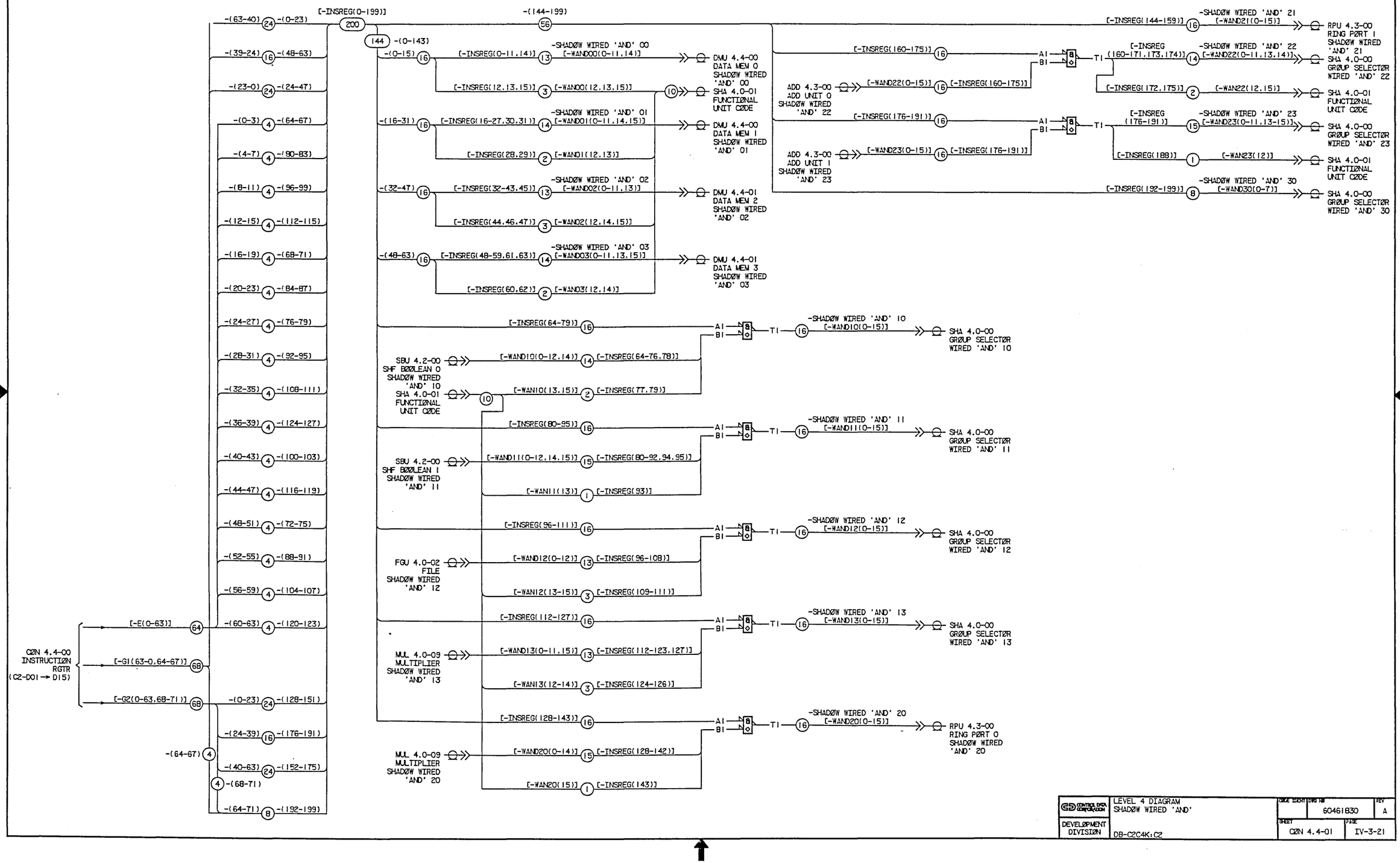
X→Y A15 A00 / B15 B00 / C15 C00 / D15 D00 / E15 E00 / F15 F00
MUX A,B,C,D,E,F
24 DØ(0) 25 DØ(1) 30 DØ(2) 04 DØ(3) 01 DØ(4) 50 DØ(5)
0 03

[-CF0,CF1,CF2,CF3] 32

[-JUMPB(0-3)] C2N 4.5-02 (C2/B1-E06-02,01,22,19)

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM CØNDITIØN VECTØR	CODE IDENT DWG NO 60461830	REV A
DEVELOPMENT DIVISION	DB-A2MUL:A2 DB-C2C4K:C2	SHEET C2N 4.3-00	PAGE IV-3-17


INSTRUCTIØN REGISTER
MASTER
SLAVE
-WRITE STACK [-PUSH]
-DEC STACK [-P⌀P]
-JUMP INHIBIT [-INHIBT]
-FALL THRU INHIBIT [-NJINH]
-CØNTRØL CLØCK BITS [-CLK(XX)]
[-CLCDM(0-3)]
-XMAUØ WDR [-ACSBTØ]
-XMAUØ CLK A [-CLKBIT(34)/CLK34]
-XMAU1 WDR [-ACSBT1]
-XMAU1 CLK A [-CLKBIT(38)/CLK38]
+SEL K FIELD [-CLKBIT(45)]
[-CLB46]
[-XBADD(0-7)]
-SEL STACK [-SELSTK]
SHADØW
LEVEL 4 DIAGRAM
INSTRUCTIØN REGISTER
DB-C2C4K:C2
DEVELOPMENT DIVISIØN
60461830
CØN 4.4-00
IV-3-19


[-INSREG(0-199)]
-(144-199)
-(63-40) 24 -(0-23)
200
56
144 -(0-143)
-(39-24) 16 -(48-63)
-(23-0) 24 -(24-47)
-(0-3) 4 -(64-67)
-(4-7) 4 -(90-83)
-(8-11) 4 -(96-99)
-(12-15) 4 -(112-115)
-(16-19) 4 -(68-71)
-(20-23) 4 -(84-87)
-(24-27) 4 -(76-79)
-(28-31) 4 -(92-95)
-(32-35) 4 -(108-111)
-(36-39) 4 -(124-127)
-(40-43) 4 -(100-103)
-(44-47) 4 -(116-119)
-(48-51) 4 -(72-75)
-(52-55) 4 -(88-91)
-(56-59) 4 -(104-107)
-(60-63) 4 -(120-123)
-(0-15) 16 [-INSREG(0-11,14)] 13 -SHADØW WIRED 'AND' 00 [-WAND00(0-11,14)]
DMU 4.4-00 DATA MEM 0 SHADØW WIRED 'AND' 00
[-INSREG(12,13,15)] 3 [-WAN00(12,13,15)] 10
SHA 4.0-01 FUNCTIØNAL UNIT CØDE
-(16-31) 16 [-INSREG(16-27,30,31)] 14 -SHADØW WIRED 'AND' 01 [-WAND01(0-11,14,15)]
DMU 4.4-00 DATA MEM 1 SHADØW WIRED 'AND' 01
[-INSREG(28,29)] 2 [-WAN01(12,13)]
-(32-47) 16 [-INSREG(32-43,45)] 13 -SHADØW WIRED 'AND' 02 [-WAND02(0-11,13)]
DMU 4.4-01 DATA MEM 2 SHADØW WIRED 'AND' 02
[-INSREG(44,46,47)] 3 [-WAN02(12,14,15)]
-(48-63) 16 [-INSREG(48-59,61,63)] 14 -SHADØW WIRED 'AND' 03 [-WAND03(0-11,13,15)]
DMU 4.4-01 DATA MEM 3 SHADØW WIRED 'AND' 03
[-INSREG(60,62)] 2 [-WAN03(12,14)]
[-INSREG(64-79)] 16
SBU 4.2-00 SHF BØØLEAN 0 SHADØW WIRED 'AND' 10
[-WAND10(0-12,14)] 14 [-INSREG(64-76,78)]
SHA 4.0-01 FUNCTIØNAL UNIT CØDE
10 [-WAN10(13,15)] 2 [-INSREG(77,79)]
[-INSREG(80-95)] 16
SBU 4.2-00 SHF BØØLEAN 1 SHADØW WIRED 'AND' 11
[-WAND11(0-12,14,15)] 15 [-INSREG(80-92,94,95)]
[-WAN11(13)] 1 [-INSREG(93)]
[-INSREG(96-111)] 16
FGU 4.0-02 FILE SHADØW WIRED 'AND' 12
[-WAND12(0-12)] 13 [-INSREG(96-108)]
[-WAN12(13-15)] 3 [-INSREG(109-111)]
[-INSREG(112-127)] 16
MUL 4.0-09 MULTIPLIER SHADØW WIRED 'AND' 13
[-WAND13(0-11,15)] 13 [-INSREG(112-123,127)]
[-WAN13(12-14)] 3 [-INSREG(124-126)]
[-INSREG(128-143)] 16
MUL 4.0-09 MULTIPLIER SHADØW WIRED 'AND' 20
[-WAND20(0-14)] 15 [-INSREG(128-142)]
[-WAN20(15)] 1 [-INSREG(143)]
A I
B I
8
T I
-SHADØW WIRED 'AND' 10 [-WAND10(0-15)] 16
SHA 4.0-00 GRØUP SELECTØR WIRED 'AND' 10
-SHADØW WIRED 'AND' 11 [-WAND11(0-15)] 16
SHA 4.0-00 GRØUP SELECTØR WIRED 'AND' 11
-SHADØW WIRED 'AND' 12 [-WAND12(0-15)] 16
SHA 4.0-00 GRØUP SELECTØR WIRED 'AND' 12
-SHADØW WIRED 'AND' 13 [-WAND13(0-15)] 16
SHA 4.0-00 GRØUP SELECTØR WIRED 'AND' 13
-SHADØW WIRED 'AND' 20 [-WAND20(0-15)] 16
RPU 4.3-00 RING PØRT 0 SHADØW WIRED 'AND' 20
[-INSREG(160-175)] 16
ADD 4.3-00 ADD UNIT 0 SHADØW WIRED 'AND' 22
[-WAND22(0-15)] 16 [-INSREG(160-175)]
[-INSREG(176-191)] 16
ADD 4.3-00 ADD UNIT 1 SHADØW WIRED 'AND' 23
[-WAND23(0-15)] 16 [-INSREG(176-191)]
[-INSREG(144-159)] 16
-SHADØW WIRED 'AND' 21 [-WAND21(0-15)]
RPU 4.3-00 RING PØRT 1 SHADØW WIRED 'AND' 21
[-INSREG(160-171,173,174)] 14
-SHADØW WIRED 'AND' 22 [-WAND22(0-11,13,14)]
SHA 4.0-00 GRØUP SELECTØR WIRED 'AND' 22
[-INSREG(172,175)] 2 [-WAN22(12,15)]
SHA 4.0-01 FUNCTIØNAL UNIT CØDE
[-INSREG(176-191)]
[-INSREG(176-187)] 15
-SHADØW WIRED 'AND' 23 [-WAND23(0-11,13-15)]
SHA 4.0-00 GRØUP SELECTØR WIRED 'AND' 23
[-INSREG(188)] 1 [-WAN23(12)]
SHA 4.0-01 FUNCTIØNAL UNIT CØDE
[-INSREG(192-199)] 8
-SHADØW WIRED 'AND' 30 [-WAND30(0-7)]
SHA 4.0-00 GRØUP SELECTØR WIRED 'AND' 30
CØN 4.4-00 INSTRUCTIØN RGTR (C2-D01 → D15)
[-E(0-63)] 64
[-G1(63-0,64-67)] 68
[-G2(0-63,68-71)] 68
-(0-23) 24 -(128-151)
-(24-39) 16 -(176-191)
-(64-67) 4
-(40-63) 24 -(152-175)
4 -(68-71)
-(64-71) 8 -(192-199)

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM SHADØW WIRED 'AND'	CODE IDENT / DWG NO	REV
		60461830	A
DEVELOPMENT DIVISION	DB-C2C4K,C2	SHEET CØN 4.4-01	PAGE IV-3-21

NOTES:

1

BIT	AUX	LSI
0	13-2	C2-B14-2
1	13-5	C2-B14-5
2	13-4	C2-B14-4
3	13-3	C2-B14-3
4	13-8	C2-B14-8
5	13-9	C2-B14-9
6	13-10	C2-B14-10
7	13-15	C2-B14-15
8	12-3	C2-B13-3
9	12-7	C2-B13-7
10	12-4	C2-B13-4
11	12-6	C2-B13-6

2

BIT	AUX	LSI
192	13-6	C2-B14-6
193	13-17	C2-B14-17
194	13-25	C2-B14-25
195	12-8	C2-B13-8
196	13-1	C2-B14-1
197	13-21	C2-B14-21
198	13-26	C2-B14-26
199	12-9	C2-B13-9

3

BIT	AUX	LSI
0	4-16	C2-B05-16
1	4-15	C2-B05-15
2	4-9	C2-B05-9
3	4-7	C2-B05-7
4	4-20	C2-B05-20
5	4-19	C2-B05-19
6	4-21	C2-B05-21
7	4-24	C2-B05-24

4

BIT	AUX	LSI
0	1-16	C2-B02-16
1	1-17	C2-B02-17
2	1-19	C2-B02-19
3	1-20	C2-B02-20
4	2-26	C2-B03-26
5	1-1	C2-B02-1
6	1-4	C2-B02-4
7	1-6	C2-B02-6
8	2-6	C2-B03-6
9	2-7	C2-B03-7
10	2-8	C2-B03-8
11	2-9	C2-B03-9
12	3-7	C2-B04-7
13	3-10	C2-B04-10
14	3-9	C2-B04-9
15	4-25	C2-B05-25

5

BIT	AUX	LSI
0	1-26	C2-B02-26
1	1-25	C2-B02-25
2	1-24	C2-B02-24
3	1-21	C2-B02-21
4	1-15	C2-B02-15
5	1-10	C2-B02-10
6	1-9	C2-B02-9
7	1-8	C2-B02-8
8	2-15	C2-B03-15
9	2-10	C2-B03-10
10	2-17	C2-B03-17
11	2-16	C2-B03-16
12	3-19	C2-B04-19
13	3-15	C2-B04-15
14	3-17	C2-B04-17
15	3-21	C2-B04-21

6

BIT	TP	BIT	TP
0	-	6	114
1	-	7	116
2	118	8	104
3	120	9	102
4	106	10	110
5	108	11	112

7

BIT	AUX	LSI
192	13-7	C2-B14-07
193	13-19	C2-B14-09
194	13-24	C2-B14-24
195	12-25	C2-B13-25
196	13-16	C2-B14-16
197	13-20	C2-B14-20
198	12-1	C2-B13-01
199	12-26	C2-B13-26

8

BIT	A	T1	T2	F1	F2
0	19	17	18	16	15
1	20	11	12	13	14
2	23	7	8	6	5
3	24	1	2	3	4

AUX BØARD MEMØRY BIT XX-XXX	HØLDS INST RGTR BIT YYY	USE
BI - 192 ↓ 195 196 ↓ BI - 199	192 ↓ 195 196 ↓ 199	XBAR

9 MAKE FØIL FRØM D13-12 TØ E12-16 AS CLØSE TØ 4 INCHES AS IS PØSSIBLE. FØIL TERMINATES AT D10-05.

INSTRUCTIØN MEMØRY

12470 C17/C17 BIT 192
12470 C16/C16 193
12470 C15/C15 194
12470 C14/C14 195
12470 D17/D17 196
12470 D16/D16 197
12470 D15/D15 198
12470 D14/D14 BIT 199

-WRITE 1
-WRITE 2
-(0) … -(11)
X↔Y
2 2048
3 1024
4 512
5 256
6 128
7 64 A4095
8 32 A0000
10 16
11 8
12 4
13 2
14 1
15
16
&↔C
&↔G
MEM
17 ACD AG

12112 E17/C01 BITS 0-3
12112 E16/C02 4-7
12112 E15/C03 BITS 8-11
A
T1 T2 F1 F2
CX 22 G1

C2N 4.0-00 (C2-A04,A05)
[-PREG(0-11)]
[-PREG(0,1)] (13-18) (C2-B14-18) (13-22) (C2-B14-22)
C2N 4.0-00 (C2-F01-38,42)

XMA 4.0-02 (D2-C04)
[-UMID(192-199)]
-BI UMEM [-UMEM(0-7)]
C2N 4.4-00 (C2-A15)

XMA 4.10-00 (D2/E1-B17-12)
[-UMWE4] (11-10) (C2-B12-10)
-WE PARCEL 4(1)
-WE PARCEL 4(2)
TP83

12102 D13/A53
CX A1 B1 A2 B2 A3 B3 A4 B4 A5 B5
a
T1 F1 T2 F2 T3 F3 T4 F4 T5 F5

C2N 4.4-00 (C2-D02-22)
-FALL THRU INHIBIT [-NJINH] (11-20) (C2-B12-20)
C2N 4.5-04 (C2/B1-C12-15)
+BLØCK WM
XMA 4.0-00 (D2-D11-02)
[-WRUN] (9-3) (C2-B10-3)
C2N 4.5-01 (C2/B1-B12-01)
[-SYCLCK1]
CLK 4.1-00 (A2-K01/B-06)
[-ØFFCLK(2T)] (11-08) (C2-B12-08)

-CØNT CLKE • BLØCK WM
C2N 4.5-01 (C2/B1-C06-18)
-CØNT CLKE • BLØCK WM
C2N 4.5-02 (C2/B1-D07/B,C09/B-04,03)
+SET STACK WRITE
C2N 4.5-04 (C2/B1-C07-02)
9 [-ØFFCLKE]
C2N 4.5-01 (C2/B1-E12/C-16)
C2N 4.5-03 (C2/B1-D10/A-05)
[-SYSCLKE]
C2N 4.5-03 (C2/B1-B10-19)

P-STACK
12145 E01/B20 BITS 0-3
12145 E02/B21 4-7
12145 E03/B22 8-11
12145 E04/B23 BITS 12-15
W3 W2 W1 W0 S3 S2 S1 S0 C1 C2 E1 E2 MS
X↔Y 1A15 1A00
X↔Y 2A15 2A00
G4/C5 G2/C3 G1 R
MEM D T
16,15, 14,13 7,8, 11,12
1AC5D 2A2+1 2A+C3D+1

C2N 4.0-01 (C2-A03)
[-STAKAD(0-7)]
-STACK WRITE ENABLE
C2N 4.5-03 (C2/B1-D05-13)
C2N 4.0-00 (C2-A01,A02)
-STACK WRITE [-STWD(0-15)]
-STACK READ [-STI(0-15)]
C2N 4.0-00 (C2-A04,A05,A11, A12,F03,F04)

READ/WRITE M/M F.F.
12131 E12/A57-A/C
SI DI CI RI
S CD C R
T1 F1
RGTR
MC MS MR GI S R
C2N 4.5-01 (C2/B1-B12-06)
[+SYCLK3]
[+RWMM] C2N 4.5-02 (C2/B1-C04/A-16)
[-RWMM] C2N 4.5-04 (C2/B1-C12-20)
[+RWMM] C2N 4.5-04 (C2/B1-D12/C-18)

12101 D12/A59-B/C
TP70
C2N 4.5-01 (C2/B1-C10-06) +(INHNIFF•STØP2)
C2N 4.5-03 (C2/B1-B07/A-15) +START INT BUF
-BLØCK C2N 4.5-02 (C2/B1-C09/B-22)

12101 C11/A81-A/C
C2N 4.5-04 (C2/B1-C08/A-07) -START INT
-RWMM • START INT C2N 4.5-02 (C2/B1-D07/C-19)
-RWMM • START INT C2N 4.5-04 (C2/B1-B06/B-24)

12101 E10/A87-A/C
C2N 4.4-00 (C2-D12-06)
C2N 4.5-03 (C2/B1-E09/C-14)
-XMAU0 . CLK A [-CLKBIT(34)/CLK34] (9-20) (C2/B1-B10-20) +BLØCK UMEM [-BLØCUM, BLØCUM]
-CLØCK A [-XMØCKB] (9-16) (C2-B10-16)
XMA 4.0-00 (D2-D11-43)

12101 B11/A75A
TP82
C2N 4.5-03 (C2/B1-D09/C-13) -STØP 2
+STØP C2N 4.5-02 (C2/B1-E10/C-17)

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
INSTRUCTIØN MEMØRY (192-199)
DB-C2PMC:C2/B1
CODE IDENT 60461830 REV A
SHEET C2N 4.5-00 PAGE IV-3-23

NØTES:

1. ALL ØUTPUT LINES FRØM B12 MUST MEASURE BETWEEN 5 AND 7 INCHES AT 1 TØ 1.
2. FØIL FRØM B12-16 GØES FIRST TØ B15-20 (SEE NØTE 1). FØIL LENGTH FRØN B15-20 TØ B10-20 MUST BE BETWEEN 11 AND 13 INCHES AT 1 TØ 1.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM	SIZE IDENT DWG NO	60461830 REV E
DEVELOPMENT DIVISION	DB-C2PMC:C2/B1 05-15-86	SHEET C0N 4.5-01	PAGE IV-3-25

<50 60 70 80 90 FULL>

NØTES: 1

BIT	AUX	LSI
0	5-24	C2-B06-24
1	5-20	C2-B06-20
2	5-15	C2-B06-15
3	5-9	C2-B06-9

2

BIT	AUX	LSI
0	5-25	C2-B06-25
1	5-17	C2-B06-17
2	5-16	C2-B06-16
3	5-10	C2-B06-10

3

BIT	AUX	LSI
12	6-4	C2-B07-4
13	6-1	C2-B07-1
14	6-8	C2-B07-8
15	5-19	C2-B06-19

4

BIT	AUX	LSI
12	7-9	C2-B08-9
13	7-20	C2-B08-20
14	7-15	C2-B08-15
15	6-26	C2-B07-26

5

BIT	AUX	LSI
12	7-26	C2-B08-26
13	7-10	C2-B08-10
14	7-6	C2-B08-6
15	6-9	C2-B07-9

6

BIT	AUX	LSI
12	6-3	C2-B07-3
13	6-25	C2-B07-25
14	5-3	C2-B06-3
15	5-6	C2-B06-6

7

BIT	AUX
0	5-21
1	5-26
2	7-3
3	5-7

12107 E06/A98

12101 E08/A08-A/C

12101 E08/A08-B/C

12101 E08/A08-C/C

12102 D06/A10

12101 E07/A09-A/C

12131 E12/A57-B/C

12101 E10/A87-B/C

12131 B06/A70-A/C

12117 C04/A02-A/B

12101 E07/A09-B/C

12101 E07/A09-C/C

12101 E10/A87-C/C

12117 B09/A49-A/B

12117 D07/A46-C/C

12117 D08/A45C-A/B

12117 D07/A46-A/C

12117 D07/A46-B/C

12117 C09/A97-B/C

12131 D09/A55-A/C

C2N 4.3-00 (C2-F07,FC8-24,25)

C2N 4.4-00 (C2-D01 → D04-28)

C2N 4.4-00 (C2-D01 → D04-26)

C2N 4.4-00 (C2-D07)

C2N 4.4-00 (C2-D08)

C2N 4.4-00 (C2-D09)

C2N 4.4-00 (C2-E09)

C2N 4.1-00 (C2-F09-51)

C2N 4.5-03 (C2/BI-B10-11)

C2N 4.1-00 (C2-E01/A-19)

XMA 4.10-03 (D2/E1-C07-04)

C2N 4.5-04 (C2/BI-C12-14)

C2N 4.5-01 (C2/BI-C06-12)

C2N 4.5-01 (C2/BI-C05-05)

C2N 4.5-04 (C2/BI-B06/C-08)

C2N 4.5-01 (C2/BI-B12-14)

C2N 4.5-01 (C2/BI-B12-06)

C2N 4.5-00 (C2/BI-B11-13)

C2N 4.5-01 (C2/BI-C10-15)

C2N 4.5-01 (C2/BI-B15-07)

C2N 4.5-00 (C2/BI-E12/A-07)

C2N 4.5-04 (C2/BI-C08/A-07)

C2N 4.5-04 (C2/BI-B06/B-11)

C2N 4.4-00 (C2-D01-21)

C2N 4.5-03 (C2/BI-B07/C-11)

C2N 4.5-01 (C2/BI-B08-05)

C2N 4.5-01 (C2/BI-D02-15)

C2N 4.5-00 (C2/BI-C11/A-07)

C2N 4.5-03 (C2/BI-D05-16)

C2N 4.5-04 (C2/BI-C12-13)

C2N 4.5-01 (C2/BI-C05-02)

C2N 4.5-03 (C2/BI-D05-15)

C2N 4.5-01 (C2/BI-C06-11)

C2N 4.5-00 (C2/BI-D13-16)

C2N 4.4-00 (C2-D01-04)

C2N 4.5-00 (C2/BI-D12/B-12)

C2N 4.5-01 (C2/BI-B12-04)

C2N 4.5-01 (C2/BI-C06-17)

C2N 4.5-11 (C2/B2-E09-22)

C2N 4.5-01 (C2/BI-D03-02)

C2N 4.0-00 (C2-A01,A02-49)

C2N 4.5-01 (C2/BI-D02-18)

C2N 4.5-01 (C2/BI-B15-06)

C2N 4.0-00 (C2-A04,A05-30)

C2N 4.0-00 (C2-A04,A05-15)

C2N 4.4-00 (C2-A15-17)

C2N 4.5-04 (C2/BI-C07-24)

C2N 4.5-03 (C2/B2-E09/A-04)

-(0) F C2N 4.5-01 (C2/BI-D04)

[-JUMPB(0-3)] 4 -(0)

[-CF(0-3)NB1] 4 -(0) -(1) -(2) -(3)

[-NCF0(12-15)] 4 3 -(12-14)

[-NCF1(12-15)] 4 3 -(12-14)

[-NCF2(12-15)] 4 3 -(12-14)

[-NCF3(12-15)] 4 3 -(12-14)

-LØAD CØNTRØL CØNTRØL RGTR [-GØU(0)] (5-8) (C2-B06-8)

[-CF(0-3)NB0] +(15) -(0) -(1) -(2) -(3)

+FID10

-CØNTRØL DC FIELD(0) [-FID00] (4-26) (C2-B05-26)

A C2N 4.5-01 (C2/BI-C11-B-01)

[-NEXTSP] (7-4) (C2-B08-04) K C2N 4.5-01 (C2/BI-B15-06)

+RWMM EN P

+(START INT + RP LØAD P • STØPPED)

+MC4

-INCR/DECR STACK ADRS

+BLØCK INC

+SYCLCK6

TP14 TP17 TP16 TP15 TP42 TP41 TP38 TP28 TP33 TP34 TP23 TP21 TP6 TP50 TP77 TP36 TP24 TP56 TP19 TP39 TP51 TP46

+JUMP 0 +JUMP 1 +JUMP 2 +JUMP 3

[-SDV47] (4-1) (C2-B05-1)

+STACK MANIPULATIØN

+SYCLCK3

[-RWMM] -START INT -INT INC STACK

-WRITE STACK [-PUSH] (7-1) (C2-B08-1)

-PØP STACK 1 [-CLKC]

-STK MAN • (+STK CLR)

-STACK MANIPULATIØN

-(+RWMM) • START INT

-P SEL=0 • (+START INT)

-RWMM SEL P

-MC2

-(+P SEL=0) + START INT

-START INT

+ (RP LØAD P • STØPPED)

-CØNT CLKE • (+BLØCK MM)

-JUMP INHIBIT [-INHIBT] (5-4) (C2-B06-4)

-BLØCK

+SYCLCK2

[-NSTP] (8-16) (C2-B09-16)

-INCR/DECR STACK ADRS

-WRITE STACK

-INHIBIT NEXT INST [-INHNI] (7-17) (C2-B08-17)

+BLØCK CLØCK

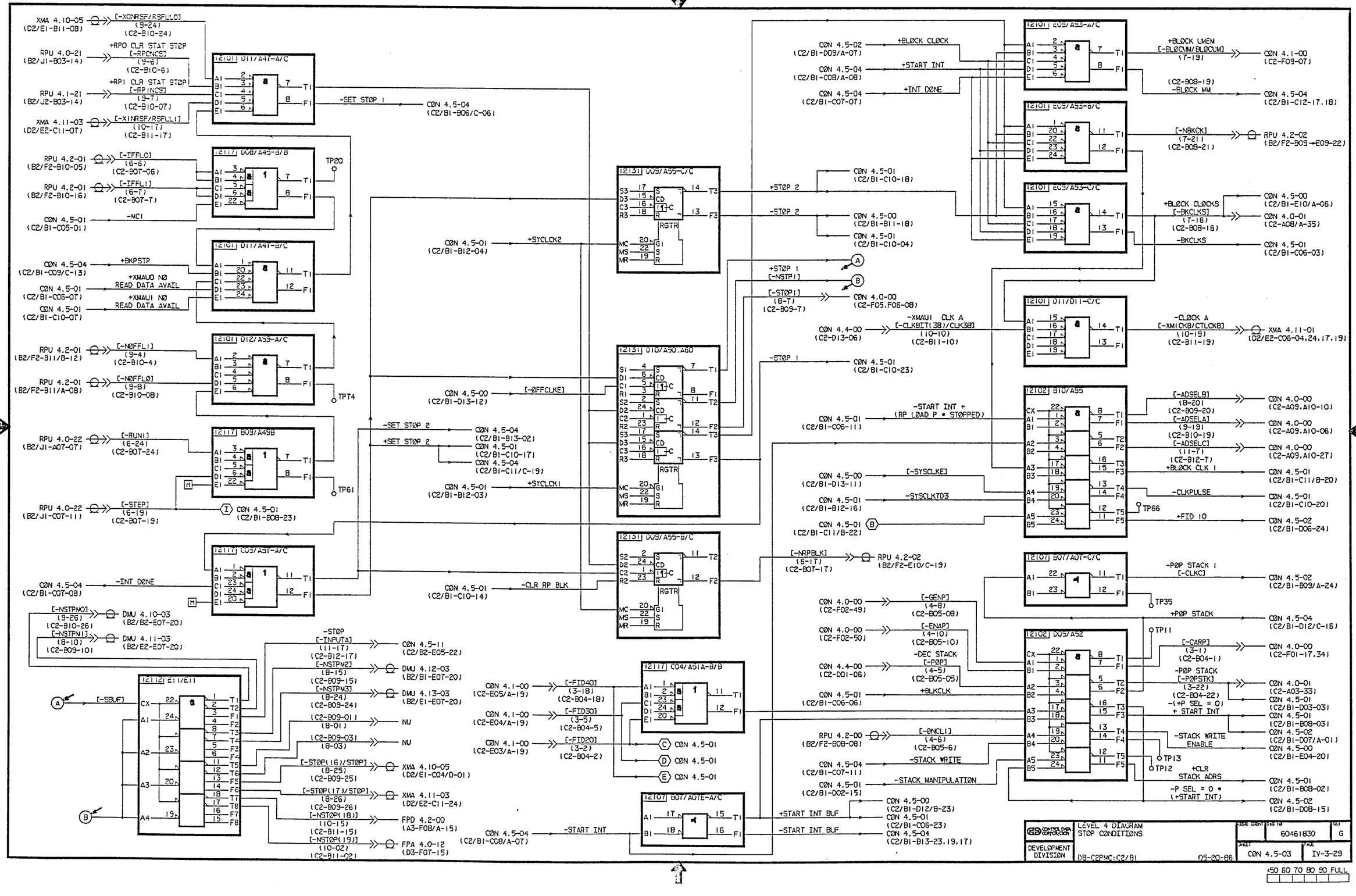
[-PRGV01] (7-7) (C2-B08-7)

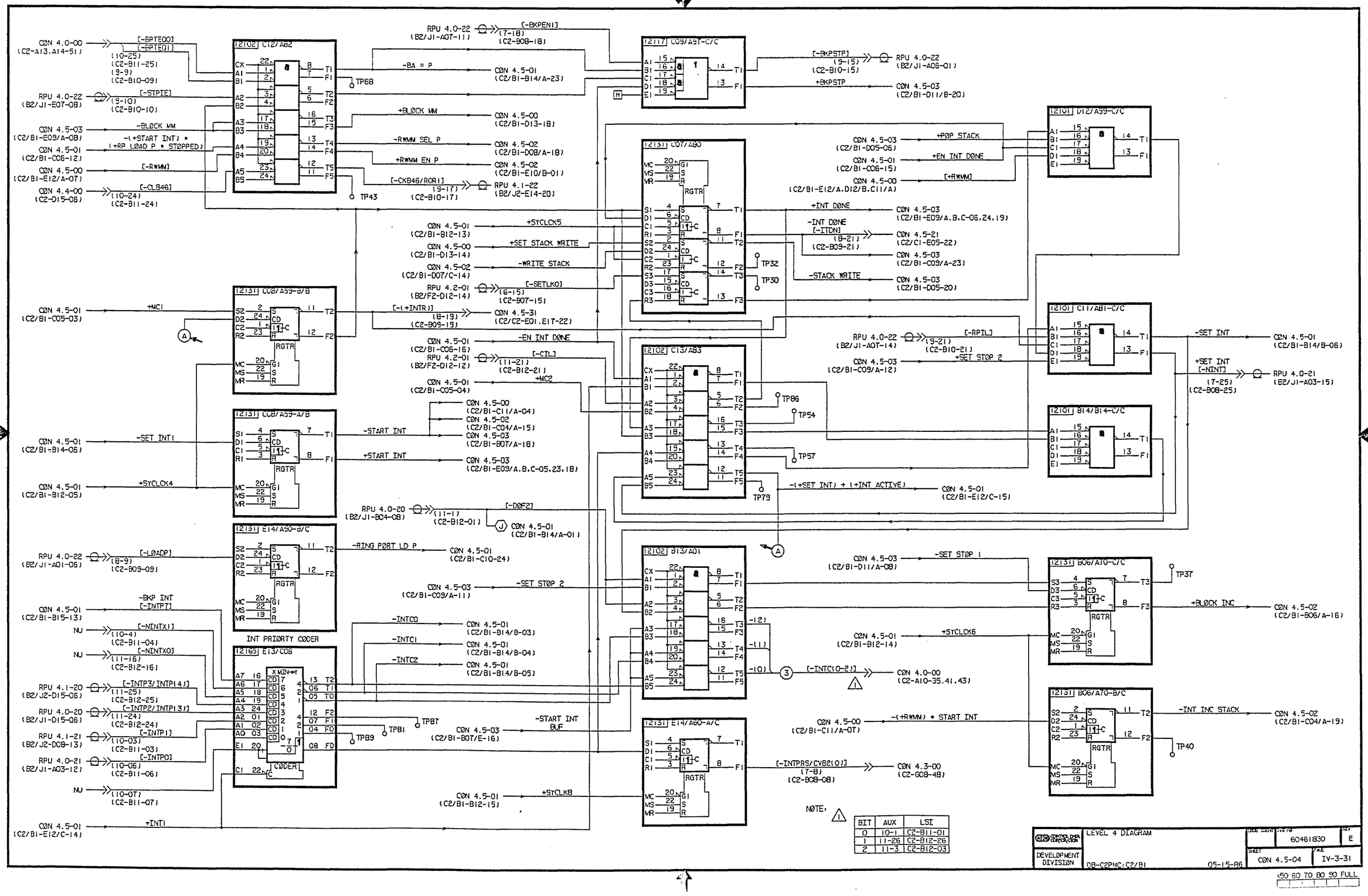
[-PRGV02] (6-21) (C2-B07-21)

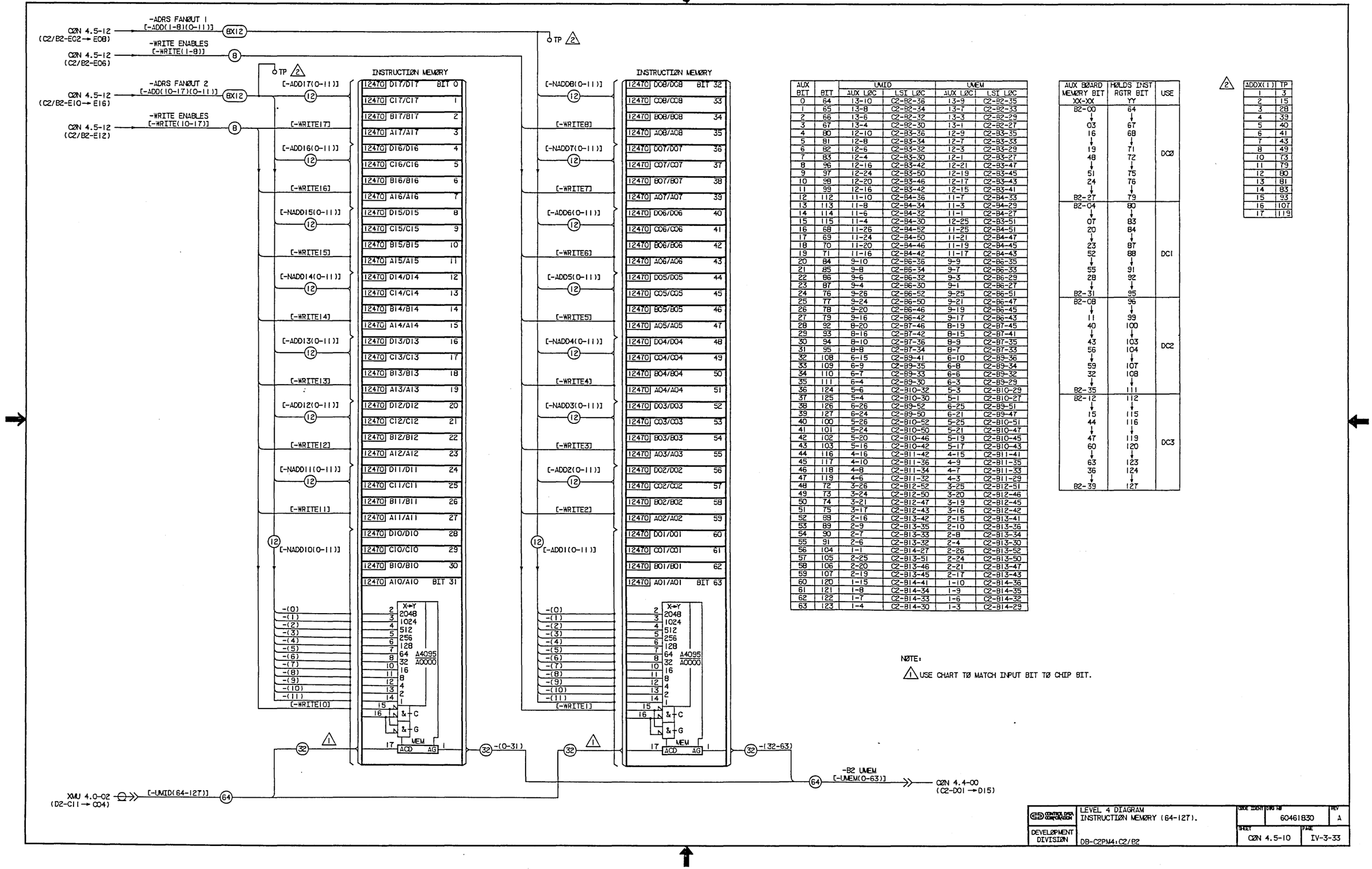
-INC STACK

[-RWMM] -START INT -INT INC STACK

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM BRANCH CØNDITIØN LØGIC	DRAWING NO 60461830	REV A
DEVELOPMENT DIVISION	DB-C2PMC; C2/BI	SHEET C2N 4.5-02	PAGE IV-3-27


XMA 4.10-05 (D2/E1-B11-08)
[-XCNRSF/RSFUL0] (9-24) (C2-B10-24)
RPU 4.0-21 (B2/J1-B03-14)
+RPO CLR STAT STØP [-RPCNCS] (9-6) (C2-B10-6)
RPU 4.1-21 (B2/J2-B03-14)
+RP1 CLR STAT STØP [-RPINCS] (9-7) (C2-B10-07)
XMA 4.11-03 (D2/E2-C11-07)
[-XINRSF/RSFUL1] (10-17) (C2-B11-17)
12101 D11/A47-A/C
-SET STØP 1
C0N 4.5-04 (C2/B1-B06/C-06)
RPU 4.2-01 (B2/F2-B10-05)
[-IFFL0] (6-8) (C2-B07-06)
RPU 4.2-01 (B2/F2-B10-16)
[-IFFL1] (6-7) (C2-B07-7)
C0N 4.5-01 (C2/B1-C05-01)
-MCI
12117 D08/A45-B/B
TP20
C0N 4.5-04 (C2/B1-C09/C-13)
+BKPSTP
C0N 4.5-01 (C2/B1-C06-07)
+XMAU0 NØ READ DATA AVAIL
C0N 4.5-01 (C2/B1-C10-07)
+XMAU1 NØ READ DATA AVAIL
12101 D11/A47-B/C
RPU 4.2-01 (B2/F2-B11/B-12)
[-NØFFL1] (9-4) (C2-B10-4)
RPU 4.2-01 (B2/F2-B11/A-08)
[-NØFFL0] (9-8) (C2-B10-08)
12101 D12/A53-A/C
TP4
RPU 4.0-22 (B2/J1-A07-07)
[-RUN1] (6-24) (C2-B07-24)
12117 B09/A49B
TP61
RPU 4.0-22 (B2/J1-C07-11)
[-STEP] (6-19) (C2-B07-19)
C0N 4.5-01 (C2/B1-B08-23)
12117 C09/A51-A/C
C0N 4.5-04 (C2/B1-C07-08)
-INT DØNE
[-NSTPM0] (9-26) (C2-B10-26)
DMU 4.10-03 (B2/B2-E07-20)
[-NSTPM1] (8-10) (C2-B09-10)
DMU 4.11-03 (B2/E2-E07-20)
12112 E11/E11
[-SBUF]
-STØP [-INPUTA] (11-17) (C2-B12-17)
C0N 4.5-11 (C2/B2-E05-22)
[-NSTPM2] (8-15) (C2-B09-15)
DMU 4.12-03 (B2/B1-E07-20)
[-NSTPM3] (8-24) (C2-B09-24)
DMU 4.13-03 (B2/E1-E07-20)
(C2-B09-01) (8-01)
NU
(C2-B09-03) (8-03)
NU
[-STØP(16)/STØP] (8-25) (C2-B09-25)
XMA 4.10-05 (D2/E1-C04/D-01)
[-STØP(17)/STØP] (8-26) (C2-B09-26)
XMA 4.11-03 (D2/E2-C11-24)
[-NST0P(18)] (10-15) (C2-B11-15)
FPD 4.2-00 (A3-F08/A-15)
[-NST0P(19)] (10-02) (C2-B11-02)
FPA 4.0-12 (D3-F07-15)
C0N 4.5-01 (C2/B1-B12-04)
+SYCLCK2
12131 D09/A55-C/C
+STØP 2
C0N 4.5-01 (C2/B1-C10-18)
-STØP 2
C0N 4.5-00 (C2/B1-B11-18)
C0N 4.5-01 (C2/B1-C10-04)
RGTR
+STØP 1 [-NSTP1]
[-STØP1] (8-7) (C2-B09-7)
C0N 4.0-00 (C2-F05.F06-08)
C0N 4.5-00 (C2/B1-D13-12)
[-0FFCLKE]
12131 D10/A50.A60
-SET STØP 2
C0N 4.5-04 (C2/B1-B13-02)
+SET STØP 2
C0N 4.5-01 (C2/B1-C10-17)
C0N 4.5-04 (C2/B1-C11/C-19)
C0N 4.5-01 (C2/B1-B12-03)
+SYCLCK1
12131 D09/A55-B/C
C0N 4.5-01 (C2/B1-C10-14)
-CLR RP BLK
RGTR
C0N 4.1-00 (C2-E05/A-19)
[-FID40] (3-18) (C2-B04-18)
C0N 4.1-00 (C2-E04/A-19)
[-FID30] (3-5) (C2-B04-5)
C0N 4.1-00 (C2-E03/A-19)
[-FID20] (3-2) (C2-B04-2)
12117 C04/A51A-B/B
C0N 4.5-01
C0N 4.5-01
C0N 4.5-01
12107 B07/A07E-A/C
C0N 4.5-04 (C2/B1-C08/A-07)
-START INT
+START INT BUF
-START INT BUF
C0N 4.5-00 (C2/B1-D12/B-23)
C0N 4.5-01 (C2/B1-C06-23)
C0N 4.5-04 (C2/B1-B13-23,19,17)
C0N 4.5-02 (C2/B1-D09/A-07)
+BLØCK CLØCK
C0N 4.5-04 (C2/B1-C08/A-08)
+START INT
C0N 4.5-04 (C2/B1-C07-07)
+INT DØNE
12101 E09/A33-A/C
+BLØCK UMEM [-BL0CMM/BL0CUM] (7-19)
C0N 4.1-00 (C2-F09-07)
(C2-B08-19) -BLØCK MM
C0N 4.5-04 (C2/B1-C12-17,18)
12101 E09/A33-B/C
[-NBKCK] (7-21) (C2-B08-21)
RPU 4.2-02 (B2/F2-B09-+E09-22)
12101 E09/A33-C/C
+BLØCK CLØCKS [-BKCLKS] (7-16) (C2-B08-16)
C0N 4.5-00 (C2/B1-E10/A-05)
C0N 4.0-01 (C2-A08/A-35)
-BKCLKS
C0N 4.5-01 (C2/B1-C06-03)
12101 D11/D11-C/C
-CLØCK A [-XMICKB/CTLCKB] (10-19) (C2-B11-19)
XMA 4.11-01 (D2/E2-C06-04,24,17,19)
C0N 4.4-00 (C2-D13-06)
-XMAU1 CLK A [-CLKBIT(3B)/CLK3B] (10-10) (C2-B11-10)
-STØP 1
C0N 4.5-01 (C2/B1-C10-23)
C0N 4.5-01 (C2/B1-C06-11)
-START INT + (RP LØAD P • STØPPED)
12102 B10/A55
[-ADSELB] (8-20) (C2-B09-20)
C0N 4.0-00 (C2-A09,A10-10)
[-ADSELA] (9-19) (C2-B10-19)
C0N 4.0-00 (C2-A09,A10-06)
[-ADSELC] (11-7) (C2-B12-7)
C0N 4.0-00 (C2-A09,A10-27)
+BLOCK CLK 1
C0N 4.5-01 (C2/B1-C11/B-20)
-CLKPULSE
C0N 4.5-01 (C2/B1-C10-20)
TP66
+FID 10
C0N 4.5-02 (C2/B1-D06-24)
C0N 4.5-00 (C2/B1-D13-11)
[-SYSCLKE]
C0N 4.5-01 (C2/B1-B12-16)
-SYSCLKTD3
C0N 4.5-01 (C2/B1-C11/B-22)
[-NRPBLK] (6-17) (C2-B07-17)
RPU 4.2-02 (B2/F2-E10/C-19)
12107 B07/A07-C/C
-PØP STACK 1 [-CLKC]
C0N 4.5-02 (C2/B1-B09/A-24)
TP35
+PØP STACK
C0N 4.5-04 (C2/B1-D12/C-16)
C0N 4.0-00 (C2-F02-49)
[-GENP] (4-8) (C2-B05-08)
C0N 4.0-00 (C2-F02-50)
[-ENAP] (4-10) (C2-B05-10)
C0N 4.4-00 (C2-D01-06)
-DEC STACK [-P0P] (4-5) (C2-B05-05)
C0N 4.5-01 (C2/B1-C06-06)
+BLKCLK
12102 D05/A52
TP11
[-CARP] (3-1) (C2-B04-1)
C0N 4.0-00 (C2-F01-17.34)
-PØP STACK [-P0PSTK] (3-22) (C2-B04-22)
-(+P SEL = 0) + START INT
C0N 4.0-01 (C2-A03-33)
C0N 4.5-01 (C2/B1-D03-03)
C0N 4.5-01 (C2/B1-B08-03)
C0N 4.5-02 (C2/B1-D07/A-01)
C0N 4.5-00 (C2/B1-E04-20)
-STACK WRITE ENABLE
TP13
TP12
+CLR STACK ADRS
C0N 4.5-01 (C2/B1-B08-02)
-P SEL = 0 • (+START INT)
C0N 4.5-02 (C2/B1-D08-15)
RPU 4.2-00 (B2/F2-B06-08)
[-0NCLI] (4-6) (C2-B05-6)
C0N 4.5-04 (C2/B1-C07-11)
-STACK WRITE
C0N 4.5-01 (C2/B1-D02-15)
-STACK MANIPULATIØN
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
STØP CØNDITIØNS
DB-C2PMC:C2/B1
05-20-66
SIZE IDENT 60461830
REV G
SHEET C0N 4.5-03
PAGE IV-3-29
<50 60 70 80 90 FULL


C12102 C12/A82
C12131 C07/A80
C12131 C08/A79-B/B
C12131 C08/A79-A/B
C12131 E14/A80-B/C
C12165 E13/C06
INT PRIORTY CODER
C12102 C13/A83
C12131 E14/A80-A/C
C12102 B13/A01
C12117 C09/A87-C/C
C12101 D12/A99-C/C
C12101 C11/A81-C/C
C12101 B14/B14-C/C
C12131 B06/A70-C/C
C12131 B06/A70-B/C
C2N 4.0-00 (C2-A13,A14-51)
[-BPTE00] [-BPTE01] (10-25) (C2-B11-25) (9-9) (C2-B10-09)
RPU 4.0-22 (B2/J1-E07-08)
[-STPIE] (9-10) (C2-B10-10)
C2N 4.5-03 (C2/B1-E09/A-08)
-BLOCK WM
C2N 4.5-01 (C2/B1-C06-12)
-(+START INT) • (+RP LOAD P • STOPPED)
C2N 4.5-00 (C2/B1-E12/A-07)
[-RWMM]
C2N 4.4-00 (C2-D15-06)
[-CLB46] (10-24) (C2-B11-24)
TP68
TP43
RPU 4.0-22 (B2/J1-A07-11)
[-BKPEN1] (7-18) (C2-B08-18)
-BA = P
C2N 4.5-01 (C2/B1-B14/A-23)
+BLOCK WM
C2N 4.5-00 (C2/B1-D13-18)
-RWMM SEL P
C2N 4.5-02 (C2/B1-D08/A-18)
+RWMM EN P
C2N 4.5-02 (C2/B1-E10/B-01)
[-CKB46/ROR1] (9-17) (C2-B10-17)
RPU 4.1-22 (B2/J2-E14-20)
H
[-BKPSTP] (9-15) (C2-B10-15)
RPU 4.0-22 (B2/J1-A06-01)
+BKPSTP
C2N 4.5-03 (C2/B1-D11/B-20)
C2N 4.5-03 (C2/B1-D05-06)
+P0P STACK
C2N 4.5-01 (C2/B1-C06-15)
+EN INT D0NE
C2N 4.5-00 (C2/B1-E12/A.D12/B.C11/A)
[+RWMM]
C2N 4.5-01 (C2/B1-B12-13)
+SYCLCK5
C2N 4.5-00 (C2/B1-D13-14)
+SET STACK WRITE
C2N 4.5-02 (C2/B1-D07/C-14)
-WRITE STACK
RPU 4.2-01 (B2/F2-D12-14)
[-SETLK0] (6-15) (C2-B07-15)
[-(+INTR)] (8-19) (C2-B09-19)
C2N 4.5-31 (C2/C2-E01.E1T-22)
+INT D0NE
C2N 4.5-03 (C2/B1-E09/A.B.C-06.24.19)
-INT D0NE [-ITDN] (8-21) (C2-B09-21)
C2N 4.5-21 (C2/C1-E05-22)
C2N 4.5-03 (C2/B1-C09/A-23)
-STACK WRITE
C2N 4.5-03 (C2/B1-D05-20)
TP32
TP30
C2N 4.5-01 (C2/B1-C05-03)
+MC1
C2N 4.5-01 (C2/B1-C06-16)
-EN INT D0NE
RPU 4.2-01 (B2/F2-D12-12)
[-CIL] (11-21) (C2-B12-21)
C2N 4.5-01 (C2/B1-C05-04)
+MC2
C2N 4.5-00 (C2/B1-C11/A-04)
C2N 4.5-02 (C2/B1-C04/A-15)
C2N 4.5-03 (C2/B1-B07/A-18)
TP86
TP54
TP57
TP79
RPU 4.0-22 (B2/J1-A07-14)
[-RPIL] (9-21) (C2-B10-21)
C2N 4.5-03 (C2/B1-C09/A-12)
+SET STOP 2
-SET INT
C2N 4.5-01 (C2/B1-B14/B-06)
+SET INT [-NINT] (7-25) (C2-B08-25)
RPU 4.0-21 (B2/J1-A03-15)
C2N 4.5-01 (C2/B1-B14-06)
-SET INT1
-START INT
C2N 4.5-01 (C2/B1-B12-05)
+SYCLCK4
+START INT
C2N 4.5-03 (C2/B1-E09/A.B.C-05.23.18)
-(+SET INT) + (+INT ACTIVE)
C2N 4.5-01 (C2/B1-E12/C-15)
RPU 4.0-20 (B2/J1-B04-08)
[-D0F2] (11-1) (C2-B12-01)
C2N 4.5-01 (C2/B1-B14/A-01)
RPU 4.0-22 (B2/J1-A01-06)
[-L0ADP] (8-9) (C2-B09-09)
-RING P0RT LD P
C2N 4.5-01 (C2/B1-C10-24)
C2N 4.5-03 (C2/B1-C09/A-11)
-SET ST0P 2
C2N 4.5-03 (C2/B1-D11/A-08)
-SET ST0P 1
-BKP INT [-INTP7]
C2N 4.5-01 (C2/B1-B15-13)
NU [-NINTX1] (10-4) (C2-B11-04)
NU [-NINTX0] (11-16) (C2-B12-16)
-INTC0
C2N 4.5-01 (C2/B1-B14/B-03)
-INTC1
C2N 4.5-01 (C2/B1-B14/B-04)
-INTC2
C2N 4.5-01 (C2/B1-B14/B-05)
RPU 4.1-20 (B2/J2-D15-06)
[-INTP3/INTP(4)] (11-25) (C2-B12-25)
RPU 4.0-20 (B2/J1-D15-06)
[-INTP2/INTP(3)] (11-24) (C2-B12-24)
RPU 4.1-21 (B2/J2-D08-13)
[-INTP1] (10-03) (C2-B11-03)
RPU 4.0-21 (B2/J1-A03-12)
[-INTP0] (10-06) (C2-B11-06)
NU (10-07) (C2-B11-07)
TP87
TP81
TP89
C2N 4.5-03 (C2/B1-B07/E-16)
-START INT BUF
C2N 4.5-01 (C2/B1-B12-15)
+SYCLK8
C2N 4.5-01 (C2/B1-E12/C-14)
+INT1
C2N 4.5-01 (C2/B1-D12/A-06)
+SYCLCK6
C2N 4.5-00 (C2/B1-C11/A-07)
-(+RWMM) • START INT
[-INTPRS/CVB2(0)] (7-8) (C2-B08-08)
C2N 4.3-00 (C2-G08-48)
[-INTC(0-2)]
C2N 4.0-00 (C2-A10-35.41.43)
-12)
-11)
-10)
TP37
TP40
+BLOCK INC
C2N 4.5-02 (C2/B1-B06/A-16)
-INT INC STACK
C2N 4.5-02 (C2/B1-C04/A-19)
NOTE:
BIT | AUX | LSI
0 | 10-1 | C2-B11-01
1 | 11-26 | C2-B12-26
2 | 11-3 | C2-B12-03
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
DB-C2PMC:C2/B1
05-15-66
CODE IDENT
60461830
REV
E
SHEET
C0N 4.5-04
PAGE
IV-3-31



AUX BIT	BIT	UMID AUX LØC	UMID LSI LØC	UMEM AUX LØC	UMEM LSI LØC
0	64	13-10	C2-B2-36	13-9	C2-B2-35
1	65	13-8	C2-B2-34	13-7	C2-B2-33
2	66	13-6	C2-B2-32	13-3	C2-B2-29
3	67	13-4	C2-B2-30	13-1	C2-B2-27
4	80	12-10	C2-B3-36	12-9	C2-B3-35
5	81	12-8	C2-B3-34	12-7	C2-B3-33
6	82	12-6	C2-B3-32	12-3	C2-B3-29
7	83	12-4	C2-B3-30	12-1	C2-B3-27
8	96	12-16	C2-B3-42	12-21	C2-B3-47
9	97	12-24	C2-B3-50	12-19	C2-B3-45
10	98	12-20	C2-B3-46	12-17	C2-B3-43
11	99	12-16	C2-B3-42	12-15	C2-B3-41
12	112	11-10	C2-B4-36	11-7	C2-B4-33
13	113	11-8	C2-B4-34	11-3	C2-B4-29
14	114	11-6	C2-B4-32	11-1	C2-B4-27
15	115	11-4	C2-B4-30	12-25	C2-B3-51
16	68	11-26	C2-B4-52	11-25	C2-B4-51
17	69	11-24	C2-B4-50	11-21	C2-B4-47
18	70	11-20	C2-B4-46	11-19	C2-B4-45
19	71	11-16	C2-B4-42	11-17	C2-B4-43
20	84	9-10	C2-B6-36	9-9	C2-B6-35
21	85	9-8	C2-B6-34	9-7	C2-B6-33
22	86	9-6	C2-B6-32	9-3	C2-B6-29
23	87	9-4	C2-B6-30	9-1	C2-B6-27
24	76	9-26	C2-B6-52	9-25	C2-B6-51
25	77	9-24	C2-B6-50	9-21	C2-B6-47
26	78	9-20	C2-B6-46	9-19	C2-B6-45
27	79	9-16	C2-B6-42	9-17	C2-B6-43
28	92	8-20	C2-B7-46	8-19	C2-B7-45
29	93	8-16	C2-B7-42	8-15	C2-B7-41
30	94	8-10	C2-B7-36	8-9	C2-B7-35
31	95	8-8	C2-B7-34	8-7	C2-B7-33
32	108	6-15	C2-B9-41	6-10	C2-B9-36
33	109	6-9	C2-B9-35	6-8	C2-B9-34
34	110	6-7	C2-B9-33	6-6	C2-B9-32
35	111	6-4	C2-B9-30	6-3	C2-B9-29
36	124	5-6	C2-B10-32	5-3	C2-B10-29
37	125	5-4	C2-B10-30	5-1	C2-B10-27
38	126	6-26	C2-B9-52	6-25	C2-B9-51
39	127	6-24	C2-B9-50	6-21	C2-B9-47
40	100	5-26	C2-B10-52	5-25	C2-B10-51
41	101	5-24	C2-B10-50	5-21	C2-B10-47
42	102	5-20	C2-B10-46	5-19	C2-B10-45
43	103	5-16	C2-B10-42	5-17	C2-B10-43
44	116	4-16	C2-B11-42	4-15	C2-B11-41
45	117	4-10	C2-B11-36	4-9	C2-B11-35
46	118	4-8	C2-B11-34	4-7	C2-B11-33
47	119	4-6	C2-B11-32	4-3	C2-B11-29
48	72	3-26	C2-B12-52	3-25	C2-B12-51
49	73	3-24	C2-B12-50	3-20	C2-B12-46
50	74	3-21	C2-B12-47	3-19	C2-B12-45
51	75	3-17	C2-B12-43	3-16	C2-B12-42
52	88	2-16	C2-B13-42	2-15	C2-B13-41
53	89	2-9	C2-B13-35	2-10	C2-B13-36
54	90	2-7	C2-B13-33	2-8	C2-B13-34
55	91	2-6	C2-B13-32	2-4	C2-B13-30
56	104	1-1	C2-B14-27	2-26	C2-B13-52
57	105	2-25	C2-B13-51	2-24	C2-B13-50
58	106	2-20	C2-B13-46	2-21	C2-B13-47
59	107	2-19	C2-B13-45	2-17	C2-B13-43
60	120	1-15	C2-B14-41	1-10	C2-B14-36
61	121	1-8	C2-B14-34	1-9	C2-B14-35
62	122	1-7	C2-B14-33	1-6	C2-B14-32
63	123	1-4	C2-B14-30	1-3	C2-B14-29

AUX BØARD MEMØRY BIT XX-XX	HØLDS INST RGTR BIT YY	USE
B2-00	64	
↓ 03	↓ 67	
16	68	
↓ 19	↓ 71	DCØ
48	72	
↓ 51	↓ 75	
24	76	
↓ B2-27	↓ 79	
B2-04	80	
↓ 07	↓ 83	
20	84	
↓ 23	↓ 87	DC1
52	88	
↓ 55	↓ 91	
28	92	
↓ B2-31	↓ 95	
B2-08	96	
↓ 11	↓ 99	
40	100	
↓ 43	↓ 103	DC2
56	104	
↓ 59	↓ 107	
32	108	
↓ B2-35	↓ 111	
B2-12	112	
↓ 15	↓ 115	
44	116	
↓ 47	↓ 119	DC3
60	120	
↓ 63	↓ 123	
36	124	
↓ B2-39	↓ 127	

ADDX(1)	TP
1	3
2	15
3	28
4	39
5	40
6	41
7	43
8	49
10	13
11	79
12	80
13	81
14	83
15	93
16	107
17	119

NØTE:
1. USE CHART TØ MATCH INPUT BIT TØ CHIP BIT.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM INSTRUCTIØN MEMØRY (64-127).	DRAWING NUMBER 60461830	REV A
DEVELØPMENT DIVISION	DB-C2PM4:C2/B2	SHEET C2N 4.5-10	PAGE IV-3-33

C2N 4.5-03
(C2/B1-E11-03)

-STØP
[-INPUTA]
(10-1)
(C2-B05-27)

12112 E05/E05 A BITS 0-7

CX	22	1	T1	-(0)
		2	T2	-(1)
A1	24	3	F1	+(0)
		4	F2	+(1)
		8	T3	-(2)
A2	23	7	T4	-(3)
		6	F3	+(2)
		5	F4	+(3)
		11	T5	-(4)
A3	20	12	T6	-(5)
		13	F5	+(4)
		14	F6	+(5)
		18	T7	-(6)
A4	19	17	T8	-(7)
		16	F7	+(6)
		15	F8	+(7)

+STØP → NU
NU
(-NSTØP(0)) → MUL 4.0-06 B HIGHER (A2-A11-09)
(-NSTØP(1)) → MUL 4.0-08 ØUTPUT RGTR LØWER (A2-A06/B-46)
NU
NU
(-NSTØP(2)) → MUL 4.0-08 ØUTPUT RGTR LØWER (A2-E05/B-46)
(-NSTØP(3)) → MUL 4.0-06 A LØWER (A2-A04/A,B03-09,46)
NU
NU
(-NSTØP(4)) → MUL 4.0-08 STATUS (A2-A15/A,E15/A-09)
(-NSTØP(5)) → SBU 4.0-02 STATUS AND ØUTPUT RGTRS (A2-G02-09,46)
NU
NU
(-NSTØP(6)) → SBU 4.1-02 STATUS AND ØUTPUT RGTRS (A2-G09,G13-09,46)
(-NSTØP(7)) → FGU 4.0-01 F FILE DATA ØUTPUT RGTR (A2-K08-09,46)

12112 E13/E13 A BITS 8-15

CX	22	1	T1	-(8)
		2	T2	-(9)
A1	24	3	F1	+(8)
		4	F2	+(9)
		8	T3	-(10)
A2	23	7	T4	-(11)
		6	F3	+(10)
		5	F4	+(11)
		11	T5	-(12)
A3	20	12	T6	-(13)
		13	F5	+(12)
		14	F6	+(13)
		18	T7	-(14)
A4	19	17	T8	-(15)
		16	F7	+(14)
		15	F8	+(15)

NU
NU
[-NSTØP(8)] → FGU 4.0-01 F FILE DATA ØUTPUT RGTR (A2-G15/A-09)
[-NSTØP(9)] → FPM 4.2-00 (B3-G01/B-43,44,10,09)
NU
NU
[-NSTØP(10)/WAND30(8)] → SHA 4.0-00 GRØUP SELECTØR (B2-K02-48)
[-NSTØP(11)] → DMU 4.0-01 (B2-A06/B,A10/B-18,44)
NU
NU
[-NSTØP(12)] → ADD 4.0-00 ØUTPUT RGTR (D2-H02/A,H03/A-46)
[-NSTØP(13)] → ADD 4.1-00 ØUTPUT RGTR (D2-H06/A,H07/A-46)
NU
NU
[-NSTØP(14)] → ADD 4.0-02 (D2-F01/B-09)
[-NSTØP(15)]] → ADD 4.1-02 STATUS RGTR (D2-F05/B-09)

C2N 4.5-02
(C2/B1-E10/C-13)

[-NSTP]
(7-3)
(C2-B08-29)

12112 E09/E09 C BITS 0-7

CX	22	1	T1	-(0)
		2	T2	-(1)
A1	24	3	F1	+(0)
		4	F2	+(1)
		8	T3	-(2)
A2	23	7	T4	-(3)
		6	F3	+(2)
		5	F4	+(3)
		11	T5	-(4)
A3	20	12	T6	-(5)
		13	F5	+(4)
		14	F6	+(5)
		18	T7	-(6)
A4	19	17	T8	-(7)
		16	F7	+(6)
		15	F8	+(7)

[-ØUTC(7)]
NU
NU
NU
NU
NU
NU
[-ENIREG] → FPC 4.0-00 (C3-B07)
NU
NU

[-INPUTB]
(13-16)
(C2-B02-42)

12112 E01/E01 B BITS 0-7

CX	22	1	T1	-(0)
		2	T2	-(1)
A1	24	3	F1	
		4	F2	
		8	T3	-(2)
A2	23	7	T4	-(3)
		6	F3	
		5	F4	
		11	T5	-(4)
A3	20	12	T6	-(5)
		13	F5	
		14	F6	
		18	T7	-(6)
A4	19	17	T8	-(7)
		16	F7	
		15	F8	

→ NU

12112 E17/E17 B BITS 8-15

CX	22	1	T1	-(8)
		2	T2	-(9)
A1	24	3	F1	
		4	F2	
		8	T3	-(10)
A2	23	7	T4	-(11)
		6	F3	
		5	F4	
		11	T5	-(12)
A3	20	12	T6	-(13)
		13	F5	
		14	F6	
		18	T7	-(14)
A4	19	17	T8	-(15)
		16	F7	
		15	F8	

→ NU

+STØP
[-ØUTB(15)] → C2N 4.0-00 (C2-A04,A05-07)

(13)

+STØP
[-ENI/EN2],
[-ØUTB(0-6,9-14),ØUTC(0-5)] → C2N 4.4-00 (C2-D01 → D15-09,46)

(6)

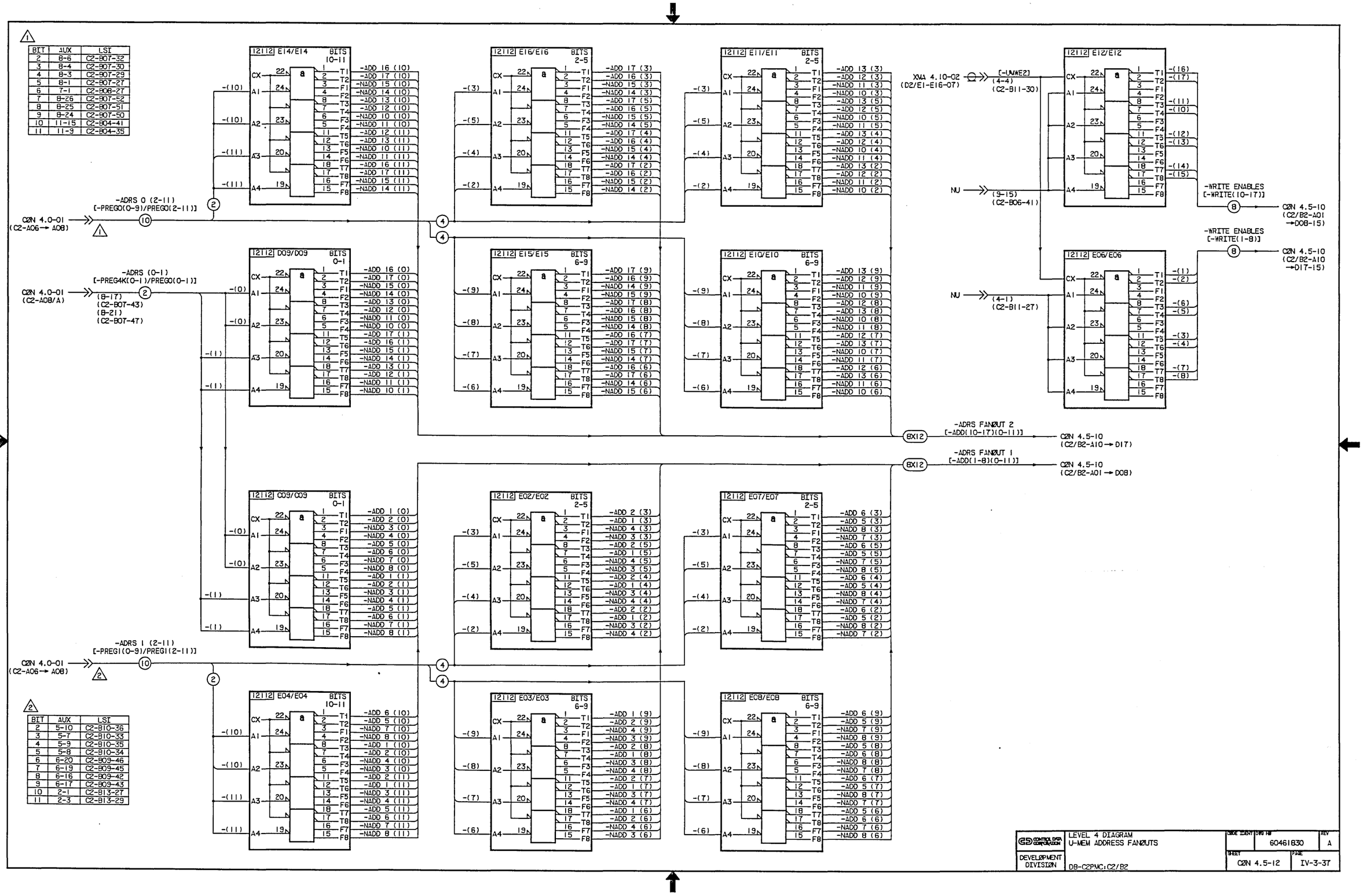
A ØUT BIT	AUX LØC/ LSI LØC	A ØUT BIT	AUX LØC/ LSI LØC	B ØUT BIT	AUX LØC/ LSI LØC	C ØUT BIT	AUX LØC/ LSI LØC
0	4-17	+0	4-20	0	1-17	0	7-8
	C2-B11-43		C2-B11-46		C2-B14-43		C2-B08-34
1	4-19	+1	4-21	1	1-19	1	7-9
	C2-B11-45		C2-B11-47		C2-B14-45		C2-B08-35
2	4-26	+2	4-25	2	1-24	2	7-21
	C2-B11-52		C2-B11-51		C2-B14-50		C2-B08-47
3	3-1	+3	4-24	3	1-26	3	7-24
	C2-B12-27		C2-B11-50		C2-B14-52		C2-B08-50
4	3-4	+4	3-6	4	1-25	4	7-20
	C2-B12-30		C2-B12-32		C2-B14-51		C2-B08-46
5	3-3	+5	3-7	5	1-21	5	7-19
	C2-B12-29		C2-B12-33		C2-B14-47		C2-B08-45
6	3-15	+6	3-9	6	1-16	6	7-6
	C2-B12-41		C2-B12-35		C2-B14-42		C2-B08-32
7	3-10	+7	3-8	7	1-20	7	7-4
	C2-B12-36		C2-B12-34		C2-B14-46		C2-B08-30
8	10-3	+8	10-6	8	13-15	+0	7-10
	C2-B05-29		C2-B05-32		C2-B02-41		C2-B08-36
9	10-4	+9	10-7	9	13-17	+1	7-15
	C2-B05-30		C2-B05-33		C2-B02-43		C2-B08-41
10	10-10	+10	10-8	10	13-24	+2	7-17
	C2-B05-36		C2-B05-34		C2-B02-50		C2-B08-43
11	10-15	+11	10-9	11	13-21	+3	7-16
	C2-B05-41		C2-B05-35		C2-B02-47		C2-B08-42
12	10-16	+12	10-19	12	13-25	+4	8-1
	C2-B05-42		C2-B05-45		C2-B02-51		C2-B09-27
13	10-17	+13	10-21	13	13-26	+5	7-25
	C2-B05-43		C2-B05-47		C2-B02-52		C2-B08-51
14	10-26	+14	10-24	14	13-19	+6	7-7
	C2-B05-52		C2-B05-50		C2-B02-45		C2-B08-33
15	10-25	+15	10-20	15	13-20	+7	7-26
	C2-B05-51		C2-B05-46		C2-B02-46		C2-B08-52

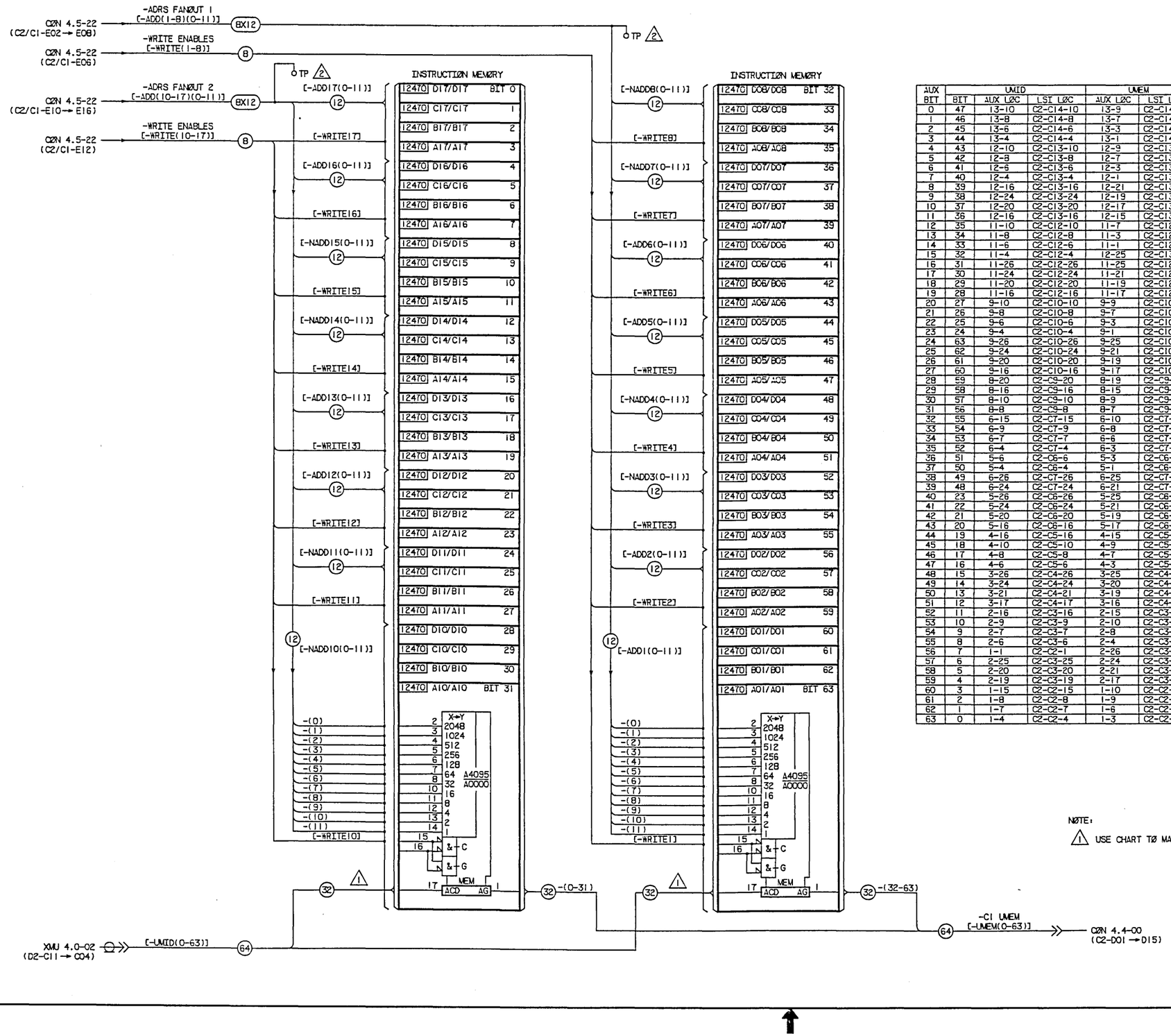
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM

DB-C2PCM4:C2/B2

CAGE IDENT: DWG NO: 60461830 REV: A
SHEET: C2N 4.5-11 SIZE: IV-3-35


1
BIT | AUX | LSI
2 | 8-6 | C2-B07-32
3 | 8-4 | C2-B07-30
4 | 8-3 | C2-B07-29
5 | 8-1 | C2-B07-27
6 | 7-1 | C2-B06-27
7 | 8-26 | C2-B07-52
8 | 8-25 | C2-B07-51
9 | 8-24 | C2-B07-50
10 | 11-15 | C2-B04-41
11 | 11-9 | C2-B04-35
12112 E14/E14 BITS 10-11
12112 E16/E16 BITS 2-5
12112 E11/E11 BITS 2-5
12112 E12/E12
12112 D09/D09 BITS 0-1
12112 E15/E15 BITS 6-9
12112 E10/E10 BITS 6-9
12112 E06/E06
12112 C09/C09 BITS 0-1
12112 E02/E02 BITS 2-5
12112 E07/E07 BITS 2-5
12112 E04/E04 BITS 10-11
12112 E03/E03 BITS 6-9
12112 EC8/EC8 BITS 6-9
-ADRS 0 (2-11) [-PREGO(0-9)/PREGO(2-11)]
C2N 4.0-01 (C2-A06→ A08)
-ADRS (0-1) [-PREG4K(0-1)/PREGO(0-1)]
C2N 4.0-01 (C2-A08/A)
(B-17) (C2-B07-43) (B-21) (C2-B07-47)
-ADRS 1 (2-11) [-PREG1(0-9)/PREG1(2-11)]
C2N 4.0-01 (C2-A06→ A08)
2
BIT | AUX | LSI
2 | 5-10 | C2-B10-36
3 | 5-7 | C2-B10-33
4 | 5-9 | C2-B10-35
5 | 5-8 | C2-B10-34
6 | 6-20 | C2-B09-46
7 | 6-19 | C2-B09-45
8 | 6-16 | C2-B09-42
9 | 6-17 | C2-B09-43
10 | 2-1 | C2-B13-27
11 | 2-3 | C2-B13-29
XMA 4.10-02 (D2/E1-E16-07)
[-UAWE2] (4-4) (C2-B11-30)
NU (9-15) (C2-B06-41)
NU (4-1) (C2-B11-27)
-WRITE ENABLES [-WRITE(10-17)]
-WRITE ENABLES [-WRITE(1-8)]
C2N 4.5-10 (C2/B2-A01 →D08-15)
C2N 4.5-10 (C2/B2-A10 →D17-15)
8X12
-ADRS FANOUT 2 [-ADD(10-17)(0-11)]
C2N 4.5-10 (C2/B2-A10→ D17)
-ADRS FANOUT 1 [-ADD(1-8)(0-11)]
C2N 4.5-10 (C2/B2-A01 → D08)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
U-MEM ADDRESS FANOUTS
D8-C2PMC:C2/B2
CAGE IDENT
DWG NO
60461830
REV
A
SHEET
C2N 4.5-12
PAGE
IV-3-37



AUX BIT	BIT	UMID AUX LØC	UMID LSI LØC	UMEM AUX LØC	UMEM LSI LØC
0	47	13-10	C2-C14-10	13-9	C2-C14-9
1	46	13-8	C2-C14-8	13-7	C2-C14-7
2	45	13-6	C2-C14-6	13-3	C2-C14-3
3	44	13-4	C2-C14-4	13-1	C2-C14-1
4	43	12-10	C2-C13-10	12-9	C2-C13-9
5	42	12-8	C2-C13-8	12-7	C2-C13-7
6	41	12-6	C2-C13-6	12-3	C2-C13-3
7	40	12-4	C2-C13-4	12-1	C2-C13-1
8	39	12-16	C2-C13-16	12-21	C2-C13-21
9	38	12-24	C2-C13-24	12-19	C2-C13-19
10	37	12-20	C2-C13-20	12-17	C2-C13-17
11	36	12-16	C2-C13-16	12-15	C2-C13-15
12	35	11-10	C2-C12-10	11-7	C2-C12-7
13	34	11-8	C2-C12-8	11-3	C2-C12-3
14	33	11-6	C2-C12-6	11-1	C2-C12-1
15	32	11-4	C2-C12-4	12-25	C2-C13-25
16	31	11-26	C2-C12-26	11-25	C2-C12-25
17	30	11-24	C2-C12-24	11-21	C2-C12-21
18	29	11-20	C2-C12-20	11-19	C2-C12-19
19	28	11-16	C2-C12-16	11-17	C2-C12-17
20	27	9-10	C2-C10-10	9-9	C2-C10-9
21	26	9-8	C2-C10-8	9-7	C2-C10-7
22	25	9-6	C2-C10-6	9-3	C2-C10-3
23	24	9-4	C2-C10-4	9-1	C2-C10-1
24	63	9-26	C2-C10-26	9-25	C2-C10-25
25	62	9-24	C2-C10-24	9-21	C2-C10-21
26	61	9-20	C2-C10-20	9-19	C2-C10-19
27	60	9-16	C2-C10-16	9-17	C2-C10-17
28	59	8-20	C2-C9-20	8-19	C2-C9-19
29	58	8-16	C2-C9-16	8-15	C2-C9-15
30	57	8-10	C2-C9-10	8-9	C2-C9-9
31	56	8-8	C2-C9-8	8-7	C2-C9-7
32	55	6-15	C2-C7-15	6-10	C2-C7-10
33	54	6-9	C2-C7-9	6-8	C2-C7-8
34	53	6-7	C2-C7-7	6-6	C2-C7-6
35	52	6-4	C2-C7-4	6-3	C2-C7-3
36	51	5-6	C2-C6-6	5-3	C2-C6-3
37	50	5-4	C2-C6-4	5-1	C2-C6-1
38	49	6-26	C2-C7-26	6-25	C2-C7-25
39	48	6-24	C2-C7-24	6-21	C2-C7-21
40	23	5-26	C2-C6-26	5-25	C2-C6-25
41	22	5-24	C2-C6-24	5-21	C2-C6-21
42	21	5-20	C2-C6-20	5-19	C2-C6-19
43	20	5-16	C2-C6-16	5-17	C2-C6-17
44	19	4-16	C2-C5-16	4-15	C2-C5-15
45	18	4-10	C2-C5-10	4-9	C2-C5-9
46	17	4-8	C2-C5-8	4-7	C2-C5-7
47	16	4-6	C2-C5-6	4-3	C2-C5-3
48	15	3-26	C2-C4-26	3-25	C2-C4-25
49	14	3-24	C2-C4-24	3-20	C2-C4-20
50	13	3-21	C2-C4-21	3-19	C2-C4-19
51	12	3-17	C2-C4-17	3-16	C2-C4-16
52	11	2-16	C2-C3-16	2-15	C2-C3-15
53	10	2-9	C2-C3-9	2-10	C2-C3-10
54	9	2-7	C2-C3-7	2-8	C2-C3-8
55	8	2-6	C2-C3-6	2-4	C2-C3-4
56	7	1-1	C2-C2-1	2-26	C2-C3-26
57	6	2-25	C2-C3-25	2-24	C2-C3-24
58	5	2-20	C2-C3-20	2-21	C2-C3-21
59	4	2-19	C2-C3-19	2-17	C2-C3-17
60	3	1-15	C2-C2-15	1-10	C2-C2-10
61	2	1-8	C2-C2-8	1-9	C2-C2-9
62	1	1-7	C2-C2-7	1-6	C2-C2-6
63	0	1-4	C2-C2-4	1-3	C2-C2-3

AUX BØARD MEMØRY BIT XX-XX	HØLDS INST RGTR BIT YY	USE
C1-63	00	
↓	↓	
40	23	CLØCK BITS
23	24	
↓	↓	
00	47	
39	48	K FIELD
↓	↓	
C1-24	63	

2

ADDX(1)	TP
1	3
2	15
3	28
4	39
5	40
6	41
7	43
8	49
10	73
11	79
12	80
13	81
14	83
15	93
16	107
17	119

NØTE:

1 USE CHART TØ MATCH INPUT BIT TØ CHIP BIT.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM INSTRUCTION MEMORY (0-63).	CAGE IDENT 60461830	REV A
DEVELØPMENT DIVISIØN	DB-C2PM4:C2/C1	SHEET C2N 4.5-20	PAGE IV-3-39

C2N 4.5-04
(C2/B1-C07-08)

-INT DØNE
[-ITDN]
(10-11)
(C2-C11-1)

12112 E05/E05 A BITS 0-7

12112 E09/E09 C BITS 0-7

(7-3)
(C2-C08-03)

-INTERRUPT DØNE
[-ITDØNE(0)] — MUL 4.0-07 CØNTRØL (A2-A06/A-08)
[-ITDØNE(1)] — MUL 4.0-08 STATUS RGTR (A2-A15-08)
NU
NU
[-ITDØNE(2)] — MUL 4.0-08 CØMPARE LØWER (A2-D02/A.E04/A-08)
[-ITDØNE(3)] — MUL 4.0-08 CØMPARE UPPER (A2-E08/A→E11/A-08)
NU
NU
[-ITDØNE(4)] — SBU 4.0-00 SHIFT ØPERAND/DØUBLE SHIFT RGTR (A2-K03/A→K06-08)
[-ITDØNE(5)] — FGU 4.0-00 FILE CØNTRØL (A2-H08-08)
NU
NU
[-ITDØNE(6)] — SBU 4.1-00 DØUBLE SHIFT RGTR/SHIFT ØPERAND (A2-K10/A→K13/A-08)
[-ITDØNE(7)]
[-ITDØNE(7)] — FGU 4.0-00 FILE CØNTRØL (A2-H08-08)
NU
NU
[-ITDØNE(8)] — FGU 4.0-00 FILE CØNTRØL (A2-H14-08)
[-ITDØNE(9)] — FPC 4.0-00 (C3-D08-08)
NU
NU
[-ITDØNE(10)] — RPU 4.0-01 (B2-G07,H09-08)
[-ITDØNE(11)] — RPU 4.1-01 (B2-G09,H06-08)
NU
NU
[-ITDØNE(12)] — DMU 4.10-00 (B2/B2-E10-24)
[-ITDØNE(13)] — DMU 4.0-00 INPUT ADDRESS RGTR [A] (B2-C08-08)
NU
NU
[-ITDØNE(14)] — DMU 4.0-01 DATA CØMPARE RGTR [CD] (B2-C01→C04-08)
NU
NU

12112 E13/E13 A BITS 8-15

-INT DØNE
(13-16)
(C2-C14-16)

12112 E01/E01 B BITS 0-7

[-ITDØNE(15)] — DMU 4.11-00 (B2/E2-E10-24)
[-ITDØNE(16)] — DMU 4.1-00 INPUT ADDRESS REGISTER (B2-D09-08)
[-ITDØNE(17)] — DMU 4.1-01 DATA CØMPARE REGISTER (B2-D01→D03,C06-08)
[-ITDØNE(18)] — DMU 4.12-00 (B2/B1-E10-24)
[-ITDØNE(19)] — DMU 4.2-00 INPUT ADDRESS REGISTER (B2-A08-08)
[-ITDØNE(20)] — DMU 4.2-01 DATA CØMPARE REGISTER (B2-A12→A15-08)

12112 E17/E17 B BITS 8-15

[-ITDØNE(21)] — DMU 4.13-00 (B2/E1-E10-24)
[-ITDØNE(22)] — DMU 4.3-00 ADDRESS REGISTER (B2-D08-08)
[-ITDØNE(23)] — DMU 4.3-01 DATA CØMPARE REGISTER (B2-D10-08)
NU
NU

-INT DØNE
[-XFR/ØUTB(0,1,13-15)] — (5) — C2N 4.4-00 (C2-D01→D15-08)

[-ITDØNE(27)] — XMA 4.10-01 (D2/E1-B08/C-23)
[-ITDØNE(28)] — XMA 4.11-01 (D2/E2-C07/C-20)
[-ITDØNE(29)] — XMA 4.1-00 (D2-F11-08)
[-ITDØNE(30)] — ADD 4.0-00 A & B ØPERANDS (D2-F01/A,F04/A,G01/A,G04/A-08)
[-ITDØNE(31)] — ADD 4.1-00 A & B ØPERANDS (D2-F05/A,F08/A,G05/A,G08/A-08)
NU
NU
[-ITDØNE(32)] — ADD 4.0-00 ØUTPUT RGTR (D2-H02/A,H03/A-08)
[-ITDØNE(33)] — ADD 4.1-00 ØUTPUT RGTR (D2-H06/A,H07/A-08)

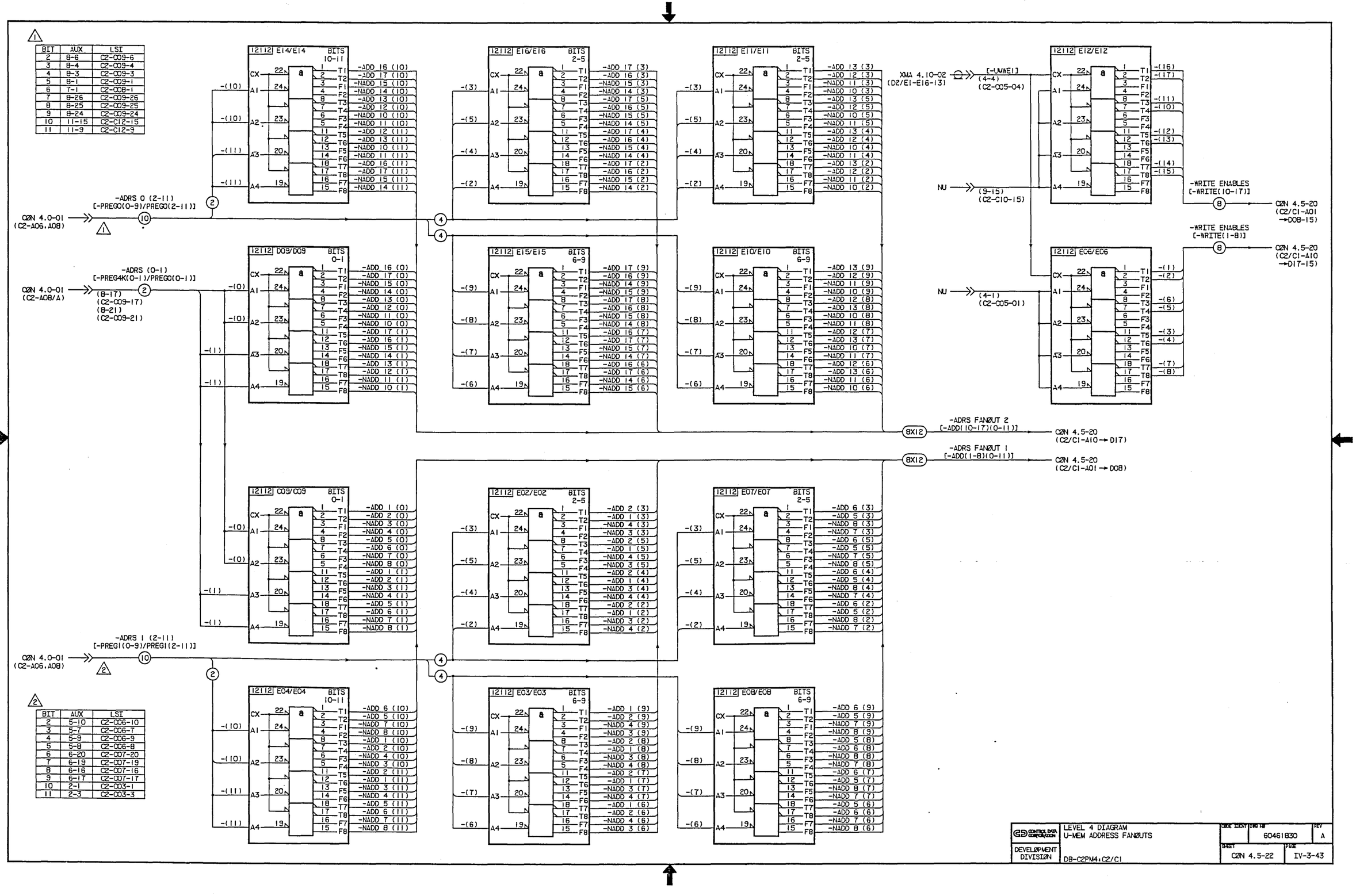
A ØUT BIT	AUX LØC/ LSI LØC	A ØUT BIT	AUX LØC/ LSI LØC	B ØUT BIT	AUX LØC/ LSI LØC	C ØUT BIT	AUX LØC/ LSI LØC
0	4-17 C2-C05-17	+0	4-20 C2-C05-20	0	1-17 C2-C02-17	0	7-8 C2-C08-08
1	4-19 C2-C05-19	+1	4-21 C2-C05-21	1	1-19 C2-C02-19	1	7-9 C2-C08-09
2	4-26 C2-C05-26	+2	4-25 C2-C05-25	2	1-24 C2-C02-24	2	7-21 C2-C08-21
3	3-1 C2-C04-01	+3	4-24 C2-C05-24	3	1-26 C2-C02-26	3	7-24 C2-C08-24
4	3-4 C2-C04-04	+4	3-6 C2-C04-06	4	1-25 C2-C02-25	4	7-20 C2-C08-20
5	3-3 C2-C04-03	+5	3-7 C2-C04-07	5	1-21 C2-C02-21	5	7-19 C2-C08-19
6	3-15 C2-C04-15	+6	3-9 C2-C04-09	6	1-16 C2-C02-16	6	7-6 C2-C08-06
7	3-10 C2-C04-10	+7	3-8 C2-C04-08	7	1-20 C2-C02-20	7	7-4 C2-C08-04
8	10-3 C2-C11-03	+8	10-6 C2-C11-06	8	13-15 C2-C14-15	+0	7-10 C2-C08-10
9	10-4 C2-C11-04	+9	10-7 C2-C11-07	9	13-17 C2-C14-17	+1	7-15 C2-C08-15
10	10-10 C2-C11-10	+10	10-8 C2-C11-08	10	13-24 C2-C14-24	+2	7-17 C2-C08-17
11	10-15 C2-C11-15	+11	10-9 C2-C11-09	11	13-21 C2-C14-21	+3	7-16 C2-C08-16
12	10-16 C2-C11-16	+12	10-19 C2-C11-19	12	13-25 C2-C14-25	+4	8-1 C2-C09-01
13	10-17 C2-C11-17	+13	10-21 C2-C11-21	13	13-26 C2-C14-26	+5	7-25 C2-C08-25
14	10-26 C2-C11-26	+14	10-24 C2-C11-24	14	13-19 C2-C14-19	+6	7-7 C2-C08-07
15	10-25 C2-C11-25	+15	10-20 C2-C11-20	15	13-20 C2-C14-20	+7	7-26 C2-C08-26

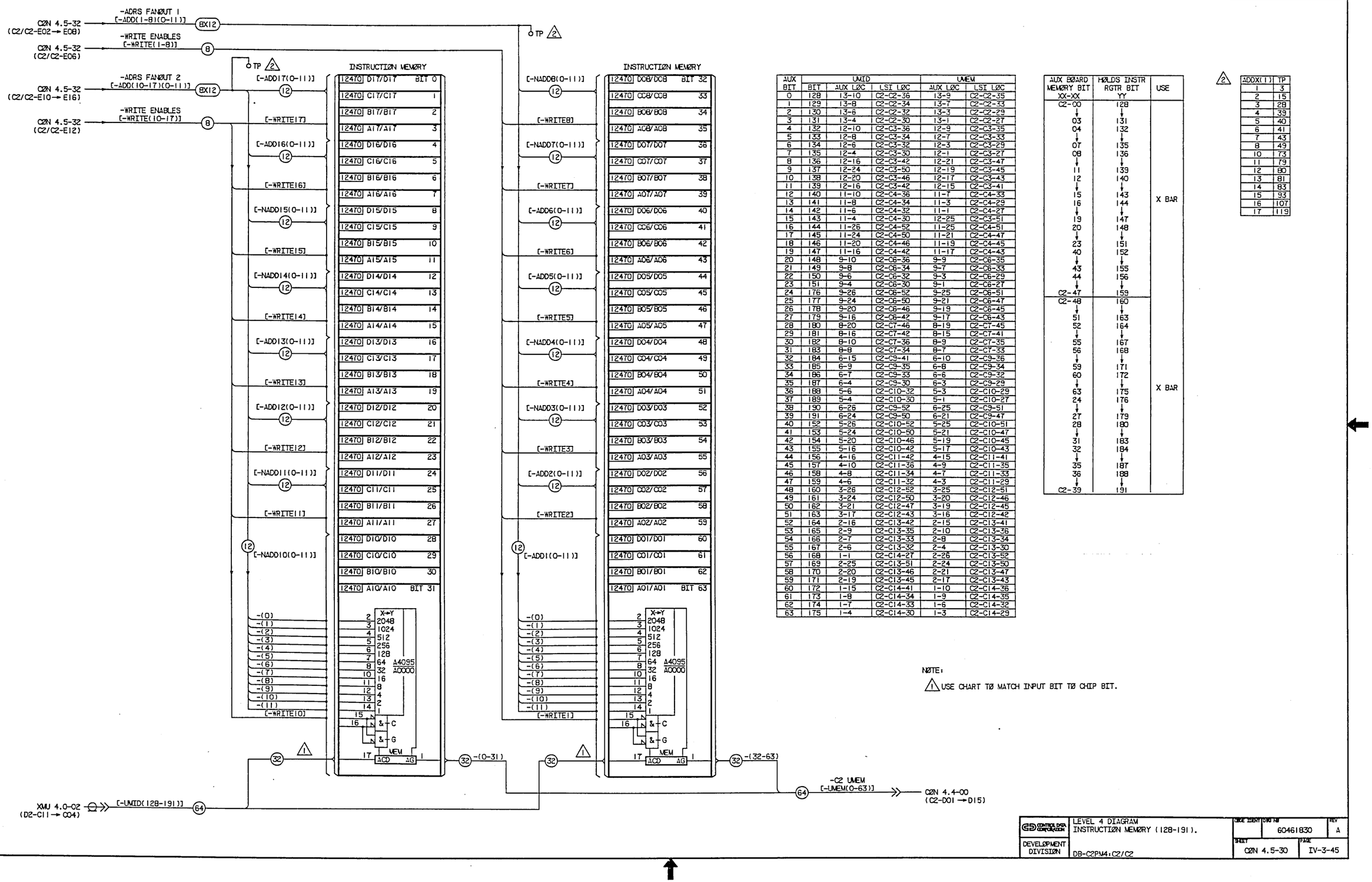
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM

DB-C2PM4,C2/C1

CAGE IDENT | DRG NO: 60461830 | REV: A
SHEET: C2N 4.5-21 | PAGE: IV-3-41


1
BIT | AUX | LSI
2 | 8-6 | C2-C09-6
3 | 8-4 | C2-C09-4
4 | 8-3 | C2-C09-3
5 | 8-1 | C2-C09-1
6 | 7-1 | C2-C08-1
7 | 8-26 | C2-C09-26
8 | 8-25 | C2-C09-25
9 | 8-24 | C2-C09-24
10 | 11-15 | C2-C12-15
11 | 11-9 | C2-C12-9
12112 E14/E14 BITS 10-11
12112 E16/E16 BITS 2-5
12112 E11/E11 BITS 2-5
12112 E12/E12
12112 D09/D09 BITS 0-1
12112 E15/E15 BITS 6-9
12112 E10/E10 BITS 6-9
12112 E06/E06
12112 C09/C09 BITS 0-1
12112 E02/E02 BITS 2-5
12112 E07/E07 BITS 2-5
12112 E04/E04 BITS 10-11
12112 E03/E03 BITS 6-9
12112 E08/E08 BITS 6-9
-ADRS 0 (2-11)
[-PREG0(0-9)/PREG0(2-11)]
C2N 4.0-01
(C2-A06,A08)
-ADRS (0-1)
[-PREG4K(0-1)/PREG0(0-1)]
(8-17)
(C2-C09-17)
(8-21)
(C2-C09-21)
-ADRS 1 (2-11)
[-PREG1(0-9)/PREG1(2-11)]
2
BIT | AUX | LSI
2 | 5-10 | C2-C06-10
3 | 5-7 | C2-C06-7
4 | 5-9 | C2-C06-9
5 | 5-8 | C2-C06-8
6 | 6-20 | C2-C07-20
7 | 6-19 | C2-C07-19
8 | 6-16 | C2-C07-16
9 | 6-17 | C2-C07-17
10 | 2-1 | C2-C03-1
11 | 2-3 | C2-C03-3
XMA 4.10-02
(D2/E1-E16-13)
[-UMWE1]
(4-4)
(C2-C05-04)
NU
(9-15)
(C2-C10-15)
NU
(4-1)
(C2-C05-01)
-WRITE ENABLES
[-WRITE(10-17)]
-WRITE ENABLES
[-WRITE(1-8)]
C2N 4.5-20
(C2/C1-A01
→D08-15)
C2N 4.5-20
(C2/C1-A10
→D17-15)
8X12
-ADRS FANOUT 2
[-ADD(10-17)(0-11)]
C2N 4.5-20
(C2/C1-A10→D17)
8X12
-ADRS FANOUT 1
[-ADD(1-8)(0-11)]
C2N 4.5-20
(C2/C1-A01→D08)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
U-MEM ADDRESS FANOUTS
DB-C2PM4:C2/C1
CODE IDENT
DWG NO
60461830
REV
A
SHEET
C2N 4.5-22
SIZE
IV-3-43



AUX BIT	UMID BIT	UMID AUX LØC	UMID LSI LØC	UMEM AUX LØC	UMEM LSI LØC
0	128	13-10	C2-C2-36	13-9	C2-C2-35
1	129	13-8	C2-C2-34	13-7	C2-C2-33
2	130	13-6	C2-C2-32	13-3	C2-C2-29
3	131	13-4	C2-C2-30	13-1	C2-C2-27
4	132	12-10	C2-C3-36	12-9	C2-C3-35
5	133	12-8	C2-C3-34	12-7	C2-C3-33
6	134	12-6	C2-C3-32	12-3	C2-C3-29
7	135	12-4	C2-C3-30	12-1	C2-C3-27
8	136	12-16	C2-C3-42	12-21	C2-C3-47
9	137	12-24	C2-C3-50	12-19	C2-C3-45
10	138	12-20	C2-C3-46	12-17	C2-C3-43
11	139	12-16	C2-C3-42	12-15	C2-C3-41
12	140	11-10	C2-C4-36	11-7	C2-C4-33
13	141	11-8	C2-C4-34	11-3	C2-C4-29
14	142	11-6	C2-C4-32	11-1	C2-C4-27
15	143	11-4	C2-C4-30	12-25	C2-C3-51
16	144	11-26	C2-C4-52	11-25	C2-C4-51
17	145	11-24	C2-C4-50	11-21	C2-C4-47
18	146	11-20	C2-C4-46	11-19	C2-C4-45
19	147	11-16	C2-C4-42	11-17	C2-C4-43
20	148	9-10	C2-C6-36	9-9	C2-C6-35
21	149	9-8	C2-C6-34	9-7	C2-C6-33
22	150	9-6	C2-C6-32	9-3	C2-C6-29
23	151	9-4	C2-C6-30	9-1	C2-C6-27
24	176	9-26	C2-C6-52	9-25	C2-C6-51
25	177	9-24	C2-C6-50	9-21	C2-C6-47
26	178	9-20	C2-C6-46	9-19	C2-C6-45
27	179	9-16	C2-C6-42	9-17	C2-C6-43
28	180	8-20	C2-C7-46	8-19	C2-C7-45
29	181	8-16	C2-C7-42	8-15	C2-C7-41
30	182	8-10	C2-C7-36	8-9	C2-C7-35
31	183	8-8	C2-C7-34	8-7	C2-C7-33
32	184	6-15	C2-C9-41	6-10	C2-C9-36
33	185	6-9	C2-C9-35	6-8	C2-C9-34
34	186	6-7	C2-C9-33	6-6	C2-C9-32
35	187	6-4	C2-C9-30	6-3	C2-C9-29
36	188	5-6	C2-C10-32	5-3	C2-C10-29
37	189	5-4	C2-C10-30	5-1	C2-C10-27
38	190	6-26	C2-C9-52	6-25	C2-C9-51
39	191	6-24	C2-C9-50	6-21	C2-C9-47
40	152	5-26	C2-C10-52	5-25	C2-C10-51
41	153	5-24	C2-C10-50	5-21	C2-C10-47
42	154	5-20	C2-C10-46	5-19	C2-C10-45
43	155	5-16	C2-C10-42	5-17	C2-C10-43
44	156	4-16	C2-C11-42	4-15	C2-C11-41
45	157	4-10	C2-C11-36	4-9	C2-C11-35
46	158	4-8	C2-C11-34	4-7	C2-C11-33
47	159	4-6	C2-C11-32	4-3	C2-C11-29
48	160	3-26	C2-C12-52	3-25	C2-C12-51
49	161	3-24	C2-C12-50	3-20	C2-C12-46
50	162	3-21	C2-C12-47	3-19	C2-C12-45
51	163	3-17	C2-C12-43	3-16	C2-C12-42
52	164	2-16	C2-C13-42	2-15	C2-C13-41
53	165	2-9	C2-C13-35	2-10	C2-C13-36
54	166	2-7	C2-C13-33	2-8	C2-C13-34
55	167	2-6	C2-C13-32	2-4	C2-C13-30
56	168	1-1	C2-C14-27	2-26	C2-C13-52
57	169	2-25	C2-C13-51	2-24	C2-C13-50
58	170	2-20	C2-C13-46	2-21	C2-C13-47
59	171	2-19	C2-C13-45	2-17	C2-C13-43
60	172	1-15	C2-C14-41	1-10	C2-C14-36
61	173	1-8	C2-C14-34	1-9	C2-C14-35
62	174	1-7	C2-C14-33	1-6	C2-C14-32
63	175	1-4	C2-C14-30	1-3	C2-C14-29

AUX BØARD MEMØRY BIT XX-XX	HØLDS INSTR RGTR BIT YY	USE
C2-00	128	
↓	↓	
03	131	
04	132	
↓	↓	
07	135	
08	136	
↓	↓	
11	139	
12	140	
↓	↓	
15	143	X BAR
16	144	
↓	↓	
19	147	
20	148	
↓	↓	
23	151	
40	152	
↓	↓	
43	155	
44	156	
↓	↓	
C2-47	159	
C2-48	160	
↓	↓	
51	163	
52	164	
↓	↓	
55	167	
56	168	
↓	↓	
59	171	
60	172	
↓	↓	
63	175	X BAR
24	176	
↓	↓	
27	179	
28	180	
↓	↓	
31	183	
32	184	
↓	↓	
35	187	
36	188	
↓	↓	
C2-39	191	

2

ADDX(I)	TP
1	3
2	15
3	28
4	39
5	40
6	41
7	43
8	49
10	73
11	79
12	80
13	81
14	83
15	93
16	107
17	119

NØTE:

1 USE CHART TØ MATCH INPUT BIT TØ CHIP BIT.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM INSTRUCTIØN MEMØRY (128-191).	CDC IDENT/DWG NO 60461830	REV A
DEVELØPMENT DIVISIØN	DB-C2PM4:C2/C2	SHEET CØN 4.5-30	PAGE IV-3-45

Δ ØUT BIT	AUX LØC/ LSI LØC	Δ ØUT BIT	AUX LØC/ LSI LØC	B ØUT BIT	AUX LØC/ LSI LØC	C ØUT BIT	AUX LØC/ LSI LØC
0	4-17 C2-C11-43	+0	4-20 C2-C11-46	0	1-17 C2-C14-43	0	T-8 C2-C08-34
1	4-19 C2-C11-45	+1	4-21 C2-C11-47	1	1-19 C2-C14-45	1	T-9 C2-C08-35
2	4-26 C2-C11-52	+2	4-25 C2-C11-51	2	1-24 C2-C14-50	2	T-21 C2-C08-47
3	3-1 C2-C12-27	+3	4-24 C2-C11-50	3	1-26 C2-C14-52	3	T-24 C2-C08-50
4	3-4 C2-C12-30	+4	3-6 C2-C12-32	4	1-25 C2-C14-51	4	T-20 C2-C08-46
5	3-3 C2-C12-29	+5	3-7 C2-C12-33	5	1-21 C2-C14-47	5	T-19 C2-C08-45
6	3-15 C2-C12-41	+6	3-9 C2-C12-35	6	1-16 C2-C14-42	6	T-6 C2-C08-32
7	3-10 C2-C12-36	+7	3-8 C2-C12-34	7	1-20 C2-C14-46	7	T-4 C2-C08-30
8	10-3 C2-C05-29	+8	10-6 C2-C05-32	8	13-15 C2-C02-41	+0	T-10 C2-C08-36
9	10-4 C2-C05-30	+9	10-7 C2-C05-33	9	13-17 C2-C02-43	+1	T-15 C2-C08-41
10	10-10 C2-C05-36	+10	10-8 C2-C05-34	10	13-24 C2-C02-50	+2	T-17 C2-C08-43
11	10-15 C2-C05-41	+11	10-9 C2-C05-35	11	13-21 C2-C02-47	+3	T-16 C2-C08-42
12	10-16 C2-C05-42	+12	10-19 C2-C05-45	12	13-25 C2-C02-51	+4	B-1 C2-C09-27
13	10-17 C2-C05-43	+13	10-21 C2-C05-47	13	13-26 C2-C02-52	+5	T-25 C2-C08-51
14	10-26 C2-C05-52	+14	10-24 C2-C05-50	14	13-19 C2-C02-45	+6	T-7 C2-C08-33
15	10-25 C2-C05-51	+15	10-20 C2-C05-46	15	13-20 C2-C02-46	+7	T-26 C2-C08-52

C2N 4.5-01 (C2/B1-E12/C-13) → [-INTR1] (10-1) (C2-C05-27)

12|12 E05/E05 A BITS 0-7

CX 22, A1 24, A2 23, A3 20, A4 19

1	T1	-(0)
2	T2	-(1)
3	F1	+(0)
4	F2	+(1)
8	T3	-(2)
7	T4	-(3)
6	F3	+(2)
5	F4	+(3)
11	T5	-(4)
12	T6	-(5)
13	F5	+(4)
14	F6	+(5)
18	T7	-(6)
17	T8	-(7)
16	F7	+(6)
15	F8	+(7)

- NU
- NU
- [-NINTR(0)] → C2N 4.3-00 (A2-A02-15)
- [-NINTR(1)] → RPU 4.0-01 (B2-G07,H09-10)
- NU
- NU
- [-NINTR(2)] → RPU 4.1-01 (B2-G09,H06-10)
- [-NINTR(3)] → FPA 4.0-12 (D3-F07-17)
- [-INTR(4)] → FPU 4.0-00 (C3-B08/A-20)
- [-INTR(5)] → NU
- [-NINTR(4)] → DMU 4.10-03 (B2/B2-E07-19)
- [-NINTR(5)] → DMU 4.0-01 INPUT DATA RGTR (B2-C11/B,C12/B-10)
- [-INTR(6)/ WAND30(9)] → SHA 4.0-00 GRØUP SELECTØR (B2-K02-47)
- NU
- [-NINTR(6)] → DMU 4.0-00 INPUT ADDRESS RGTR (B2-C08-10)
- [-NINTR(7)] → DMU 4.0-01 ØUTPUT RGTR (B2-C02,C03,C01-10)

12|12 E13/E13 A BITS 8-15

CX 22, A1 24, A2 23, A3 20, A4 19

1	T1	-(8)
2	T2	-(9)
3	F1	+(8)
4	F2	+(9)
8	T3	-(10)
7	T4	-(11)
6	F3	+(10)
5	F4	+(11)
11	T5	-(12)
12	T6	-(13)
13	F5	+(12)
14	F6	+(13)
18	T7	-(14)
17	T8	-(15)
16	F7	+(14)
15	F8	+(15)

- [-INTR(8)] → DMU 4.10-03 (B2/B2-E07-18)
- [-NINTR(9)] → DMU 4.11-03 (B2/E2-E07-18)
- [-NINTR(8)] → DMU 4.11-03 (B2/E2-E07-19)
- [-NINTR(9)] → DMU 4.1-01 INPUT DATA RGTR (B2-D11/B,D12/B-10)
- [-INTR(10)] → DMU 4.12-03 (B2/B1-E07-18)
- [-INTR(11)] → DMU 4.13-03 (B2/E1-E07-18)
- [-NINTR(10)] → DMU 4.1-00 INPUT ADDRESS RGTR (B2-D09-10)
- [-NINTR(11)] → DMU 4.1-01 ØUTPUT RGTR (B2-D02,D03,D01-10)
- [-INTR] → FPD 4.2-00 (A3-F07/B-07)
- [-INTR(13)] → XMA 4.10-01 (D2/E1-B08/A-24)
- [-NINTR(12)] → DMU 4.12-03 (B2/B1-E07-19)
- [-NINTR(13)] → DMU 4.2-01 INPUT DATA RGTR (B2-A04/B,A05/B-10)
- [-INTR(14)] → XMA 4.11-01 (D2/E2-C07/A-23)
- [-INTR(15)] → (7-3) (C2-C08-29)
- [-NINTR(14)/ NINTR(27)] → ADD 4.1-01 C2MPARE RGTR (D2-H08/B-10)
- [-NINTR(15)/ NINTR(24)] → ADD 4.0-00 A/B ØPERAND (D2-F01/A,G01/A-10)

C2N 4.5-04 (C2/B1-C08/B-11) → [-(+INTR)] (13-16) (C2-C02-42)

12|12 E01/E01 B BITS 0-7

CX 22, A1 24, A2 23, A3 20, A4 19

1	T1	-(0)
2	T2	-(1)
3	F1	
4	F2	
8	T3	-(2)
7	T4	-(3)
6	F3	
5	F4	
11	T5	-(4)
12	T6	-(5)
13	F5	
14	F6	
18	T7	-(6)
17	T8	-(7)
16	F7	
15	F8	

12|12 E17/E17 B BITS 8-15

CX 22, A1 24, A2 23, A3 20, A4 19

1	T1	-(8)
2	T2	-(9)
3	F1	
4	F2	
8	T3	-(10)
7	T4	-(11)
6	F3	
5	F4	
11	T5	-(12)
12	T6	-(13)
13	F5	
14	F6	
18	T7	-(14)
17	T8	-(15)
16	F7	
15	F8	

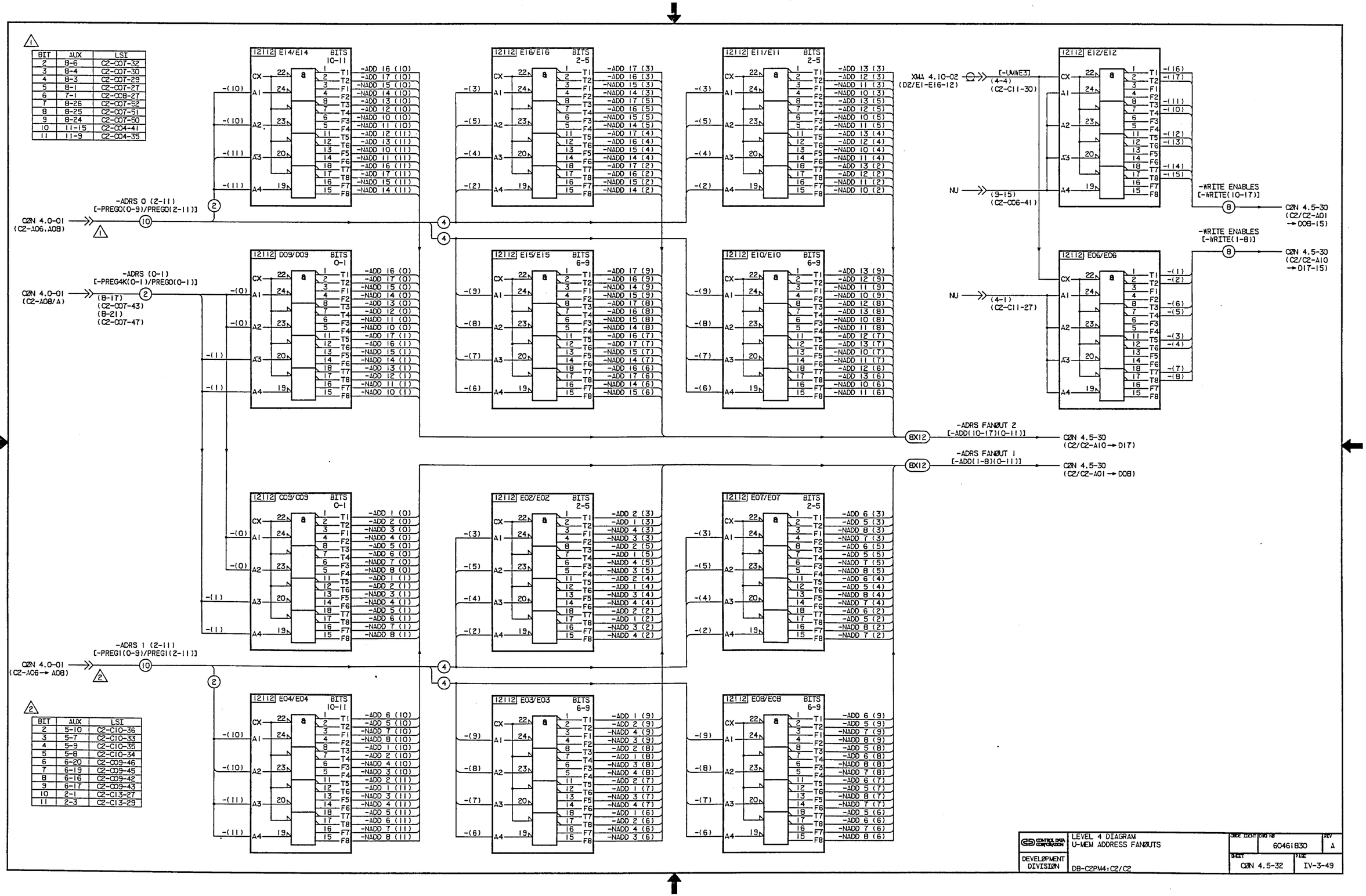
12|12 E09/E09 C BITS 0-7

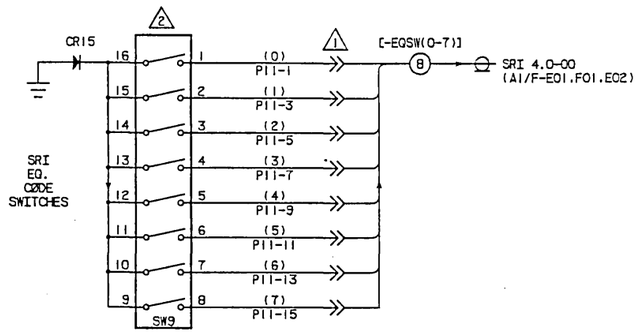
CX 22, A1 24, A2 23, A3 20, A4 19

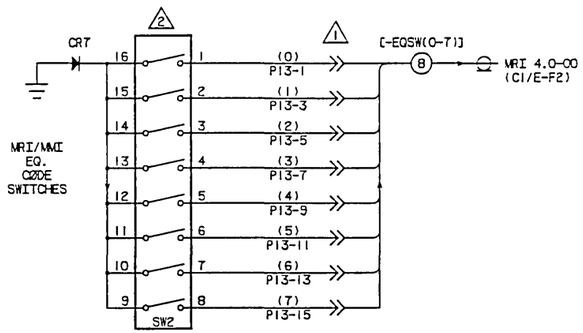
1	T1	-(0)
2	T2	-(1)
3	F1	+(0)
4	F2	+(1)
8	T3	-(2)
7	T4	-(3)
6	F3	+(2)
5	F4	+(3)
11	T5	-(4)
12	T6	-(5)
13	F5	+(4)
14	F6	+(5)
18	T7	-(6)
17	T8	-(7)
16	F7	+(6)
15	F8	+(7)

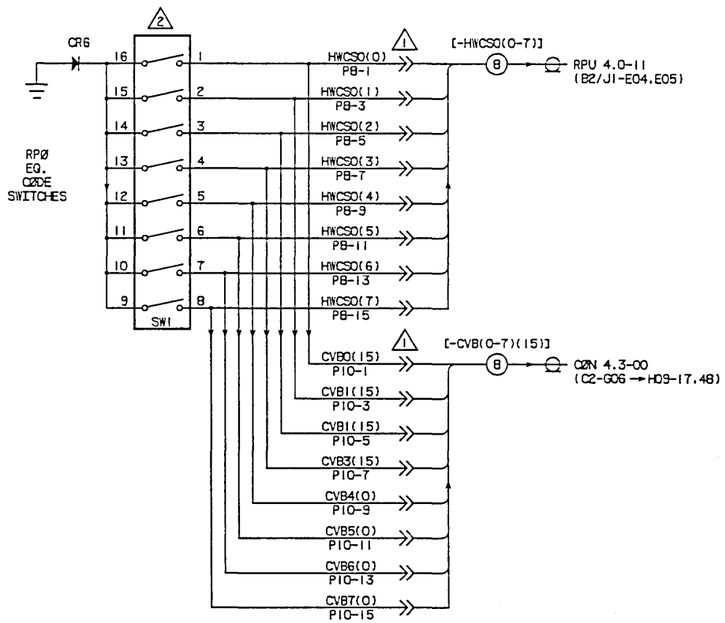
- NU
- [-NINTR(21)] → ADD 4.0-00 A/B ØPERAND (D2-F04/A,G04/A-10)
- [-NINTR(22)] → XMA 4.1-00 (D2-F11-10)
- [-NINTR(16)] → DMU 4.13-03 (B2/E1-E07-19)
- [-NINTR(17)] → DMU 4.3-01 INPUT DATA RGTR (B2-D06/B,D05/B-10)
- [-NINTR(18)] → DMU 4.3-00 INPUT ADDRESS RGTR (B2-D08-10)
- [-NINTR(19)] +INT [-NINTR]. → DMU 4.3-01 ØUTPUT DATA RGTR (B2-D13,D14,C14,D10/B)
- 9 → 10 [-ØUTB(3-7,12-15),NØTC(7)] → C2N 4.4-00 (C2-D01 → D15-10)
- +(7)
- NU
- NU
- [-NINTR(23)] → ADD 4.1-00 A/B ØPERAND (D2-F08/A,G08/A,H07/A-10)
- [-NINTR(24)/NINTR(15)] → DMU 4.2-01 ØUTPUT DATA RGTR (B2-A13,A14,A15-10)
- NU
- NU
- [-NINTR(25)] → ADD 4.1-00 A/B ØPERAND (D2-F05/A,G05/A-10)
- [-NINTR(26)] → ADD 4.0-00 ØUTPUT RGTR (D2-H02/A,H03/A-10)
- NU
- NU
- [-NINTR(27)/NINTR(14)] → DMU 4.2-00 INPUT ADDRESS RGTR (B2-A08-10)
- [-NINTR(28)] → C2N 4.3-00 (A2-H10-15)
- NU
- NU
- [-NINTR(29)] → FGU 4.0-01 F FILE DATA ØUTPUT RGTR (A2-G15,H15-10)

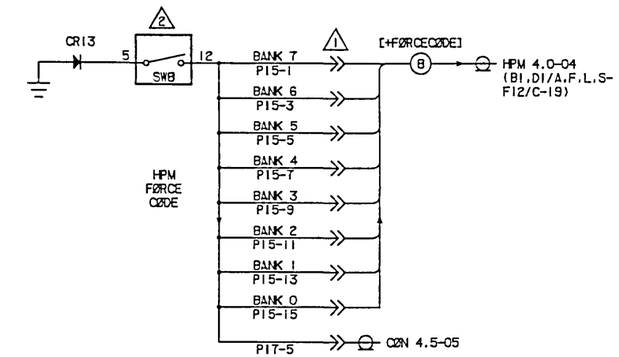
CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-C2PM4:C2/C2	SHEET C2N 4.5-31	PAGE IV-3-47

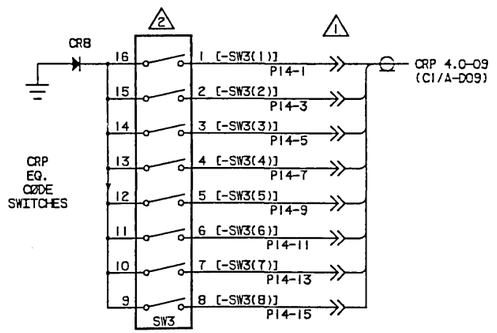

1
BIT AUX LSI
2 8-6 C2-C07-32
3 8-4 C2-C07-30
4 8-3 C2-C07-29
5 8-1 C2-C07-27
6 7-1 C2-C08-27
7 8-26 C2-C07-52
8 8-25 C2-C07-51
9 8-24 C2-C07-50
10 11-15 C2-C04-41
11 11-9 C2-C04-35
12112 E14/E14 BITS 10-11
12112 E16/E16 BITS 2-5
12112 E11/E11 BITS 2-5
12112 E12/E12
12112 D09/D09 BITS 0-1
12112 E15/E15 BITS 6-9
12112 E10/E10 BITS 6-9
12112 E06/E06
-ADRS 0 (2-11)
[-PREG0(0-9)/PREG0(2-11)]
C2N 4.0-01
(C2-A06,A08)
-ADRS (0-1)
[-PREG4K(0-1)/PREG0(0-1)]
C2N 4.0-01
(C2-A08/A)
(8-17)
(C2-C07-43)
(8-21)
(C2-C07-47)
XMA 4.10-02
(D2/E1-E16-12)
[-LWWE3]
(4-4)
(C2-C11-30)
NU
(9-15)
(C2-C06-41)
NU
(4-1)
(C2-C11-27)
-WRITE ENABLES
[-WRITE(10-17)]
C2N 4.5-30
(C2/C2-A01
→D08-15)
-WRITE ENABLES
[-WRITE(1-8)]
C2N 4.5-30
(C2/C2-A10
→D17-15)
BX12
-ADRS FANOUT 2
[-ADD(10-17)(0-11)]
C2N 4.5-30
(C2/C2-A10→D17)
BX12
-ADRS FANOUT 1
[-ADD(1-8)(0-11)]
C2N 4.5-30
(C2/C2-A01→D08)
12112 C09/C09 BITS 0-1
12112 E02/E02 BITS 2-5
12112 E07/E07 BITS 2-5
12112 E04/E04 BITS 10-11
12112 E03/E03 BITS 6-9
12112 E08/E08 BITS 6-9
-ADRS 1 (2-11)
[-PREG1(0-9)/PREG1(2-11)]
C2N 4.0-01
(C2-A06→A08)
2
BIT AUX LSI
2 5-10 C2-C10-36
3 5-7 C2-C10-33
4 5-9 C2-C10-35
5 5-8 C2-C10-34
6 6-20 C2-C09-46
7 6-19 C2-C09-45
8 6-16 C2-C09-42
9 6-17 C2-C09-43
10 2-1 C2-C13-27
11 2-3 C2-C13-29
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
U-MEM ADDRESS FANOUTS
DB-C2PM4:C2/C2
ORDER AGENCY DRG NO 60461830 REV A
SHEET C2N 4.5-32 FILE IV-3-49

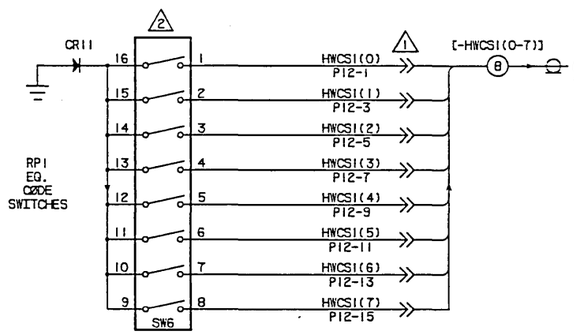


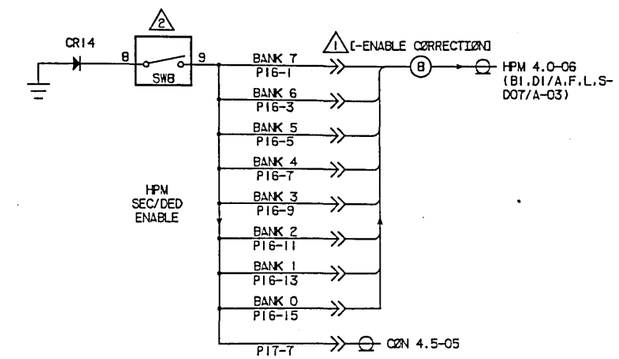


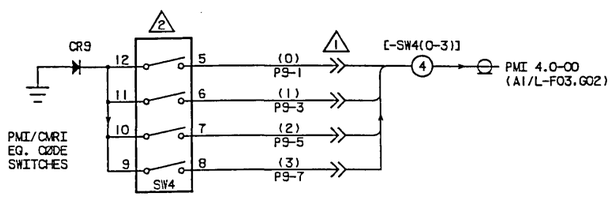


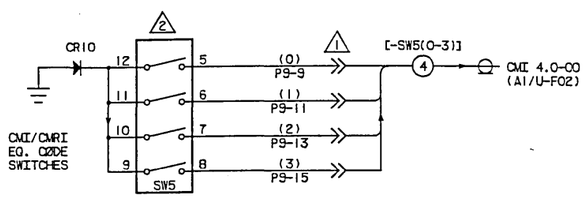


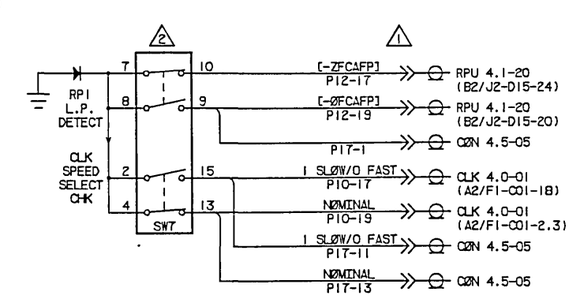












NØTES:

1. ALL EVEN NUMBERED PINS ØN CØNNECTØRS P6 THRØUGH P17 ARE GRØUNDED.
2. ØPEN SWITCH = ØUTPUT = 1
   CLØSED SWITCH = ØUTPUT = 0.

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	LEVEL 4 DIAGRAM EQ. CØDE SWITCH BØARD A1 (REAR)	CODE IDENT / DWG NO 60461830	REV A
		SHEET CØN 4.6-00	PAGE IV-3-51

4. DATA MEMORY UNIT (DMU)

SYSTEM FUNCTION

The data memory unit, which is located in the base processor, stores variables, intermediate operands, and results presented from the crossbar and sends the same data out onto the crossbar.

GENERAL DESCRIPTION

Each base processor has four data memory units, each with 4096-word 16-bit data file and a 16-word 16-bit index file and associated registers and control. The data memory unit takes one clock cycle for any operation. New operands can be accepted and new results can be available each clock cycle.

LOCATION

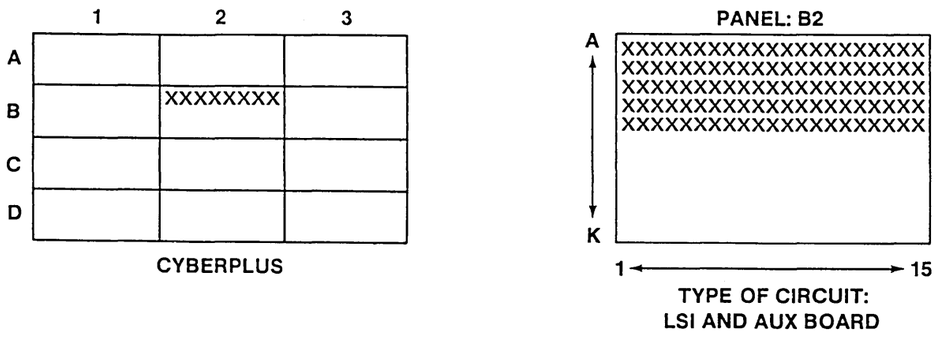


Figure IV-4-1. Location of Data Memory Unit Logic Circuits

FUNCTIONAL DESCRIPTION

The discussion in the following paragraphs refers to the simplified block diagram of the data memory unit as shown in figure IV-4-2 and the level 2 diagram DMU 2.0. The control register receives the 12-bit operation code from the 16-bit dynamic control field of the instruction word. The bits of the operation code determine what function the data memory unit will perform. However, the DMU cannot perform the function unless the enables from the control register and microinstruction register are gated by the presence of the C clock. The load functions controlled by the A and B clocks are not inhibited by the absence of the C clock.

The 12-bit input address (A) register, the 16-bit input data (B) register, receive address and data from the crossbar when enabled by the A and B clocks, respectively. The least significant 12 bits of crossbar output 4(DMU 0), 2(DMU 1), 5(DMU 2), 6(DMU 3) is used as the address in all directly addressed operations on either the 4096-word data file or 16-word index file. The least significant 4 bits of the A register provide the address for the index file. The data in the B register may be written into the data file, the index file, or passed directly to the output register Z. (Note that the data loaded into the B register comes from the same crossbar output as the address loaded into the A register, thereby possibly creating conflicts between address and data during some write operations.)

The 12-bit increment register I, 12-bit address compare register CA, and 16-bit data compare register CD are loaded when enabled by clock C. As was the case for the address register, the increment and address compare registers are loaded from the 12 least significant bits of the crossbar input. The increment register value is the increment/decrement value used to obtain the index address during an increment/decrement instruction. The address compare register provides one of the inputs to the address compare network.

The address specifying the memory location to be accessed in the index file comes from either a ring port unit or the input address register via the address multiplexer. The data to be stored in the index file comes from either the B register, a ring port, or the adder via the index select multiplexer. The output of the index file goes to the adder network where it is incremented or decremented by 1 and then written back into the index file; to the address compare network where it is compared to a program-loaded value, to the output register where it is available to the crossbar, or to the data file as an address.

The address specifying the memory location to be accessed in the data file comes from either the A register, or the least significant 12 bits of the index file via the data address multiplexer. The data to be stored in the data file comes from either the B register or a ring port via the data select multiplexer. The output of the data file goes to the output register or interrupt processing through the data out multiplexer and the data compare logic via the interrupt register.

The adder network performs 2's complement addition or subtraction on the least significant 12-bits of data from the index file. The adder can be set to add or subtract 1 or the value in the increment register. The result is to change the index file entry as required. The output of the adder is written back into the index file at the same location the original, unchanged data was read.

The two compare networks perform a magnitude compare of the current contents of the address compare or data compare register to the address or data of the current data file operation prior to any post increment or decrement. Two types of magnitude compares are performed: one is a 12-bit (address) or 16-bit (data) compare of each value, and the other, for data only, is a 8-bit byte compare where each byte is considered as a separate integer. The output of the compare networks are loaded into the status register.

Besides the compare-equal and compare-greater-than status, the status receives the sign-bit status from the output register. The early status bits, which are available at the same time as the data from the file memories, include the sign-bit and the address compare results. The data compare results are available one clock cycle later.

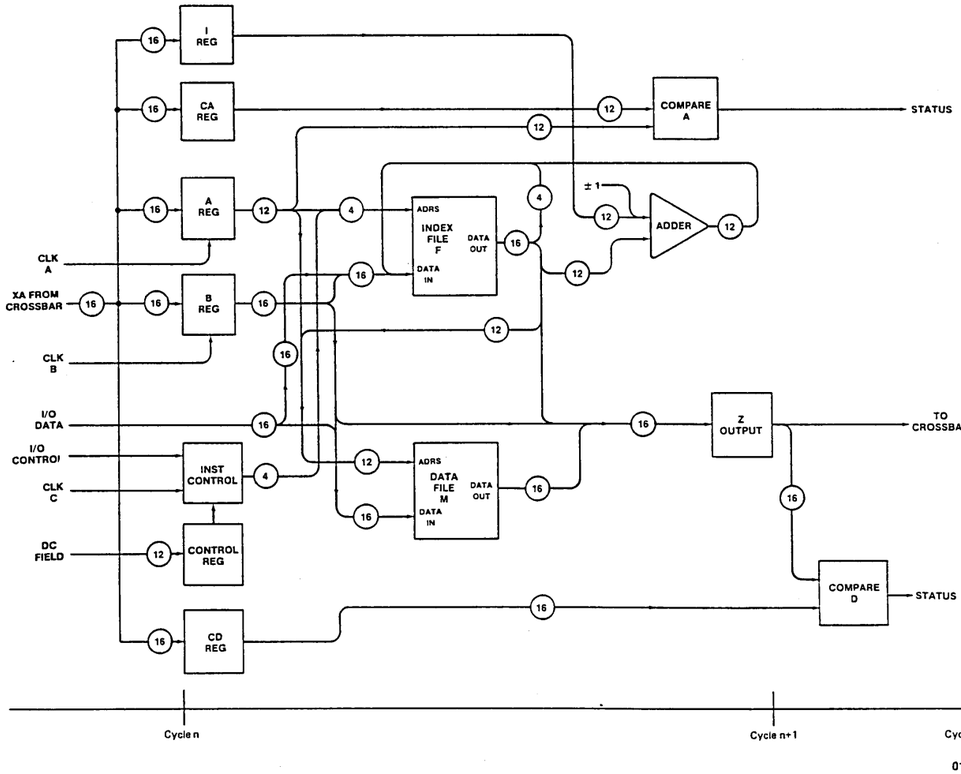


Figure IV-4-2. Data Memory Unit Block Diagram

TIMING

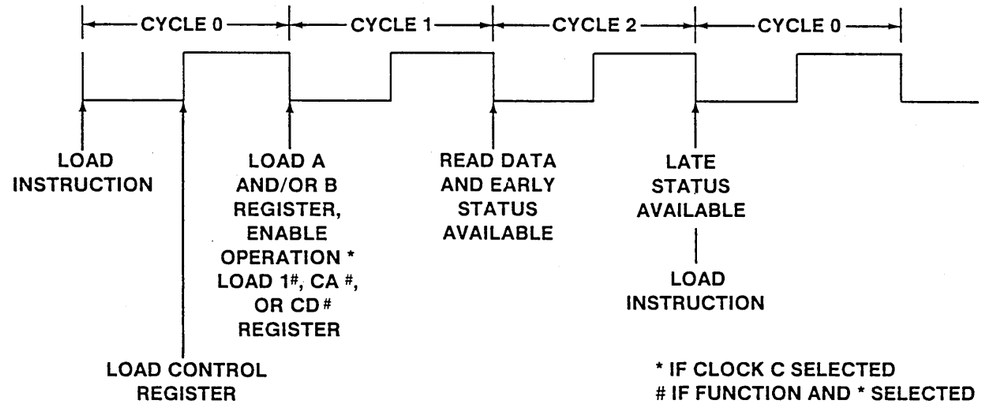
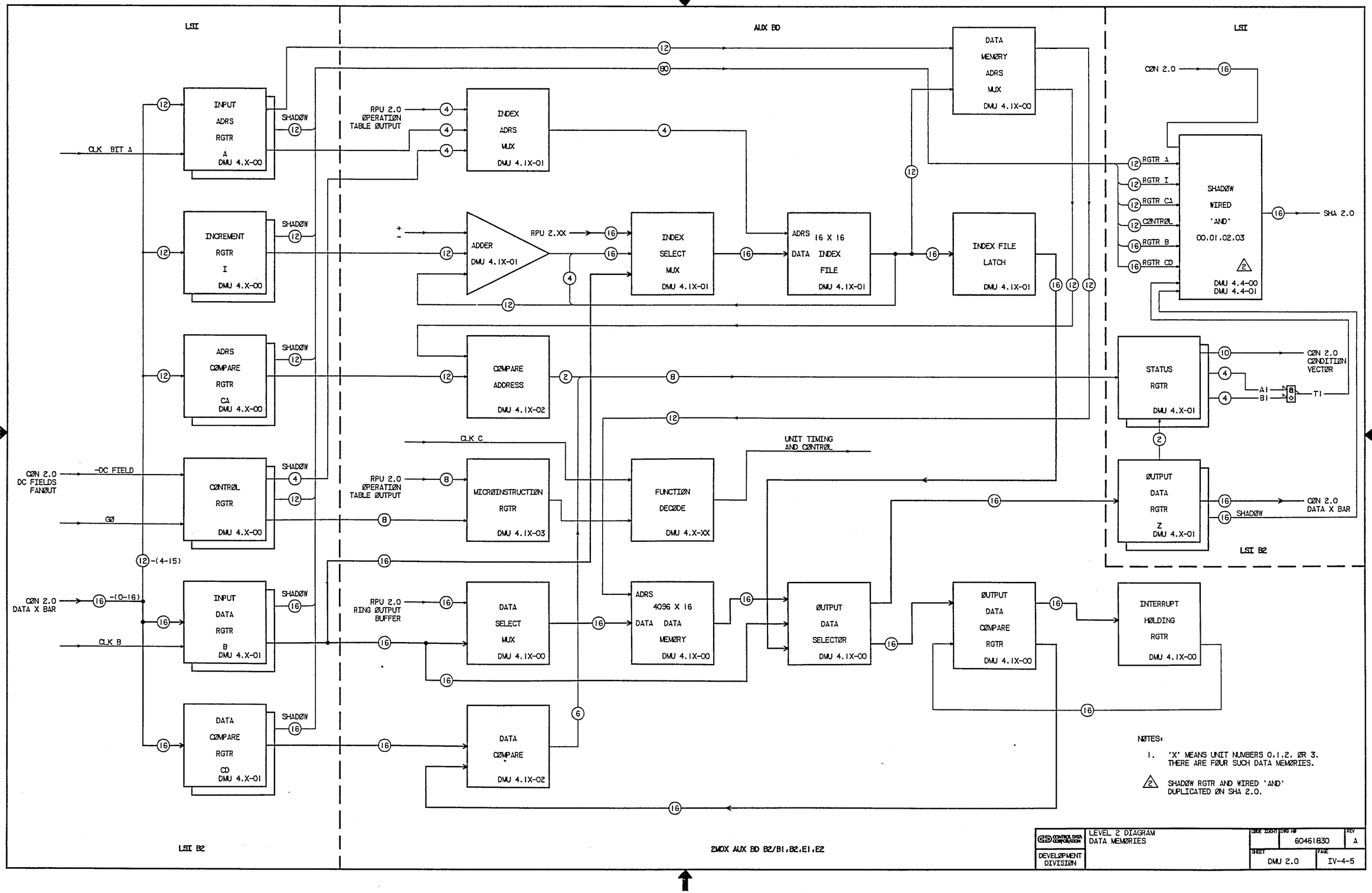
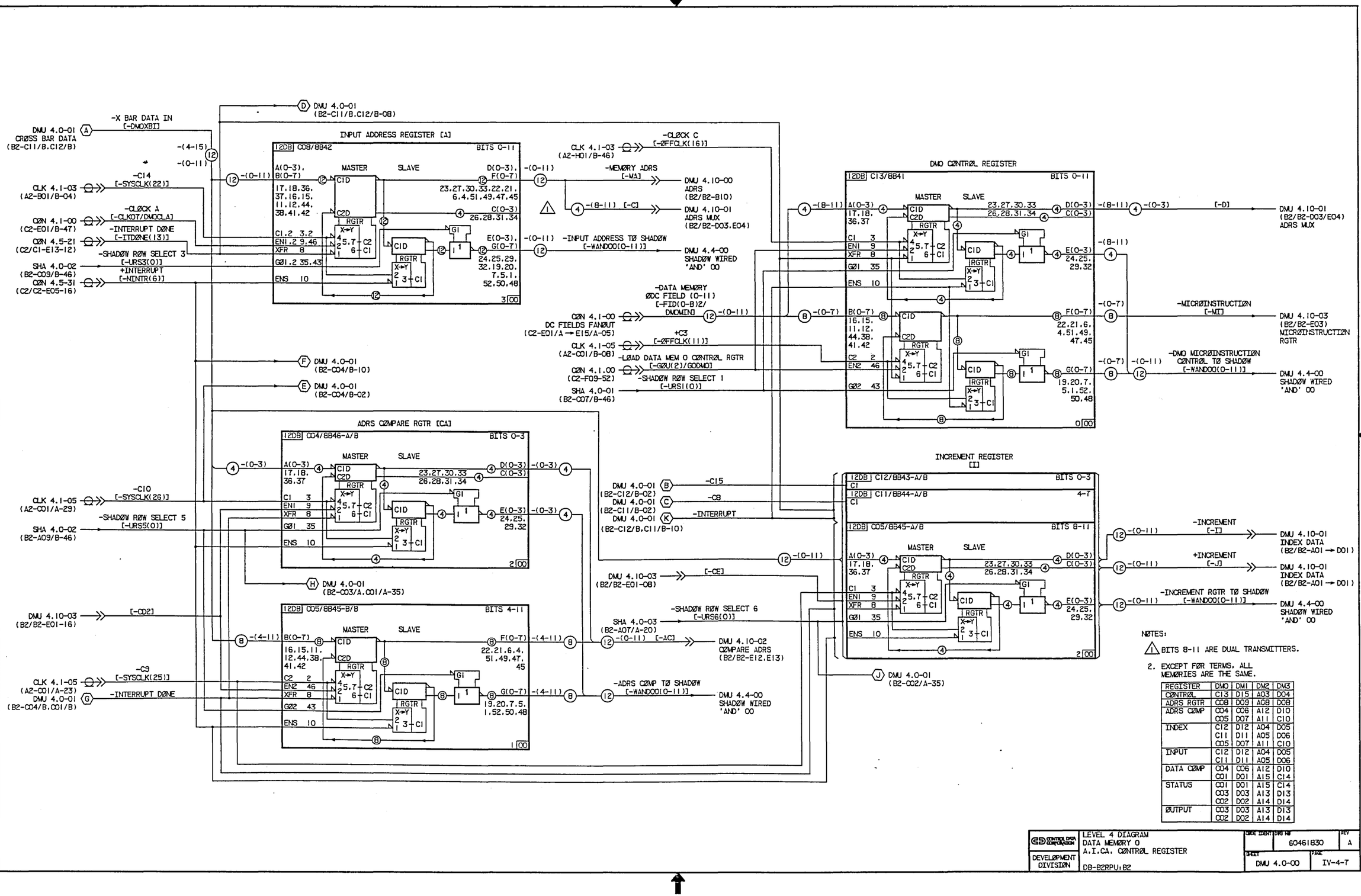
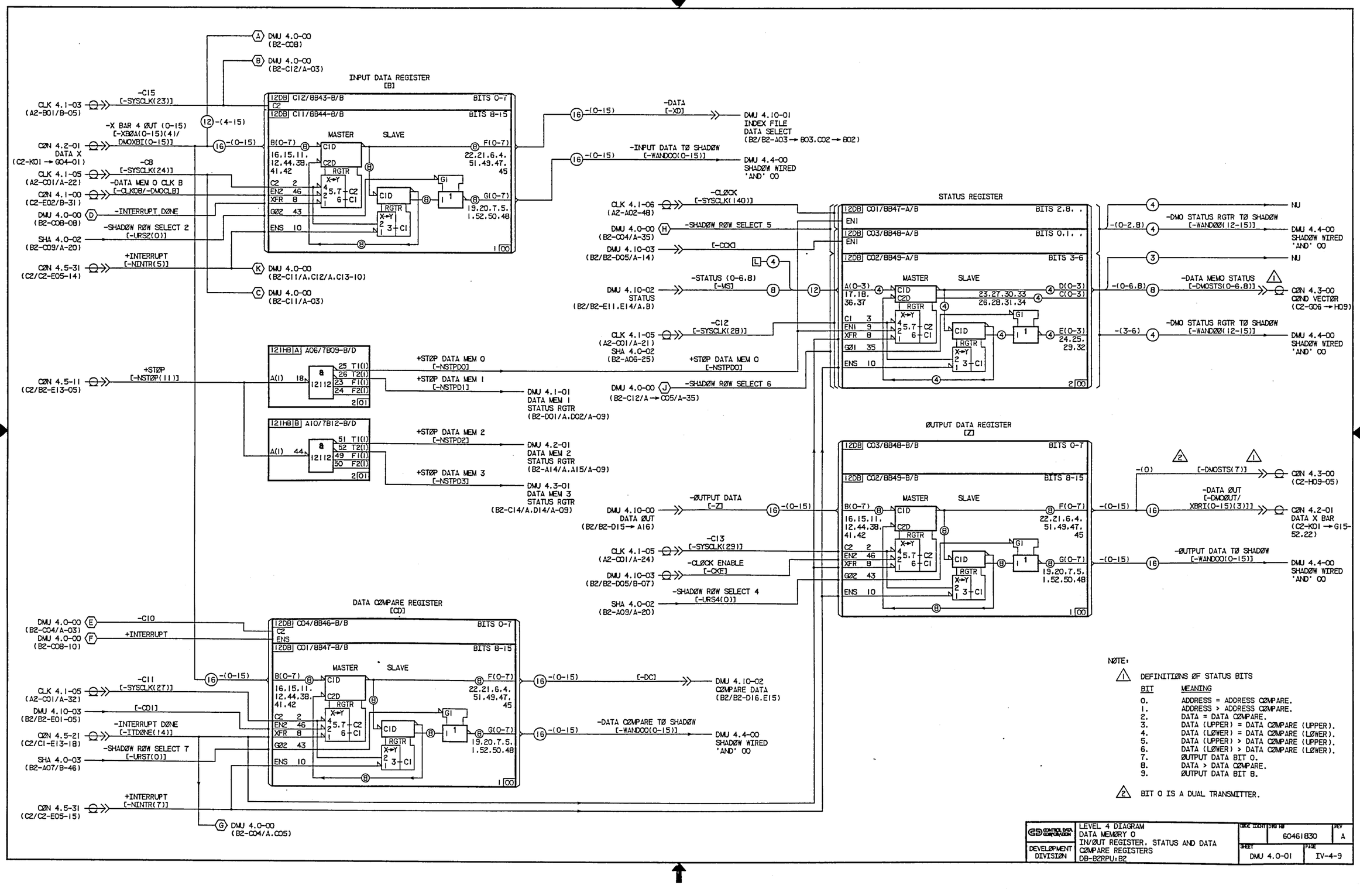

CYCLE 0
CYCLE 1
CYCLE 2
CYCLE 0
LOAD INSTRUCTION
LOAD A AND/OR B REGISTER, ENABLE OPERATION * LOAD 1#, CA #, OR CD # REGISTER
READ DATA AND EARLY STATUS AVAILABLE
LATE STATUS AVAILABLE
LOAD INSTRUCTION
LOAD CONTROL REGISTER
* IF CLOCK C SELECTED
IF FUNCTION AND * SELECTED

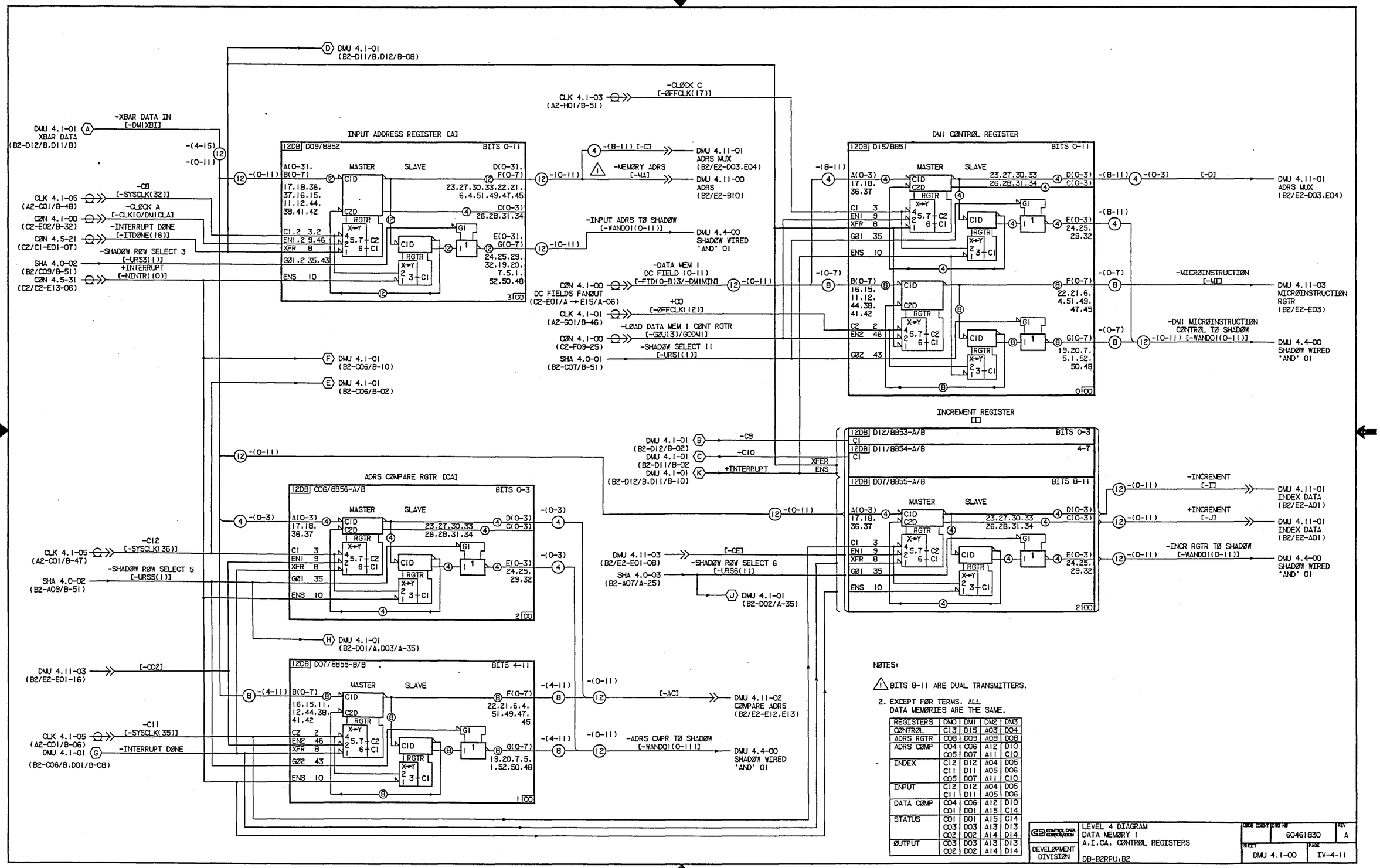
Figure IV-4-3. Data Memory Unit Instructions Timing

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LSI
AUX BD
LSI
INPUT ADRS RGTR A DMU 4.X-00
INCREMENT RGTR I DMU 4.X-00
ADRS COMPARE RGTR CA DMU 4.X-00
CONTROL RGTR DMU 4.X-00
INPUT DATA RGTR B DMU 4.X-01
DATA COMPARE RGTR CD DMU 4.X-01
SHADOW
CLK BIT A
CON 2.0 DC FIELDS FANOUT
-DC FIELD
GO
CON 2.0 DATA X BAR
-(0-16)
CLK B
-(4-15)
RPU 2.0 OPERATION TABLE OUTPUT
INDEX ADRS MUX DMU 4.1X-01
ADDER DMU 4.1X-01
RPU 2.XX
INDEX SELECT MUX DMU 4.1X-01
COMPARE ADDRESS DMU 4.1X-02
CLK C
RPU 2.0 OPERATION TABLE OUTPUT
MICROINSTRUCTION RGTR DMU 4.1X-03
FUNCTION DECODE DMU 4.X-XX
UNIT TIMING AND CONTROL
RPU 2.0 RING OUTPUT BUFFER
DATA SELECT MUX DMU 4.1X-00
DATA COMPARE DMU 4.1X-02
ADRS 4096 X 16 DATA DATA MEMORY DMU 4.1X-00
DATA MEMORY ADRS MUX DMU 4.1X-00
ADRS 16 X 16 DATA INDEX FILE DMU 4.1X-01
INDEX FILE LATCH DMU 4.1X-01
OUTPUT DATA SELECTOR DMU 4.1X-00
OUTPUT DATA COMPARE RGTR DMU 4.1X-00
INTERRUPT HOLDING RGTR DMU 4.1X-00
CON 2.0
RGTR A
RGTR I
RGTR CA
CONTROL
RGTR B
RGTR CD
SHADOW WIRED 'AND' 00.01.02.03
DMU 4.4-00 DMU 4.4-01
SHA 2.0
STATUS RGTR DMU 4.X-01
CON 2.0 CONDITION VECTOR
AI
BI
TI
OUTPUT DATA RGTR Z DMU 4.X-01
CON 2.0 DATA X BAR
SHADOW
LSI B2
NOTES:
1. 'X' MEANS UNIT NUMBERS 0,1,2, OR 3. THERE ARE FOUR SUCH DATA MEMORIES.
2 SHADOW RGTR AND WIRED 'AND' DUPLICATED ON SHA 2.0.
LSI B2
2MOX AUX BD B2/B1,B2,E1,E2
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 2 DIAGRAM
DATA MEMORIES
CODE IDENT NO 60461830
REV A
SHEET DMU 2.0
FILE IV-4-5


INPUT ADDRESS REGISTER [A]
12DB C08/8842
BITS 0-11
MASTER
SLAVE
A(0-3), B(0-7)
17,18,36, 37,16,15, 11,12,44, 38,41,42
C1,2 3,2
EN1,2 9,46
XFR 8
GØ1,2 35,43
ENS 10
D(0-3), F(0-7)
23,27,30,33,22,21, 6,4,51,49,47,45
C(0-3)
26,28,31,34
E(0-3), G(0-7)
24,25,29, 32,19,20, 7,5,1, 52,50,48
3 00
-X BAR DATA IN [-DMOXB(]
DMU 4.0-01 CRØSS BAR DATA (B2-C11/B,C12/B)
-C14 [-SYSCLK(22)]
CLK 4.1-03 (A2-B01/B-04)
-CLØCK A [-CLKOT/DMOCLA]
C2N 4.1-00 (C2-E01/B-47)
-INTERRUPT DØNE [-ITDØNE(13)]
C2N 4.5-21 (C2/C1-E13-12)
-SHADØW RØW SELECT 3 [-URS3(0)]
SHA 4.0-02 (B2-C09/B-46)
+INTERRUPT [-NINTR(6)]
C2N 4.5-31 (C2/C2-E05-16)
DMU 4.0-01 (B2-C11/B,C12/B-08)
DMU 4.0-01 (B2-C04/B-10)
DMU 4.0-01 (B2-C04/B-02)
-CLØCK C [-ØFFCLK(16)]
CLK 4.1-03 (A2-H01/B-46)
-MEMØRY ADRS [-MA]
DMU 4.10-00 ADRS (B2/B2-B10)
DMU 4.10-01 ADRS MUX (B2/B2-D03,E04)
-INPUT ADDRESS TØ SHADØW [-WANDOO(0-11)]
DMU 4.4-00 SHADØW WIRED 'AND' 00
-DATA MEMØRY ØDC FIELD (0-11) [-FID(0-8)2/ DMOMIND
C2N 4.1-00 DC FIELDS FANØUT (C2-E01/A → E15/A-05)
+C3 [-ØFFCLK(11)]
CLK 4.1-05 (A2-C01/B-08)
-LØAD DATA MEM 0 CØNTRØL RGTR [-GØU(2)/GODMO]
C2N 4.1-00 (C2-F09-52)
-SHADØW RØW SELECT 1 [-URS1(0)]
SHA 4.0-01 (B2-C07/B-46)
DMU 4.10-03 (B2/B2-E01-08)
[-CE]
DMU 4.0-01 (B2-C02/A-35)
DMO CØNTRØL REGISTER
12DB C13/8841
BITS 0-11
MASTER
SLAVE
A(0-3) 17,18, 36,37
B(0-7) 16,15, 11,12, 44,38, 41,42
C1 3
EN1 9
XFR 8
GØ1 35
GØ2 43
ENS 10
C2 2
EN2 46
23,27,30,33
26,28,31,34
E(0-3) 24,25, 29,32
F(0-7) 22,21,6, 4,51,49, 47,45
G(0-7) 19,20,7, 5,1,52, 50,48
0 00
DMU 4.10-01 (B2/B2-D03/E04) ADRS MUX
-MICRØINSTRUCTIØN [-MI]
DMU 4.10-03 (B2/B2-E03) MICRØINSTRUCTIØN RGTR
-DMO MICRØINSTRUCTIØN CØNTRØL TØ SHADØW [-WANDOO(0-11)]
DMU 4.4-00 SHADØW WIRED 'AND' 00
ADRS CØMPARE RGTR [CA]
12DB CO4/8846-A/B
BITS 0-3
MASTER
SLAVE
A(0-3) 17,18, 36,37
C1 3
EN1 9
XFR 8
GØ1 35
ENS 10
23,27,30,33
26,28,31,34
E(0-3) 24,25, 29,32
2 00
-C10 [-SYSCLK(26)]
CLK 4.1-05 (A2-C01/A-29)
-SHADØW RØW SELECT 5 [-URS5(0)]
SHA 4.0-02 (B2-A09/B-46)
DMU 4.0-01 (B2-C03/A,C01/A-35)
12DB C05/8845-B/B
BITS 4-11
MASTER
SLAVE
B(0-7) 16,15,11, 12,44,38, 41,42
C2 2
EN2 46
XFR 8
GØ2 43
ENS 10
F(0-7) 22,21,6,4, 51,49,47, 45
G(0-7) 19,20,7,5, 1,52,50,48
1 00
DMU 4.10-03 (B2/B2-E01-16)
[-CD2]
-C9 [-SYSCLK(25)]
CLK 4.1-05 (A2-C01/A-23)
DMU 4.0-01 (B2-C04/B,C01/B)
-INTERRUPT DØNE
DMU 4.0-01 (B2-C12/B-02)
-C15
DMU 4.0-01 (B2-C11/B-02)
-C8
DMU 4.0-01 (B2-C12/B,C11/B-10)
-INTERRUPT
SHA 4.0-03 (B2-A07/A-20)
-SHADØW RØW SELECT 6 [-URS6(0)]
DMU 4.10-02 CØMPARE ADRS (B2/B2-E12,E13)
-ADRS CØMP TØ SHADØW [-WANDOO(0-11)]
DMU 4.4-00 SHADØW WIRED 'AND' 00
INCREMENT REGISTER [I]
12DB C12/8843-A/B
BITS 0-3
12DB C11/8844-A/B
4-7
12DB C05/8845-A/B
BITS 8-11
MASTER
SLAVE
A(0-3) 17,18, 36,37
C1 3
EN1 9
XFR 8
GØ1 35
ENS 10
23,27,30,33
26,28,31,34
E(0-3) 24,25, 29,32
2 00
-INCREMENT [-I]
DMU 4.10-01 INDEX DATA (B2/B2-A01 → D01)
+INCREMENT [-J]
DMU 4.10-01 INDEX DATA (B2/B2-A01 → D01)
-INCREMENT RGTR TØ SHADØW [-WANDOO(0-11)]
DMU 4.4-00 SHADØW WIRED 'AND' 00
NØTES:
1. BITS 8-11 ARE DUAL TRANSMITTERS.
2. EXCEPT FØR TERMS, ALL MEMØRIES ARE THE SAME.
REGISTER | DM0 | DM1 | DM2 | DM3
CØNTRØL | C13 | D15 | A03 | D04
ADRS RGTR | C08 | D09 | A08 | D08
ADRS CØMP | C04 | C06 | A12 | D10
C05 | D07 | A11 | C10
INDEX | C12 | D12 | A04 | D05
C11 | D11 | A05 | D06
C05 | D07 | A11 | C10
INPUT | C12 | D12 | A04 | D05
C11 | D11 | A05 | D06
DATA CØMP | C04 | C06 | A12 | D10
C01 | D01 | A15 | C14
STATUS | C01 | D01 | A15 | C14
C03 | D03 | A13 | D13
C02 | D02 | A14 | D14
ØUTPUT | C03 | D03 | A13 | D13
C02 | D02 | A14 | D14
CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 4 DIAGRAM
DATA MEMØRY 0
A,I,CA, CØNTRØL REGISTER
DB-B2RPU:B2
CODE IDENT
DWG NO
60461830
REV
A
SHEET
DMU 4.0-00
PAGE
IV-4-7


INPUT DATA REGISTER [B]
STATUS REGISTER
ØUTPUT DATA REGISTER [Z]
DATA CØMPARE REGISTER [CD]
MASTER
SLAVE
CLK 4.1-03 (A2-B01/B-05)
-C15 [-SYSCLK(23)]
-X BAR 4 ØUT (0-15) [-XBØA(0-15)(4)/ DMOXBI(0-15)]
CØN 4.2-01 DATA X (C2-K01 → G04-01)
CLK 4.1-05 (A2-C01/A-22)
-C8 [-SYSCLK(24)]
-DATA MEM 0 CLK B [-CLKDB/-DMOCLB]
CØN 4.1-00 (C2-E02/B-31)
DMU 4.0-00 (B2-C08-08)
-INTERRUPT DØNE
SHA 4.0-02 (B2-C09/A-20)
-SHADØW RØW SELECT 2 [-URS2(0)]
CØN 4.5-31 (C2/C2-E05-14)
+INTERRUPT [-NINTR(5)]
DMU 4.0-00 (B2-C08-00)
DMU 4.0-00 (B2-C12/A-03)
DMU 4.0-00 (B2-C11/A,C12/A,C13-10)
DMU 4.0-00 (B2-C11/A-03)
-DATA [-XD]
DMU 4.10-01 INDEX FILE DATA SELECT (B2/B2-A03 → B03.C02 → B02)
-INPUT DATA TØ SHADØW [-WANDØØ(0-15)]
DMU 4.4-00 SHADØW WIRED 'AND' 00
CLK 4.1-06 (A2-A02-48)
-CLØCK [-SYSCLK(140)]
DMU 4.0-00 (B2-C04/A-35)
-SHADØW RØW SELECT 5
DMU 4.10-03 (B2/B2-D05/A-14)
[-CØCI]
DMU 4.10-02 STATUS (B2/B2-E11,E14/A,B)
-STATUS (0-6,8) [-MS]
CLK 4.1-05 (A2-C01/A-21)
SHA 4.0-02 (B2-A06-25)
-C12 [-SYSCLK(28)]
+STØP DATA MEM 0 [-NSTPD0]
DMU 4.0-00 (B2-C12/A → C05/A-35)
-SHADØW RØW SELECT 6
CØN 4.5-11 (C2/B2-E13-05)
+STØP [-NSTØP(11)]
+STØP DATA MEM 1 [-NSTPD1]
DMU 4.1-01 DATA MEM 1 STATUS RGTR (B2-D01/A,D02/A-09)
+STØP DATA MEM 2 [-NSTPD2]
DMU 4.2-01 DATA MEM 2 STATUS RGTR (B2-A14/A,A15/A-09)
+STØP DATA MEM 3 [-NSTPD3]
DMU 4.3-01 DATA MEM 3 STATUS RGTR (B2-C14/A,D14/A-09)
DMU 4.10-00 DATA ØUT (B2/B2-D15 → A16)
-ØUTPUT DATA [-Z]
CLK 4.1-05 (A2-C01/A-24)
-C13 [-SYSCLK(29)]
DMU 4.10-03 (B2/B2-D05/B-07)
-CLØCK ENABLE [-CKE]
SHA 4.0-02 (B2-A09/A-20)
-SHADØW RØW SELECT 4 [-URS4(0)]
DMU 4.0-00 (B2-C04/A-03)
DMU 4.0-00 (B2-C08-10)
-C10
+INTERRUPT
CLK 4.1-05 (A2-C01/A-32)
-C11 [-SYSCLK(27)]
DMU 4.10-03 (B2/B2-E01-05)
[-CØI]
CØN 4.5-21 (C2/C1-E13-18)
-INTERRUPT DØNE [-ITDØNE(14)]
SHA 4.0-03 (B2-A07/B-46)
-SHADØW RØW SELECT 7 [-URS7(0)]
CØN 4.5-31 (C2/C2-E05-15)
+INTERRUPT [-NINTR(7)]
DMU 4.0-00 (B2-C04/A.C05)
DMU 4.10-02 CØMPARE DATA (B2/B2-D16.E15)
[-DC]
-DATA CØMPARE TØ SHADØW [-WANDØØ(0-15)]
DMU 4.4-00 SHADØW WIRED 'AND' 00
-DMØ STATUS RGTR TØ SHADØW [-WANDØØ(12-15)]
DMU 4.4-00 SHADØW WIRED 'AND' 00
NU
-DATA MEMØ STATUS [-DMOSTS(0-6,8)]
CØN 4.3-00 CØND VECTØR (C2-G06 → H09)
-DMØ STATUS RGTR TØ SHADØW [-WANDØØ(12-15)]
DMU 4.4-00 SHADØW WIRED 'AND' 00
-ØUTPUT DATA TØ SHADØW [-WANDØØ(0-15)]
-DATA ØUT [-DMOØUT/ XBRI(0-15)(3)]]
CØN 4.2-01 DATA X BAR (C2-K01 → G15-52.22)
-(0) [-DMOSTS(7)]
CØN 4.3-00 (C2-H09-05)
NØTE:
1 DEFINITIØNS ØF STATUS BITS
BIT MEANING
0. ADDRESS = ADDRESS CØMPARE.
1. ADDRESS > ADDRESS CØMPARE.
2. DATA = DATA CØMPARE.
3. DATA (UPPER) = DATA CØMPARE (UPPER).
4. DATA (LØWER) = DATA CØMPARE (LØWER).
5. DATA (UPPER) > DATA CØMPARE (UPPER).
6. DATA (LØWER) > DATA CØMPARE (LØWER).
7. ØUTPUT DATA BIT 0.
8. DATA > DATA CØMPARE.
9. ØUTPUT DATA BIT 8.
2 BIT 0 IS A DUAL TRANSMITTER.
LEVEL 4 DIAGRAM
DATA MEMØRY 0
IN/ØUT REGISTER, STATUS AND DATA CØMPARE REGISTERS
DB-B2RPU:B2
DEVELØPMENT DIVISIØN
60461830
A
DMU 4.0-01
IV-4-9



NØTES:

⚠1 BITS 8-11 ARE DUAL TRANSMITTERS.

2. EXCEPT FØR TERMS. ALL DATA MEMØRIES ARE THE SAME.

REGISTERS	DM0	DM1	DM2	DM3
CØNTRØL	C13	D15	A03	D04
ADRS RGTR	C08	D09	A08	D08
ADRS CØMP	C04	C06	A12	D10
	C05	D07	A11	C10
INDEX	C12	D12	A04	D05
	C11	D11	A05	D06
	C05	D07	A11	C10
INPUT	C12	D12	A04	D05
	C11	D11	A05	D06
DATA CØMP	C04	C06	A12	D10
	C01	D01	A15	C14
STATUS	C01	D01	A15	C14
	C03	D03	A13	D13
	C02	D02	A14	D14
ØUTPUT	C03	D03	A13	D13
	C02	D02	A14	D14

CONTROL DATA CORPORATION

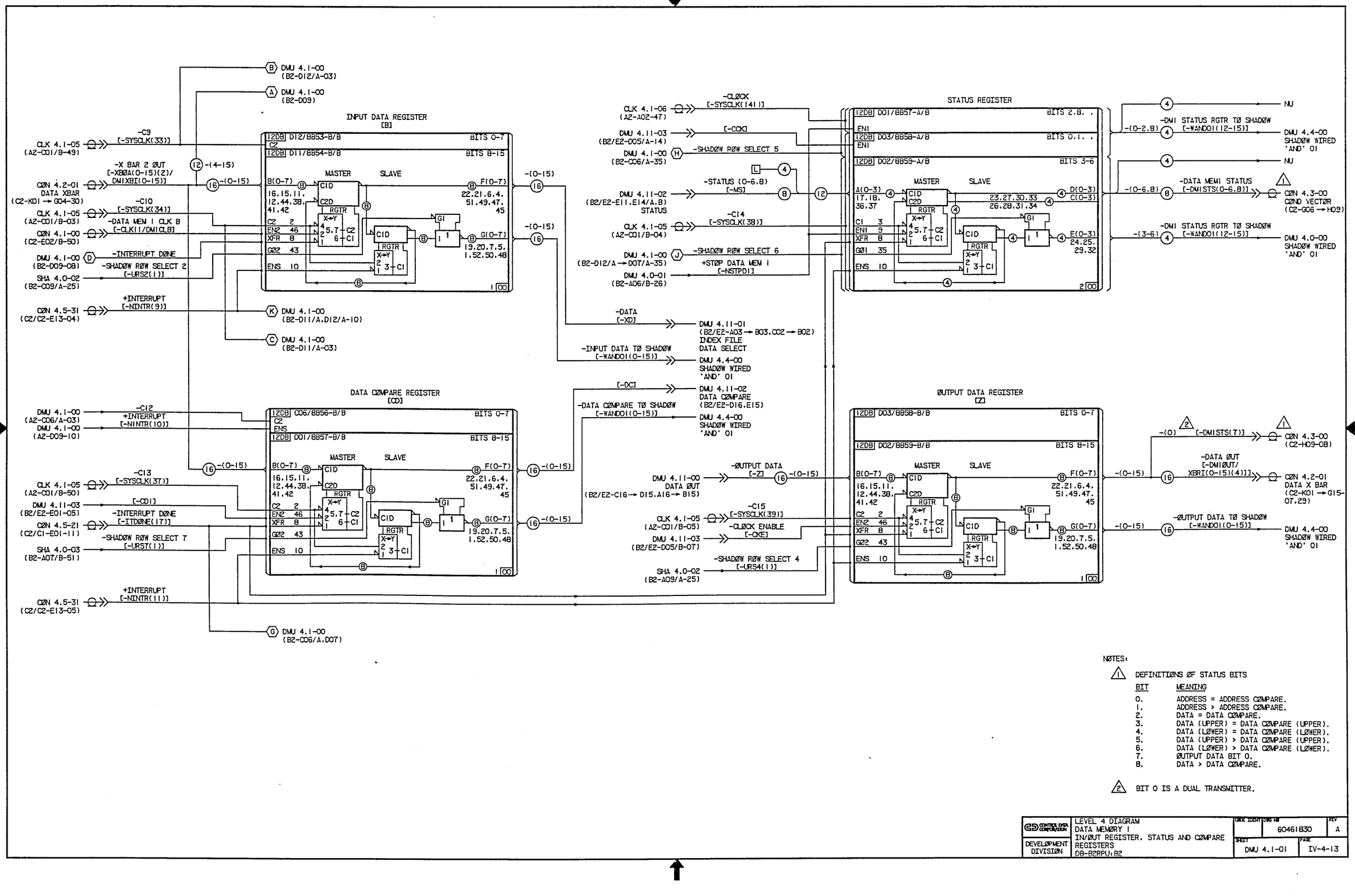
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
DATA MEMØRY I
A.I.CA. CØNTRØL REGISTERS

DB-B2RPU:B2

DRGE IDENT 60461830 REV A

SHEET DMU 4.1-00 PAGE IV-4-11

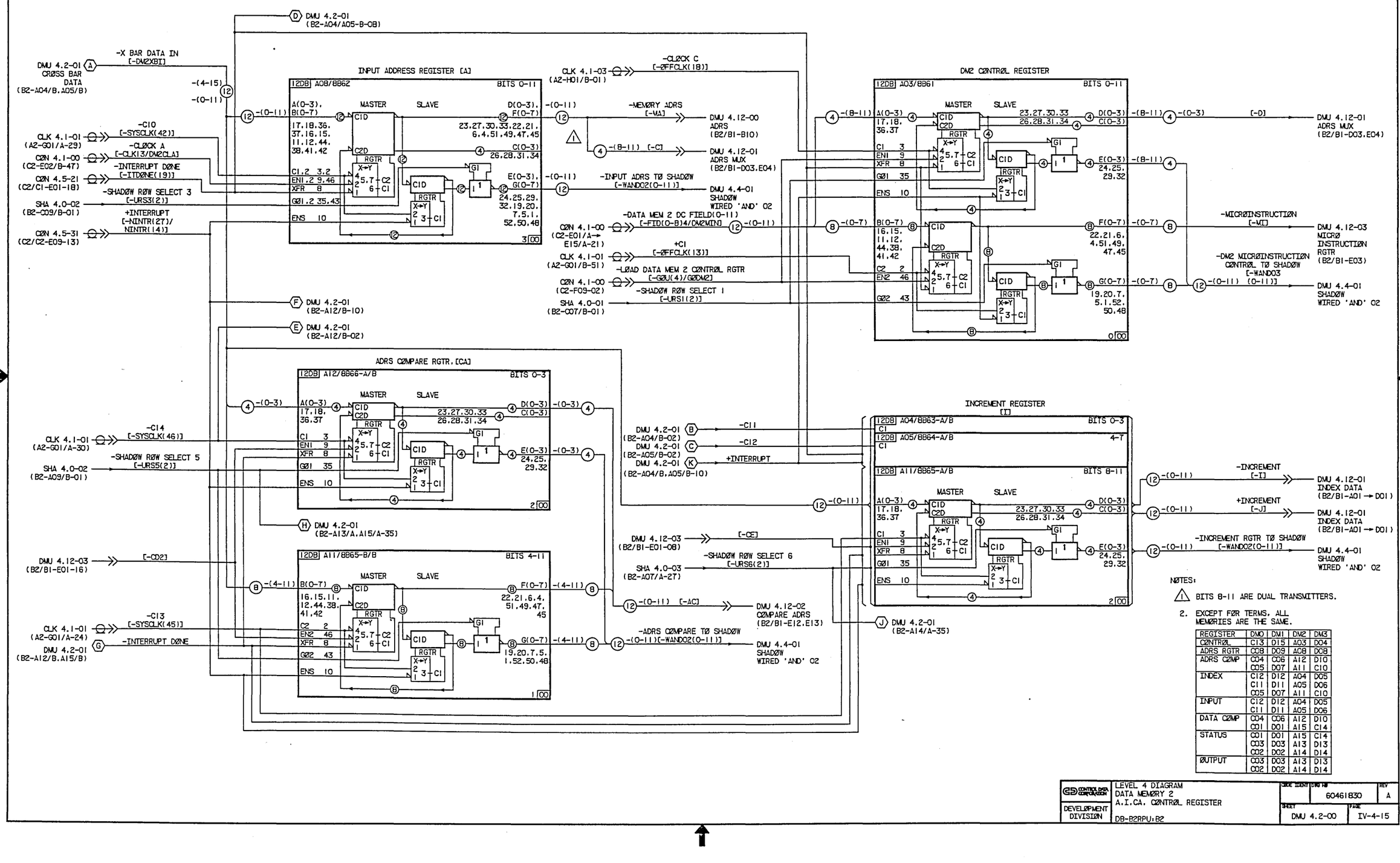


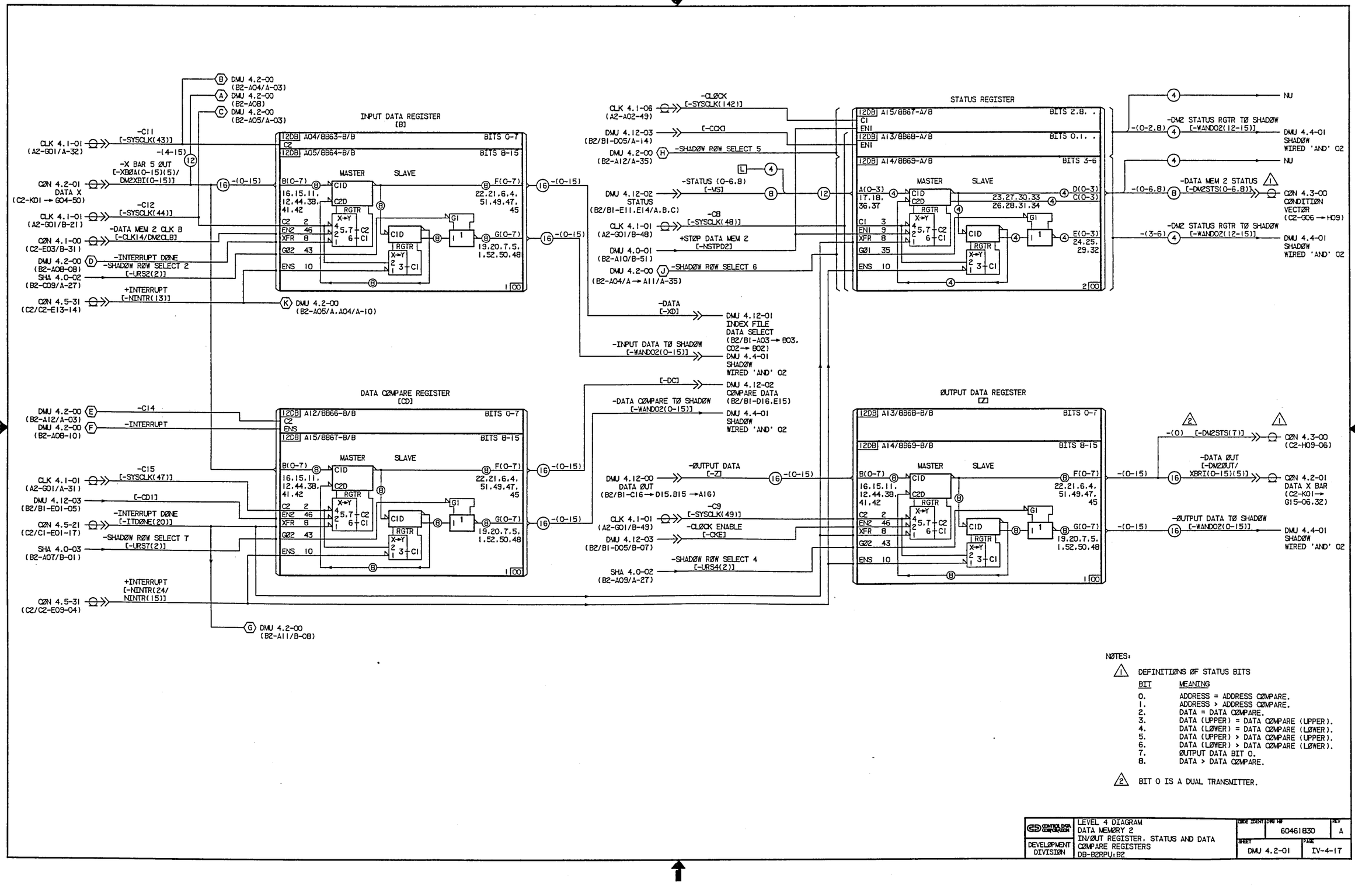
NØTES:

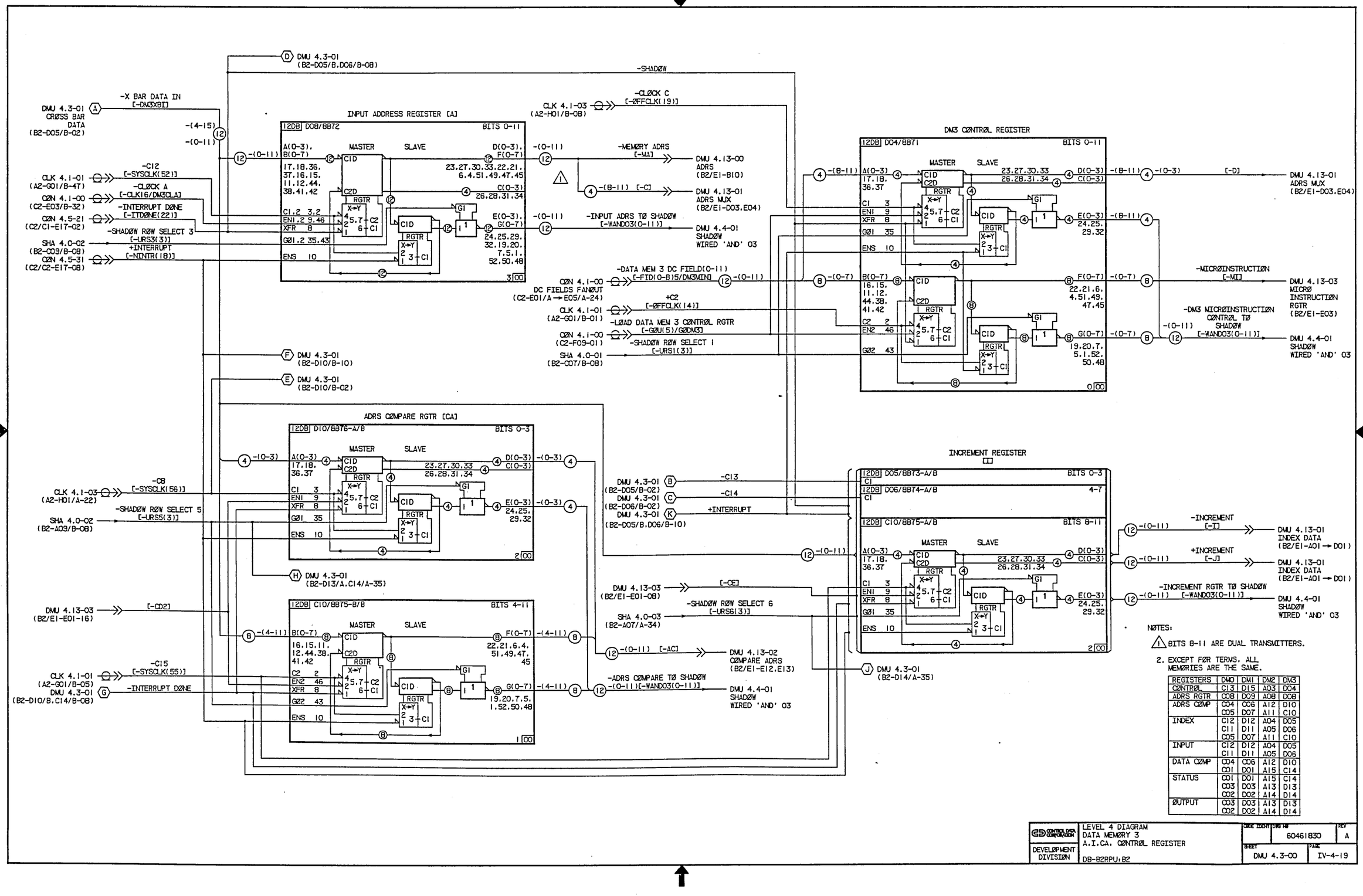
⚠1 DEFINITIØNS ØF STATUS BITS

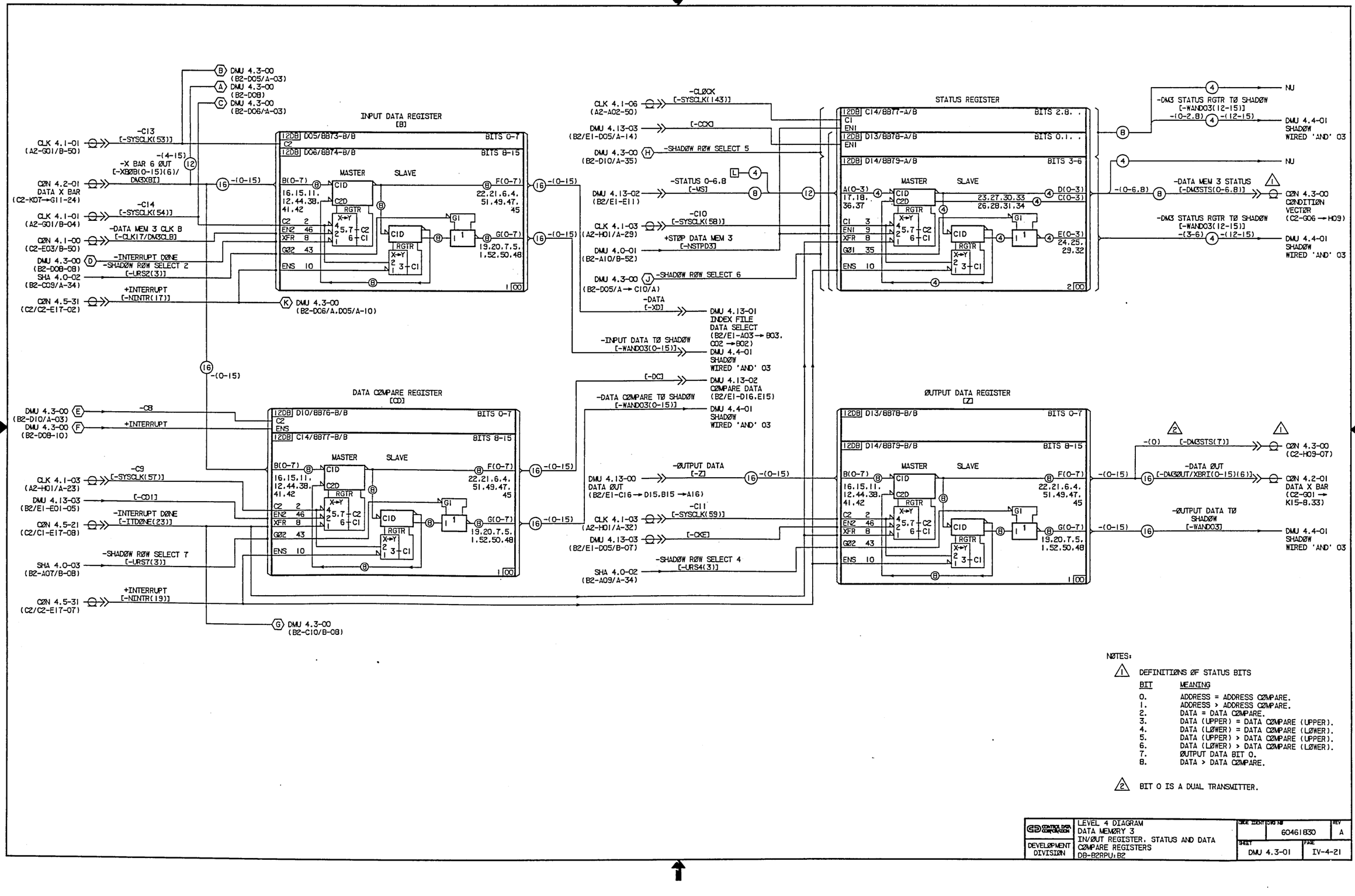
BIT	MEANING
0.	ADDRESS = ADDRESS CØMPARE.
1.	ADDRESS > ADDRESS CØMPARE.
2.	DATA = DATA CØMPARE.
3.	DATA (UPPER) = DATA CØMPARE (UPPER).
4.	DATA (LØWER) = DATA CØMPARE (LØWER).
5.	DATA (UPPER) > DATA CØMPARE (UPPER).
6.	DATA (LØWER) > DATA CØMPARE (LØWER).
7.	ØUTPUT DATA BIT 0.
8.	DATA > DATA CØMPARE.

⚠2 BIT 0 IS A DUAL TRANSMITTER.


INPUT ADDRESS REGISTER [A]
12DB A08/8B62
BITS 0-11
MASTER
SLAVE
A(0-3), B(0-7)
17,18,36,37,16,15,11,12,44,38,41,42
C1,2 3,2
ENI,2 9,46
XFR 8
GØI,2 35,43
ENS 10
D(0-3), F(0-7)
23,27,30,33,22,21,6,4,51,49,47,45
C(0-3) 26,28,31,34
E(0-3), G(0-7)
24,25,29,32,19,20,7,5,1,52,50,48
3 00
-X BAR DATA IN [-DM2XBI]
DMU 4.2-01 CRØSS BAR DATA (B2-A04/B, A05/B)
-CIØ [-SYSCLK(42)]
CLK 4.1-01 (A2-GØ1/A-29)
-CLØCK A [-CLK13/DM2CLA]
CØN 4.1-00 (C2-E02/B-47)
-INTERRUPT DØNE [-ITDØNE(19)]
CØN 4.5-21 (C2/C1-E01-18)
-SHADØW RØW SELECT 3 [-URS3(2)]
SHA 4.0-02 (B2-C09/B-01)
+INTERRUPT [-NINTR(27)/ NINTR(14)]
CØN 4.5-31 (C2/C2-E09-13)
-CLØCK C [-ØFFCLK(18)]
CLK 4.1-03 (A2-H01/B-01)
-MEMØRY ADRS [-MA]
DMU 4.12-00 ADRS (B2/B1-B10)
DMU 4.12-01 ADRS MUX (B2/B1-D03,E04)
-INPUT ADRS TØ SHADØW [-WAND02(0-11)]
DMU 4.4-01 SHADØW WIRED 'AND' 02
-DATA MEM 2 DC FIELD(0-11) [-FIDL(0-8)4/DM2WDIN]
CØN 4.1-00 (C2-E01/A→E15/A-21)
+CI [-ØFFCLK(13)]
CLK 4.1-01 (A2-GØ1/B-51)
-LØAD DATA MEM 2 CØNTRØL RGTR [-GØU(4)/GØDM2]
CØN 4.1-00 (C2-F09-02)
-SHADØW RØW SELECT 1 [-URS1(2)]
SHA 4.0-01 (B2-C07/B-01)
DMU 4.2-01 (B2-A04/A05-B-08)
DMU 4.2-01 (B2-A12/B-10)
DMU 4.2-01 (B2-A12/B-02)
DM2 CØNTRØL REGISTER
12DB A03/8B61
BITS 0-11
A(0-3) 17,18,36,37
C1 3
ENI 9
XFR 8
GØI 35
ENS 10
B(0-7) 16,15,11,12,44,38,41,42
C2 2
EN2 46
GØ2 43
D(0-3), F(0-7) 23,27,30,33,22,21,6,4,51,49,47,45
C(0-3) 26,28,31,34
E(0-3), G(0-7) 24,25,29,32,19,20,7,5,1,52,50,48
0 00
-MICRØINSTRUCTIØN [-MI]
DMU 4.12-03 MICRØ INSTRUCTIØN RGTR (B2/B1-E03)
-DM2 MICRØINSTRUCTIØN CØNTRØL TØ SHADØW [-WAND03]
DMU 4.4-01 SHADØW WIRED 'AND' 02
DMU 4.12-01 ADRS MUX (B2/B1-D03,E04)
ADRS CØMPARE RGTR, [CA]
12DB A12/8B66-A/B
BITS 0-3
-CI4 [-SYSCLK(46)]
CLK 4.1-01 (A2-GØ1/A-30)
-SHADØW RØW SELECT 5 [-URS5(2)]
SHA 4.0-02 (B2-A09/B-01)
2 00
DMU 4.2-01 (B2-A13/A, A15/A-35)
12DB A11/8B65-B/B
BITS 4-11
B(0-7) 16,15,11,12,44,38,41,42
C2 2
EN2 46
GØ2 43
F(0-7) 22,21,6,4,51,49,47,45
G(0-7) 19,20,7,5,1,52,50,48
1 00
DMU 4.12-03 (B2/B1-E01-16)
-CI3 [-SYSCLK(45)]
CLK 4.1-01 (A2-GØ1/A-24)
-INTERRUPT DØNE
DMU 4.2-01 (B2-A12/B, A15/B)
DMU 4.2-01 (B2-A04/B-02) -CI1
DMU 4.2-01 (B2-A05/B-02) -CI2
DMU 4.2-01 (B2-A04/B, A05/B-10) +INTERRUPT
DMU 4.12-03 (B2/B1-E01-08) [-CE]
-SHADØW RØW SELECT 6 [-URS6(2)]
SHA 4.0-03 (B2-A07/A-27)
-ADRS CØMPARE TØ SHADØW
DMU 4.12-02 CØMPARE ADRS (B2/B1-E12,E13)
DMU 4.4-01 SHADØW WIRED 'AND' 02
INCREMENT REGISTER [I]
12DB A04/8B63-A/B
BITS 0-3
12DB A05/8B64-A/B
4-7
12DB A11/8B65-A/B
BITS 8-11
-INCREMENT [-I]
DMU 4.12-01 INDEX DATA (B2/B1-A01→D01)
+INCREMENT [-J]
DMU 4.12-01 INDEX DATA (B2/B1-A01→D01)
-INCREMENT RGTR TØ SHADØW [-WAND02(0-11)]
DMU 4.4-01 SHADØW WIRED 'AND' 02
DMU 4.2-01 (B2-A14/A-35)
NØTES:
1. BITS 8-11 ARE DUAL TRANSMITTERS.
2. EXCEPT FØR TERMS, ALL MEMØRIES ARE THE SAME.
REGISTER | DMØ | DM1 | DM2 | DM3
CØNTRØL | C13 | D15 | A03 | D04
ADRS RGTR | C08 | D09 | A08 | D08
ADRS CØMP | C04 | C06 | A12 | D10
C05 | D07 | A11 | C10
INDEX | C12 | D12 | A04 | D05
C11 | D11 | A05 | D06
C05 | D07 | A11 | C10
INPUT | C12 | D12 | A04 | D05
C11 | D11 | A05 | D06
DATA CØMP | C04 | C06 | A12 | D10
C01 | D01 | A15 | C14
STATUS | C01 | D01 | A15 | C14
C03 | D03 | A13 | D13
C02 | D02 | A14 | D14
ØUTPUT | C03 | D03 | A13 | D13
C02 | D02 | A14 | D14
CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 4 DIAGRAM
DATA MEMØRY 2
A.I.CA, CØNTRØL REGISTER
DB-B2RPU:B2
60461830
A
SHEET DMU 4.2-00
PAGE IV-4-15


INPUT DATA REGISTER [B]
DATA COMPARE REGISTER [CD]
STATUS REGISTER
OUTPUT DATA REGISTER [Z]
MASTER
SLAVE
-CLOCK [-SYSCLK(142)]
-STATUS (0-6,8) [-MS]
-SHADOW ROW SELECT 5
-SHADOW ROW SELECT 6
-SHADOW ROW SELECT 7 [-URS7(2)]
-SHADOW ROW SELECT 4 [-URS4(2)]
-SHADOW ROW SELECT 2 [-URS2(2)]
+STOP DATA MEM 2 [-NSTPD2]
-INTERRUPT DONE
-INPUT DATA TO SHADOW [-WANDO2(0-15)]
-DATA COMPARE TO SHADOW [-WANDO2(0-15)]
-OUTPUT DATA TO SHADOW [-WANDO2(0-15)]
-DATA MEM 2 STATUS [-DM2STS(0-6,8)]
-DATA OUT [-DM2DOUT/ XBRI(0-15)(5)]
+INTERRUPT [-NINTR(13)]
+INTERRUPT [-NINTR(24/ NINTR(15)]
-INTERRUPT
-C11
-C12
-C14
-C15
-X BAR 5 OUT [-XB00(0-15)(5)/ DM2XBI(0-15)]
-DATA MEM 2 CLK B [-CLK14/DM2CLB]
-DATA
-OUTPUT DATA
-C9
-CB
-CLOCK ENABLE [-CKE]
-DC
-DC0
-DC1
-(4-15)
-(0-15)
-(0)
-(0-2,8)
-(0-6,8)
-(3-6)
BITS 0-7
BITS 8-15
BITS 2,8
BITS 0,1
BITS 3-6
CLK 4.1-01 (A2-G01/A-32)
CLK 4.1-06 (A2-A02-49)
CLK 4.1-01 (A2-G01/A-31)
CLK 4.1-01 (A2-G01/B-21)
CLK 4.1-01 (A2-G01/B-48)
CLK 4.1-01 (A2-G01/B-49)
C2N 4.2-01 DATA X (C2-K01 → G04-50)
C2N 4.1-00 (C2-E03/B-31)
C2N 4.5-31 (C2/C2-E13-14)
C2N 4.5-21 (C2/C1-E01-17)
C2N 4.5-31 (C2/C2-E09-04)
C2N 4.3-00 C2NDITION VECTOR (C2-G06 → H09)
C2N 4.3-00 (C2-H09-06)
C2N 4.2-01 DATA X BAR (C2-K01 → G15-06,32)
DMU 4.2-00 (B2-A04/A-03)
DMU 4.2-00 (B2-A08)
DMU 4.2-00 (B2-A05/A-03)
DMU 4.2-00 (B2-A05/A,A04/A-10)
DMU 4.2-00 (B2-A12/A-03)
DMU 4.2-00 (B2-A08-10)
DMU 4.2-00 (B2-A11/B-08)
DMU 4.2-00 (B2-A04/A → A11/A-35)
DMU 4.12-03 (B2/B1-D05/A-14)
DMU 4.12-03 (B2/B1-E01-05)
DMU 4.12-03 (B2/B1-D05/B-07)
DMU 4.12-02 STATUS (B2/B1-E11,E14/A,B,C)
DMU 4.12-00 DATA OUT (B2/B1-C16 → D15,B15 → A16)
DMU 4.12-01 INDEX FILE DATA SELECT (B2/B1-A03 → B03, C02 → B02)
DMU 4.12-02 COMPARE DATA (B2/B1-D16,E15)
DMU 4.4-01 SHADOW WIRED 'AND' 02
DMU 4.0-01 (B2-A10/B-51)
SHA 4.0-02 (B2-C09/A-27)
SHA 4.0-03 (B2-A07/B-01)
SHA 4.0-02 (B2-A09/A-27)
NU
NOTES:
1. DEFINITIONS OF STATUS BITS
BIT MEANING
0. ADDRESS = ADDRESS COMPARE.
1. ADDRESS > ADDRESS COMPARE.
2. DATA = DATA COMPARE.
3. DATA (UPPER) = DATA COMPARE (UPPER).
4. DATA (LOWER) = DATA COMPARE (LOWER).
5. DATA (UPPER) > DATA COMPARE (UPPER).
6. DATA (LOWER) > DATA COMPARE (LOWER).
7. OUTPUT DATA BIT 0.
8. DATA > DATA COMPARE.
2. BIT 0 IS A DUAL TRANSMITTER.
LEVEL 4 DIAGRAM
DATA MEMORY 2
IN/OUT REGISTER, STATUS AND DATA COMPARE REGISTERS
DB-B2RPU:B2
DEVELOPMENT DIVISION
60461830
A
DMU 4.2-01
IV-4-17


DMU 4.3-01 (B2-D05/B,D06/B-08)
-SHADØW
-X BAR DATA IN [-DM3XB[]
DMU 4.3-01 CRØSS BAR DATA (B2-D05/B-02)
-(4-15)
-(0-11)
INPUT ADDRESS REGISTER [A]
12DB D08/8B72
BITS 0-11
A(0-3), B(0-7)
MASTER
SLAVE
D(0-3), F(0-7)
17,18,36, 37,16,15, 11,12,44, 38,41,42
23,27,30,33,22,21, 6,4,51,49,47,45
C1,2 3,2
ENI,2 9,46
XFR 8
GØI,2 35,43
ENS 10
C(0-3) 26,28,31,34
E(0-3), G(0-7)
24,25,29, 32,19,20, 7,5,1, 52,50,48
3 00
CLK 4.1-03 (A2-H01/B-08)
-CLØCK C [-ØFFCLK(19)]
-CI2 [-SYSCLK(52)]
CLK 4.1-01 (A2-G01/B-47)
-CLØCK A [-CLK16/DM3CLA]
CØN 4.1-00 (C2-E03/B-32)
-INTERRUPT DØNE [-ITDØNE(22)]
CØN 4.5-21 (C2/C1-E17-02)
-SHADØW RØW SELECT 3 [-URS3(3)]
SHA 4.0-02 (B2-C09/B-08)
+INTERRUPT [-NINTR(18)]
CØN 4.5-31 (C2/C2-E17-08)
-MEMØRY ADRS [-MA]
DMU 4.13-00 ADRS (B2/E1-B10)
-(8-11) [-C]
DMU 4.13-01 ADRS MUX (B2/E1-D03,E04)
-INPUT ADRS TØ SHADØW [-WAND03(0-11)]
DMU 4.4-01 SHADØW WIRED 'AND' 03
-DATA MEM 3 DC FIELD(0-11) [-FID(0-8)5/DM3MIN]
CØN 4.1-00 DC FIELDS FANØUT (C2-E01/A→E05/A-24)
+C2 [-ØFFCLK(14)]
CLK 4.1-01 (A2-G01/B-01)
-LØAD DATA MEM 3 CØNTRØL RGTR [-G0U(5)/GØDM3]
CØN 4.1-00 (C2-F09-01)
-SHADØW RØW SELECT 1 [-URS1(3)]
SHA 4.0-01 (B2-C07/B-08)
DMU 4.3-01 (B2-D10/B-10)
DMU 4.3-01 (B2-D10/B-02)
DM3 CØNTRØL REGISTER
12DB D04/8B71
BITS 0-11
MASTER
SLAVE
A(0-3) 17,18, 36,37
23,27,30,33 26,28,31,34
D(0-3) C(0-3)
CI 3
ENI 9
XFR 8
GØI 35
ENS 10
E(0-3) 24,25, 29,32
B(0-7) 16,15, 11,12, 44,38, 41,42
F(0-7) 22,21,6, 4,51,49, 47,45
C2 2
EN2 46
GØ2 43
G(0-7) 19,20,7, 5,1,52, 50,48
0 00
-MICRØINSTRUCTIØN [-MI]
DMU 4.13-03 MICRØ INSTRUCTIØN RGTR (B2/E1-E03)
-DM3 MICRØINSTRUCTIØN CØNTRØL TØ SHADØW [-WAND03(0-11)]
DMU 4.4-01 SHADØW WIRED 'AND' 03
DMU 4.13-01 ADRS MUX (B2/E1-D03,E04)
DMU 4.3-01 (B2-D13/A,C14/A-35)
ADRS CØMPARE RGTR [CA]
12DB D10/8B76-A/B
BITS 0-3
2 00
-CØ [-SYSCLK(56)]
CLK 4.1-03 (A2-H01/A-22)
-SHADØW RØW SELECT 5 [-URS5(3)]
SHA 4.0-02 (B2-A03/B-08)
DMU 4.3-01 (B2-D05/B-02)
-CI3
DMU 4.3-01 (B2-D06/B-02)
-CI4
DMU 4.3-01 (B2-D05/B,D06/B-10)
+INTERRUPT
INCREMENT REGISTER
12DB D05/8B73-A/B
12DB D06/8B74-A/B
12DB C10/8B75-A/B
-INCREMENT [-I]
DMU 4.13-01 INDEX DATA (B2/E1-A01→D01)
+INCREMENT [-J]
-INCREMENT RGTR TØ SHADØW [-WAND03(0-11)]
DMU 4.4-01 SHADØW WIRED 'AND' 03
DMU 4.13-03 (B2/E1-E01-16)
[-CD2]
-(4-11)
12DB C10/8B75-B/B
BITS 4-11
1 00
-C15 [-SYSCLK(55)]
CLK 4.1-01 (A2-G01/B-05)
DMU 4.3-01 (B2-D10/B,C14/B-08)
-INTERRUPT DØNE
DMU 4.13-03 (B2/E1-E01-08)
-CE
-SHADØW RØW SELECT 6 [-URS6(3)]
SHA 4.0-03 (B2-A07/A-34)
-(0-11) [-AC]
DMU 4.13-02 CØMPARE ADRS (B2/E1-E12,E13)
-ADRS CØMPARE TØ SHADØW -(0-11)[-WAND03(0-11)]
DMU 4.3-01 (B2-D14/A-35)
NØTES:
1. BITS 8-11 ARE DUAL TRANSMITTERS.
2. EXCEPT FØR TERMS, ALL MEMØRIES ARE THE SAME.
REGISTERS | DM0 | DM1 | DM2 | DM3
CØNTRØL | C13 | D15 | A03 | D04
ADRS RGTR | C08 | D09 | A08 | D08
ADRS CØMP | C04 | C06 | A12 | D10
C05 | D07 | A11 | C10
INDEX | C12 | D12 | A04 | D05
C11 | D11 | A05 | D06
C05 | D07 | A11 | C10
INPUT | C12 | D12 | A04 | D05
C11 | D11 | A05 | D06
DATA CØMP | C04 | C06 | A12 | D10
C01 | D01 | A15 | C14
STATUS | C01 | D01 | A15 | C14
C03 | D03 | A13 | D13
C02 | D02 | A14 | D14
ØUTPUT | C03 | D03 | A13 | D13
C02 | D02 | A14 | D14
CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 4 DIAGRAM
DATA MEMØRY 3
A.I.CA. CØNTRØL REGISTER
DB-B2RPU:B2
CAGE IDENT
DWG NO 60461830
REV A
SHEET DMU 4.3-00
PAGE IV-4-19



NOTES:

1. DEFINITIONS OF STATUS BITS

BIT	MEANING
0.	ADDRESS = ADDRESS COMPARE.
1.	ADDRESS > ADDRESS COMPARE.
2.	DATA = DATA COMPARE.
3.	DATA (UPPER) = DATA COMPARE (UPPER).
4.	DATA (LOWER) = DATA COMPARE (LOWER).
5.	DATA (UPPER) > DATA COMPARE (UPPER).
6.	DATA (LOWER) > DATA COMPARE (LOWER).
7.	OUTPUT DATA BIT 0.
8.	DATA > DATA COMPARE.

2. BIT 0 IS A DUAL TRANSMITTER.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM DATA MEMORY 3 IN/OUT REGISTER, STATUS AND DATA COMPARE REGISTERS DB-B2RPU:B2	CHGE IDENT/DWG NO	60461830 REV A
DEVELOPMENT DIVISION		SHEET DMU 4.3-01	PAGE IV-4-21

CØN 4.4-01 SHADØW WIRED 'AND' 00

DMU 4.0-00 MICRØ INSTRUCTIØN CØNTRØL (B2-C13)

[-INSREG(0-11,14)] → -DMØ MICRØINSTRUCTIØN CØNTRØL TØ SHADØW [-WANDØØ(0-11)]

13 [-WANDØØ(0-11,14)]

12 -(0-11)

SHADØW WIRED 'AND' 00

a 0 ◇
a 1 ◇
a 2 ◇
a 3 ◇
a 4 ◇
a 5 ◇
a 6 ◇
a 7 ◇
a 8 ◇
a 9 ◇
a 10 ◇
a 11 ◇
a 12 ◇
a 13 ◇
a 14 ◇
a 15 ◇

SHA 4.0-01 FUNCTIØNAL UNIT CØDE → 3 -(12,13,15)

[-WANDØØ(12,13,15)/ -WANDØØ((12,13,15)]

DMU 4.0-01 STATUS RGTR (B2-CØ1/A,CØ3/A) → -DMØ STATUS RGTR TØ SHADØW [-WANDØØ(12-15)] → 4 -(12-15)

DMU 4.0-01 STATUS RGTR (B2-CØ2/A) → -DMØ STATUS RGTR TØ SHADØW [-WANDØØ(12-15)] → 4 -(12-15)

DMU 4.0-01 INPUT DATA RGTR (B2-C11/B,C12/B) → -INPUT DATA TØ SHADØW [-WANDØØ(0-15)] → 16 -(0-15)

DMU 4.0-00 INPUT ADD RGTR (B2-CØ8) → -INPUT ADDRESS TØ SHADØW [-WANDØØ(0-11)] → 12 -(0-11)

DMU 4.0-01 ØUTPUT DATA RGTR (B2-CØ2/B,CØ3/B) → -ØUTPUT DATA TØ SHADØW [-WANDØØ(0-15)] → 16 -(0-15)

DMU 4.0-00 ADDRESS CØMP (B2-CØ4/A,CØ5/B) → -ADDRESS CØMP TØ SHADØW [-WANDØØ(0-11)] → 12 -(0-11)

DMU 4.0-00 INCREMENT RGTR (B2-C12/A→CØ5/A) → -INCREMENT RGTR TØ SHADØW [-WANDØØ(0-11)] → 12 -(0-11)

DMU 4.0-01 DATA CØMP RGTR (B2-CØ1/B,CØ4/B) → -DATA CØMP TØ SHADØW [-WANDØØ(0-15)] → 16 -(0-15)

-WIRED 'AND' 00 [-W'AND'ØØ(0-15)] → 16 → SHA 4.0-00 GRØUP SELECTØR (B2-K01,02)

DATA MEMØRY 0

CØN 4.4-01 SHADØW WIRED 'AND' 01

DMU 4.1-00 MICRØ INSTRUCTIØN CØNTRØL (B2-D15)

[-INSREG(16-27,30,31)] → -DMI MICRØINSTRUCTIØN CØNTRØL TØ SHADØW [-WANDØ1(0-11)]

14 [-WANDØ1(0-11,14,15)]

12 -(0-11)

SHADØW WIRED 'AND' 01

a 0 ◇
a 1 ◇
a 2 ◇
a 3 ◇
a 4 ◇
a 5 ◇
a 6 ◇
a 7 ◇
a 8 ◇
a 9 ◇
a 10 ◇
a 11 ◇
a 12 ◇
a 13 ◇
a 14 ◇
a 15 ◇

SHA 4.1-01 FUNCTIØNAL UNIT CØDE → 2 -(12,13)

[-WANDØ1(12,13)]

DMU 4.1-01 STATUS RGTR (B2-DØ1/A→DØ2/A) → -DMI STATUS RGTR TØ SHADØW [-WANDØ1(12-15)] → 4 -(12-15)

DMU 4.1-01 STATUS RGTR (B2-DØ2/A) → -DMI STATUS RGTR TØ SHADØW [-WANDØ1(12-15)] → 4 -(12-15)

DMU 4.1-01 INPUT DATA RGTR (B2-D11/B,D12/B) → -INPUT DATA TØ SHADØW [-WANDØ1(0-15)] → 16 -(0-15)

DMU 4.1-00 INPUT ADD RGTR (B2-DØ9) → -INPUT ADDRESS TØ SHADØW [-WANDØ1(0-11)] → 12 -(0-11)

DMU 4.1-01 ØUTPUT DATA RGTR (B2-DØ2/B,DØ3/B) → -ØUTPUT DATA TØ SHADØW [-WANDØ1(0-15)] → 16 -(0-15)

DMU 4.1-00 ADDRESS CØMP (B2-CØ6/A,DØ7/A) → -ADDRESS CØMP TØ SHADØW [-WANDØ1(0-11)] → 12 -(0-11)

DMU 4.1-00 INCREMENT RGTR (B2-DØ7/A→D12/A) → -INCREMENT RGTR TØ SHADØW [-WANDØ1(0-11)] → 12 -(0-11)

DMU 4.1-01 DATA CØMP RGTR (B2-CØ6/B,DØ1/B) → -DATA CØMP TØ SHADØW [-WANDØ1(0-15)] → 16 -(0-15)

-WIRED 'AND' 01 [-W'AND'Ø1(0-15)] → 16 → SHA 4.0-00 GRØUP SELECTØR (B2-K03-04)

DATA MEMØRY 1

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
SHADØW WIRED 'AND'

CODE IDENT NO 60461830 REV A

SHEET DMU 4.4-00 PAGE IV-4-23

C2N 4.4-01 SHADØW WIRED 'AND' 02

DMU 4.2-00 MICRØ INSTRUCTIØN C2NTRØL (B2-A03)

[-INSREG(32-43,45)] → -DM2 MICRØINSTRUCTIØN C2NTRØL TØ SHADØW [-WANDO2(0-11)]

13 [-WANDO2(0-11,13)]

12 -(0-11)

SHADØW WIRED 'AND' 02

a 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

SHA 4.0-01 FUNCTIØNAL UNIT C2DE

[-WANDO2(12,14,15)/ -WANDO2(12,14,15)] → 3 -(12,14,15)

DMU 4.2-01 STATUS RGTR (B2-A13/A,A15/A)

-DM2 STATUS RGTR TØ SHADØW [-WANDO2(12-15)] → 4 -(12-15)

DMU 4.2-01 STATUS RGTR (B2-A14/A)

-DM2 STATUS RGTR TØ SHADØW [-WANDO2(12-15)] → 4 -(12-15)

16 -WIRED 'AND' 02 [-W'AND'02(0-15)] → SHA 4.0-00 GRØUP SELECTØR (B2-H12,K13)

DMU 4.2-01 INPUT DATA RGTR (B2-A04/B,A05/B)

-INPUT DATA TØ SHADØW [-WANDO2(0-15)] → 16 -(0-15)

DMU 4.2-00 INPUT ADD RGTR (B2-A08)

-INPUT ADDRESS TØ SHADØW [-WANDO2(0-11)] → 12 -(0-11)

DMU 4.2-01 ØUTPUT DATA RGTR (B2-A13/B,A14/B)

-ØUTPUT DATA TØ SHADØW [-WANDO2(0-15)] → 16 -(0-15)

DMU 4.2-00 ADDRESS C2MP (B2-A11/B,A12/A)

-ADDRESS C2MP TØ SHADØW [-WANDO2(0-11)] → 12 -(0-11)

DMU 4.2-00 INCREMENT RGTR (B2-A11/A,A04/A,A05/A)

-INCREMENT RGTR TØ SHADØW [-WANDO2(0-11)] → 12 -(0-11)

DMU 4.2-01 DATA C2MP RGTR (B2-A12/B,A15/B)

-DATA C2MPARE TØ SHADØW [-WANDO2(0-15)] → 16 -(0-15)

DATA MEMØRY 2

C2N 4.4-01 SHADØW WIRED 'AND' 01

DMU 4.3-00 MICRØ INSTRUCTIØN C2NTRØL (B2-D04)

[-INSREG(48-59,61,63)] → -DM3 MICRØINSTRUCTIØN C2NTRØL TØ SHADØW [-WANDO3(0-11)]

14 [-WANDO3(0-11,13,15)]

12 -(0-11)

SHADØW WIRED 'AND' 03

a 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

SHA 4.0-01 FUNCTIØNAL UNIT C2DE

[-WANDO3(12,14)/ -WANDO3(12,14)] → 2 -(12,14)

DMU 4.3-01 STATUS RGTR (B2-D13/A,C14/A)

-DM3 STATUS RGTR TØ SHADØW [-WANDO3(12-15)] → 4 -(12-15)

DMU 4.3-01 STATUS RGTR (B2-D14/A)

-DM3 STATUS RGTR TØ SHADØW [-WANDO3(12-15)] → 4 -(12-15)

16 -WIRED 'AND' 03 [-W'AND'03(0-15)] → SHA 4.0-00 GRØUP SELECTØR (B2-K14,K15)

DMU 4.3-01 INPUT DATA RGTR (B2-D05/B,D06/B)

-INPUT DATA TØ SHADØW [-WANDO3(0-15)] → 16 -(0-15)

DMU 4.3-00 INPUT ADD RGTR (B2-D08)

-INPUT ADDRESS TØ SHADØW [-WANDO3(0-11)] → 12 -(0-11)

DMU 4.3-01 ØUTPUT DATA RGTR (B2-D13/B,D14/B)

-ØUTPUT DATA TØ SHADØW [-WANDO3(0-15)] → 16 -(0-15)

DMU 4.3-00 ADDRESS C2MP (B2-D10/A,C10/A)

-ADDRESS C2MP TØ SHADØW [-WANDO3(0-11)] → 12 -(0-11)

DMU 4.3-00 INCREMENT RGTR (B2-C10/A,D05/A,D06/A)

-INCREMENT RGTR TØ SHADØW [-WANDO3(0-11)] → 12 -(0-11)

DMU 4.3-01 DATA C2MP RGTR (B2-D10/B,C14/B)

-DATA C2MPARE TØ SHADØW [-WANDO3(0-15)] → 16 -(0-15)

DATA MEMØRY 3

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM SHADØW WIRED 'AND'	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN		SHEET DMU 4.4-01	PAGE IV-4-25

NØTES:

1. ADDRESS LINES FØR D11 → D14, C11 → C14, B11 → B14 ARE CØNNECTED IN THE SAME ØRDER AS FØR A11 → A14.
2. 12171

A = 3,23,15 B = 4,24,16 C = 5,1,17 D = 6,2,18	T = 7,11,14 F = 8,12,13

3. ØUTPUT REGISTER

BIT	-Z AUX	-Z LSI
0	11-4	B2-B04-30
1	11-8	B2-B04-34
2	11-15	B2-B04-41
3	12-26	B2-B03-52
4	12-25	B2-B03-51
5	12-20	B2-B03-46
6	12-3	B2-B03-29
7	12-1	B2-B03-27
8	11-16	B2-B04-42
9	11-10	B2-B04-36
10	13-1	B2-B02-27
11	11-1	B2-B04-27
12	11-3	B2-B04-29
13	11-6	B2-B04-32
14	13-16	B2-B02-42
15	13-15	B2-B02-41

4.

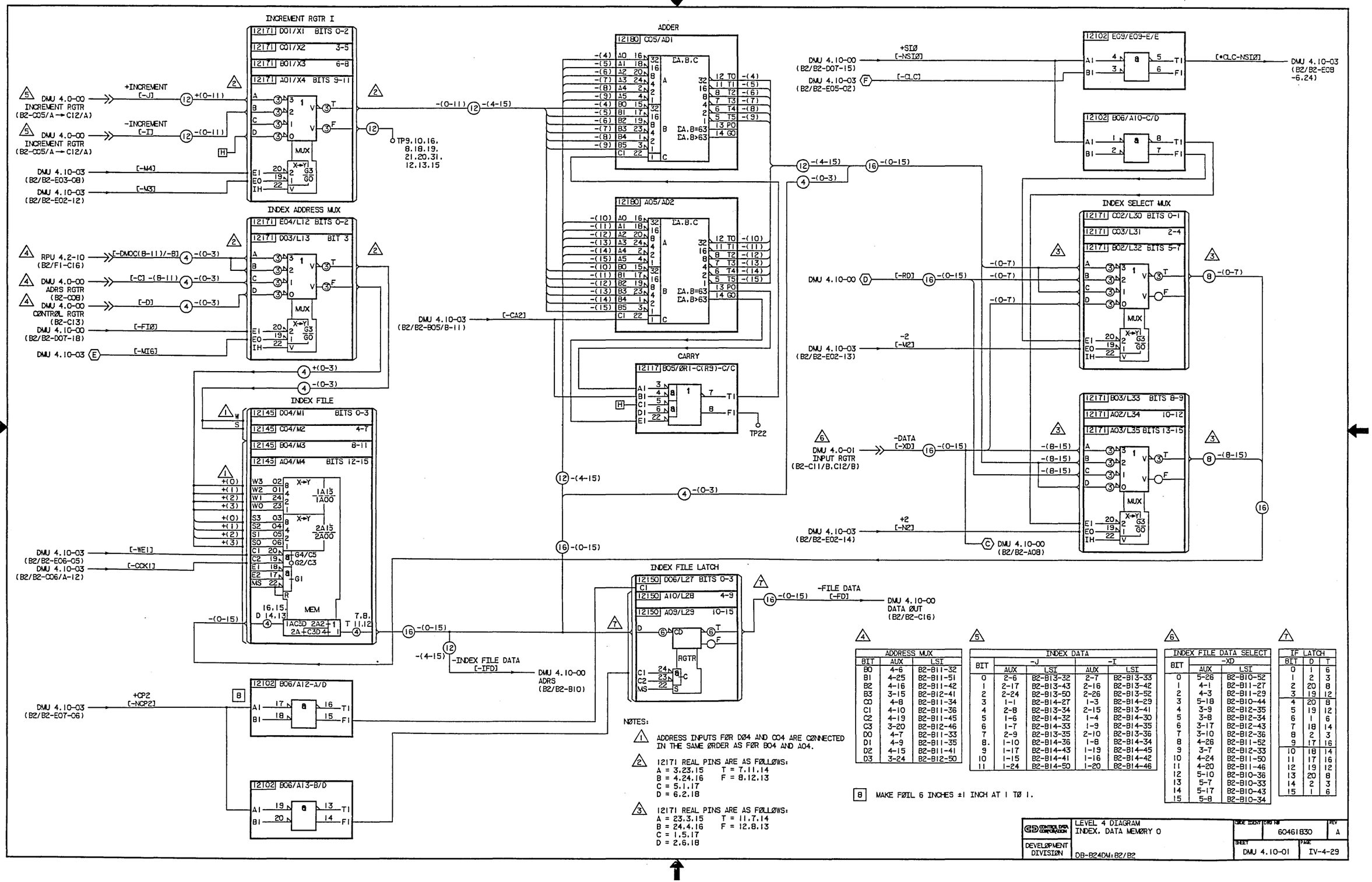
BIT	D	T
0,6,12	1	6
1,7,13	2	3
2,8	17	16
3,9,14	18	14
4,11,15	19	12
5,10	20	8

5. MAKE THESE NETS AS SHØRT AS PØSSIBLE.
6. CØNNECTED AFTER D11 → D14.

4.

BIT	-MA AUX	-MA LSI	-RD AUX	-RD LSI
0	7-9	B2-B08-35	6-6	B2-B09-32
1	7-8	B2-B08-34	6-8	B2-B09-34
2	7-10	B2-B08-36	6-7	B2-B09-33
3	7-4	B2-B08-30	6-1	B2-B09-27
4	7-7	B2-B08-33	7-26	B2-B08-52
5	7-15	B2-B08-41	6-3	B2-B09-29
6	7-17	B2-B08-43	6-10	B2-B09-36
7	7-6	B2-B08-32	6-9	B2-B09-35
8	7-3	B2-B08-29	7-25	B2-B08-51
9	7-16	B2-B08-42	7-24	B2-B08-50
10	7-19	B2-B08-45	6-16	B2-B09-42
11	7-1	B2-B08-27	6-20	B2-B09-46
12			7-21	B2-B08-47
13			7-20	B2-B08-46
14			6-24	B2-B09-50
15			6-15	B2-B09-41

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM DATA MEMØRY 0	CDC ITEM/DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-B24DM:B2/B2	SHEET DMU 4.10-00 PAGE IV-4-27



NØTES:

1. ADDRESS INPUTS FØR D04 AND C04 ARE CØNNECTED IN THE SAME ØRDER AS FØR B04 AND A04.
2. 12171 REAL PINS ARE AS FØLLØWS:
   A = 3,23,15 T = 7,11,14
   B = 4,24,16 F = 8,12,13
   C = 5,1,17
   D = 6,2,18
3. 12171 REAL PINS ARE AS FØLLØWS:
   A = 23,3,15 T = 11,7,14
   B = 24,4,16 F = 12,8,13
   C = 1,5,17
   D = 2,6,18

4

ADDRESS MUX		
BIT	AUX	LSI
B0	4-6	B2-B11-32
B1	4-25	B2-B11-51
B2	4-16	B2-B11-42
B3	3-15	B2-B12-41
C0	4-8	B2-B11-34
C1	4-10	B2-B11-36
C2	4-19	B2-B11-45
C3	3-20	B2-B12-46
D0	4-7	B2-B11-33
D1	4-9	B2-B11-35
D2	4-15	B2-B11-41
D3	3-24	B2-B12-50

5

INDEX DATA				
BIT	-J		-I	
	AUX	LSI	AUX	LSI
0	2-6	B2-B13-32	2-7	B2-B13-33
1	2-17	B2-B13-43	2-16	B2-B13-42
2	2-24	B2-B13-50	2-26	B2-B13-52
3	1-1	B2-B14-27	1-3	B2-B14-29
4	2-8	B2-B13-34	2-15	B2-B13-41
5	1-6	B2-B14-32	1-4	B2-B14-30
6	1-7	B2-B14-33	1-9	B2-B14-35
7	2-9	B2-B13-35	2-10	B2-B13-36
8.	1-10	B2-B14-36	1-8	B2-B14-34
9	1-17	B2-B14-43	1-19	B2-B14-45
10	1-15	B2-B14-41	1-16	B2-B14-42
11	1-24	B2-B14-50	1-20	B2-B14-46

6

INDEX FILE DATA SELECT		
BIT	-XD	
	AUX	LSI
0	5-26	B2-B10-52
1	4-1	B2-B11-27
2	4-3	B2-B11-29
3	5-18	B2-B10-44
4	3-9	B2-B12-35
5	3-8	B2-B12-34
6	3-17	B2-B12-43
7	3-10	B2-B12-36
8	4-26	B2-B11-52
9	3-7	B2-B12-33
10	4-24	B2-B11-50
11	4-20	B2-B11-46
12	5-10	B2-B10-36
13	5-7	B2-B10-33
14	5-17	B2-B10-43
15	5-8	B2-B10-34

7

IF LATCH		
BIT	D	T
0	1	6
1	2	3
2	20	8
3	19	12
4	20	8
5	19	12
6	1	6
7	18	14
8	2	3
9	17	16
10	18	14
11	17	16
12	19	12
13	20	8
14	2	3
15	1	6

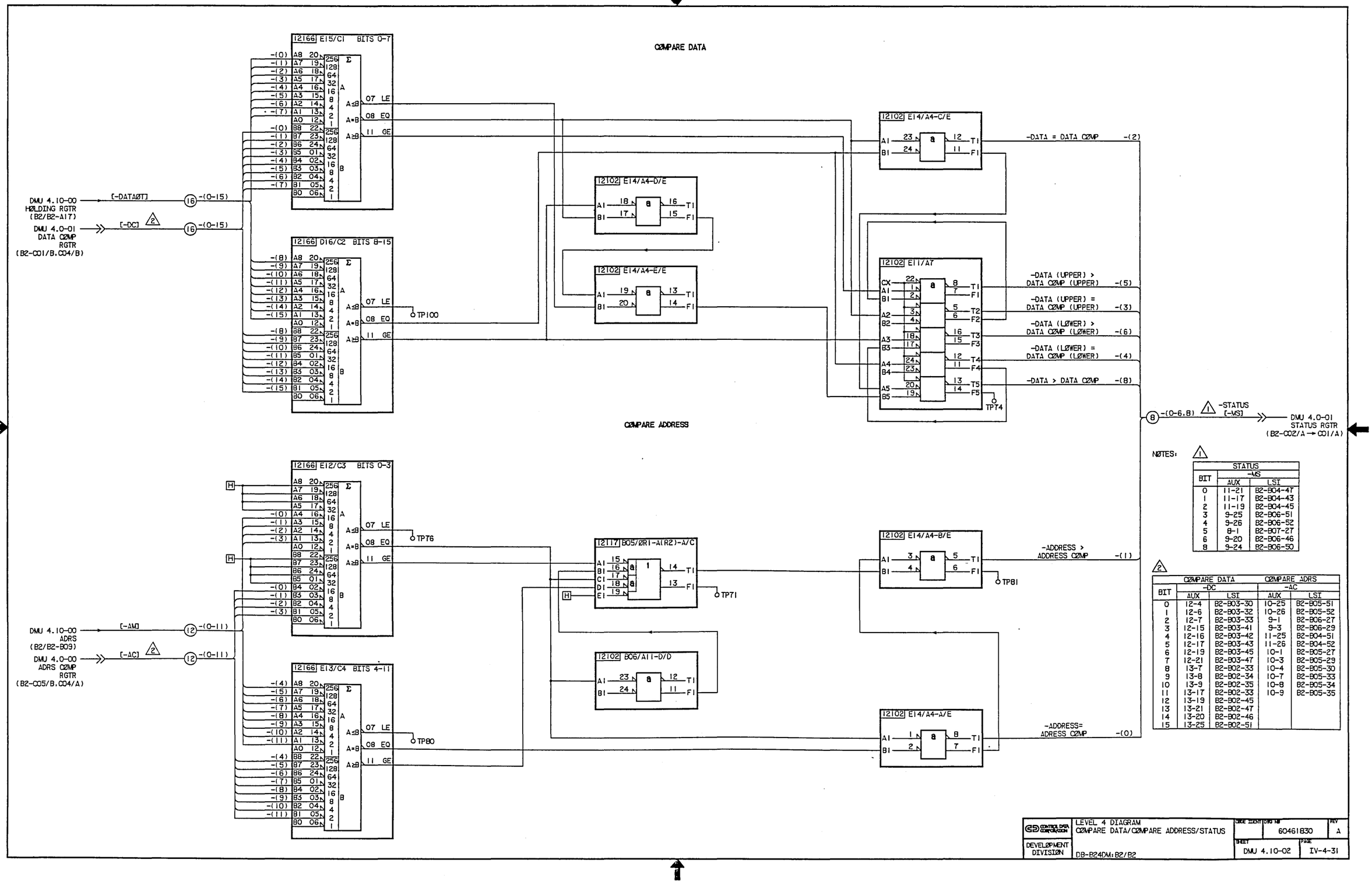
8 MAKE FØIL 6 INCHES ±1 INCH AT 1 TØ 1.

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
INDEX, DATA MEMØRY 0

DB-B24DM:B2/B2

CODE IDENT | DRG NO: 60461830 | REV: A
SHEET: DMU 4.10-01 | PAGE: IV-4-29



NØTES:

1

BIT	STATUS -MS AUX	STATUS -MS LSI
0	11-21	B2-B04-47
1	11-17	B2-B04-43
2	11-19	B2-B04-45
3	9-25	B2-B06-51
4	9-26	B2-B06-52
5	8-1	B2-B07-27
6	9-20	B2-B06-46
8	9-24	B2-B06-50

2

BIT	COMPARE DATA -DC AUX	COMPARE DATA -DC LSI	COMPARE ADRS -AC AUX	COMPARE ADRS -AC LSI
0	12-4	B2-B03-30	10-25	B2-B05-51
1	12-6	B2-B03-32	10-26	B2-B05-52
2	12-7	B2-B03-33	9-1	B2-B06-27
3	12-15	B2-B03-41	9-3	B2-B06-29
4	12-16	B2-B03-42	11-25	B2-B04-51
5	12-17	B2-B03-43	11-26	B2-B04-52
6	12-19	B2-B03-45	10-1	B2-B05-27
7	12-21	B2-B03-47	10-3	B2-B05-29
8	13-7	B2-B02-33	10-4	B2-B05-30
9	13-8	B2-B02-34	10-7	B2-B05-33
10	13-9	B2-B02-35	10-8	B2-B05-34
11	13-17	B2-B02-33	10-9	B2-B05-35
12	13-19	B2-B02-45		
13	13-21	B2-B02-47		
14	13-20	B2-B02-46		
15	13-25	B2-B02-51		

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
COMPARE DATA/COMPARE ADDRESS/STATUS

DB-B24DM:B2/B2

CODE IDENT | DRG NO | REV
60461830 | A

SHEET: DMU 4.10-02
PAGE: IV-4-31

MICRØ INST RGTR				
BIT	-MI		-RI	
	AUX	LSI	AUX	LSI
0	2-1	B2-B13-27	2-3	B2-B13-29
1	2-4	B2-B13-30	3-26	B2-B12-52
2	2-25	B2-B13-51	2-20	B2-B13-46
3	2-19	B2-B13-45	2-21	B2-B13-47
4	3-1	B2-B12-27	3-6	B2-B12-32
5	3-3	B2-B12-29	3-4	B2-B12-30
6	3-25	B2-B12-51	3-16	B2-B12-42
7	3-21	B2-B12-47	3-19	B2-B12-45

NØTES:

1. MAKE NETS SHØRT AS PØSSIBLE.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM MICRØINSTRUCTIØN FANØUT/CLØCKS.	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-B24DM:B2/B2	SHEET DMU 4.10-03	PAGE IV-4-33

NOTES:

1. ADDRESS LINES FØR D11 → D14. C11 → C14, B11 → B14 ARE CØNNECTED IN THE SAME ØRDER AS FØR A11 → A14.

2.

12171	
A = 3.23.15	T = 7.11.14
B = 4.24.16	F = 8.12.13
C = 5.1.17	
D = 6.2.18	

3.

ØUTPUT REGISTER		
BIT	-Z	
	MUX	LSI
0	11-4	B2-E04-30
1	11-8	B2-E04-34
2	11-15	B2-E04-41
3	12-26	B2-E03-52
4	12-25	B2-E03-51
5	12-20	B2-E03-46
6	12-3	B2-E03-29
7	12-1	B2-E03-27
8	11-16	B2-E04-42
9	11-10	B2-E04-36
10	13-1	B2-E02-27
11	11-1	B2-E04-27
12	11-3	B2-E04-29
13	11-6	B2-E04-32
14	13-16	B2-E02-42
15	13-15	B2-E02-41

4.

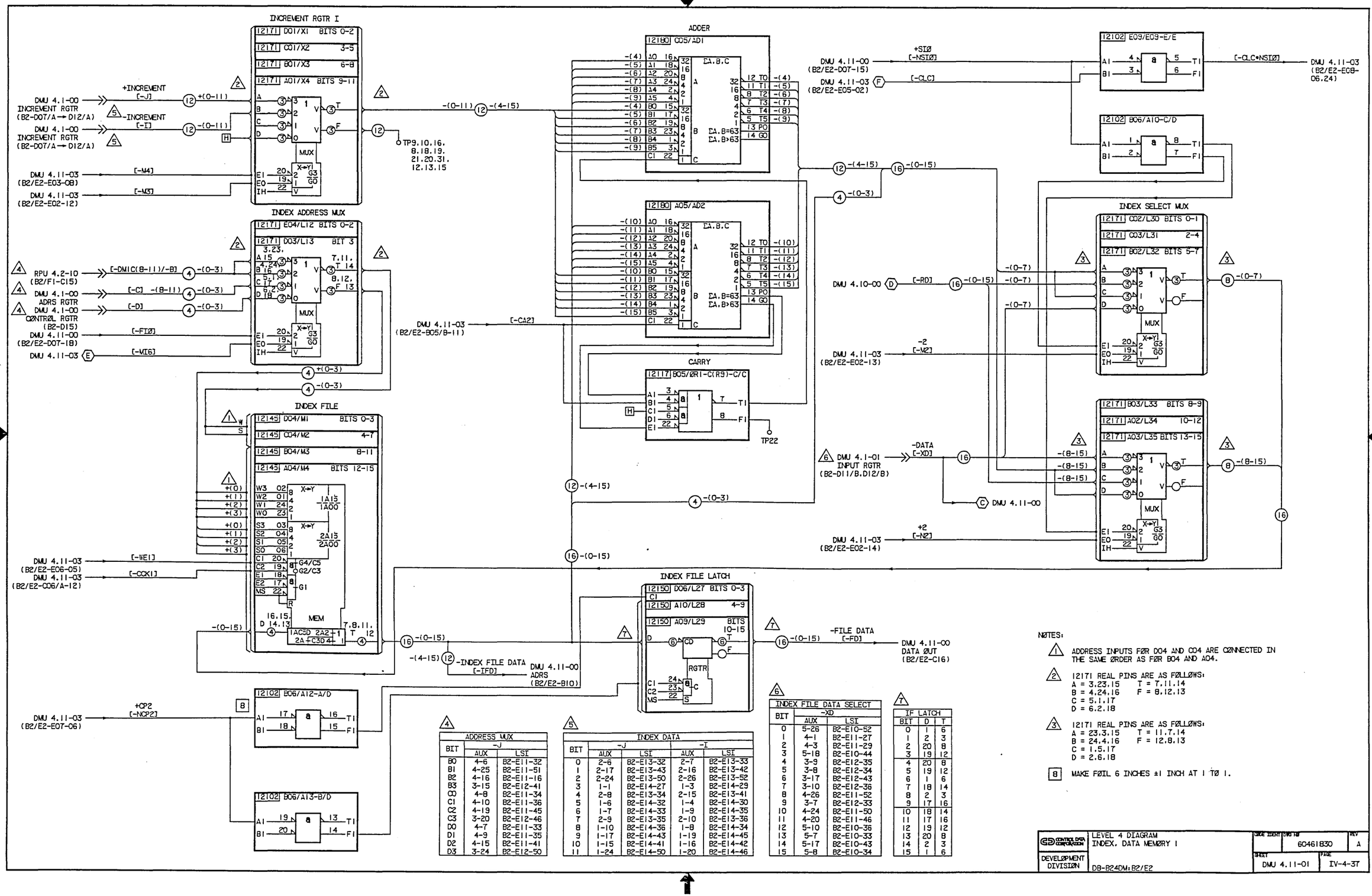
BIT	D	T
0.6.12	1	6
1.7.13	2	3
2.8	17	16
3.9.14	18	14
4.11.15	19	12
5.10	20	8

4 MAKE THESE NETS AS SHØRT AS PØSSIBLE.

5 CØNNECTED AFTER D11 → D14.

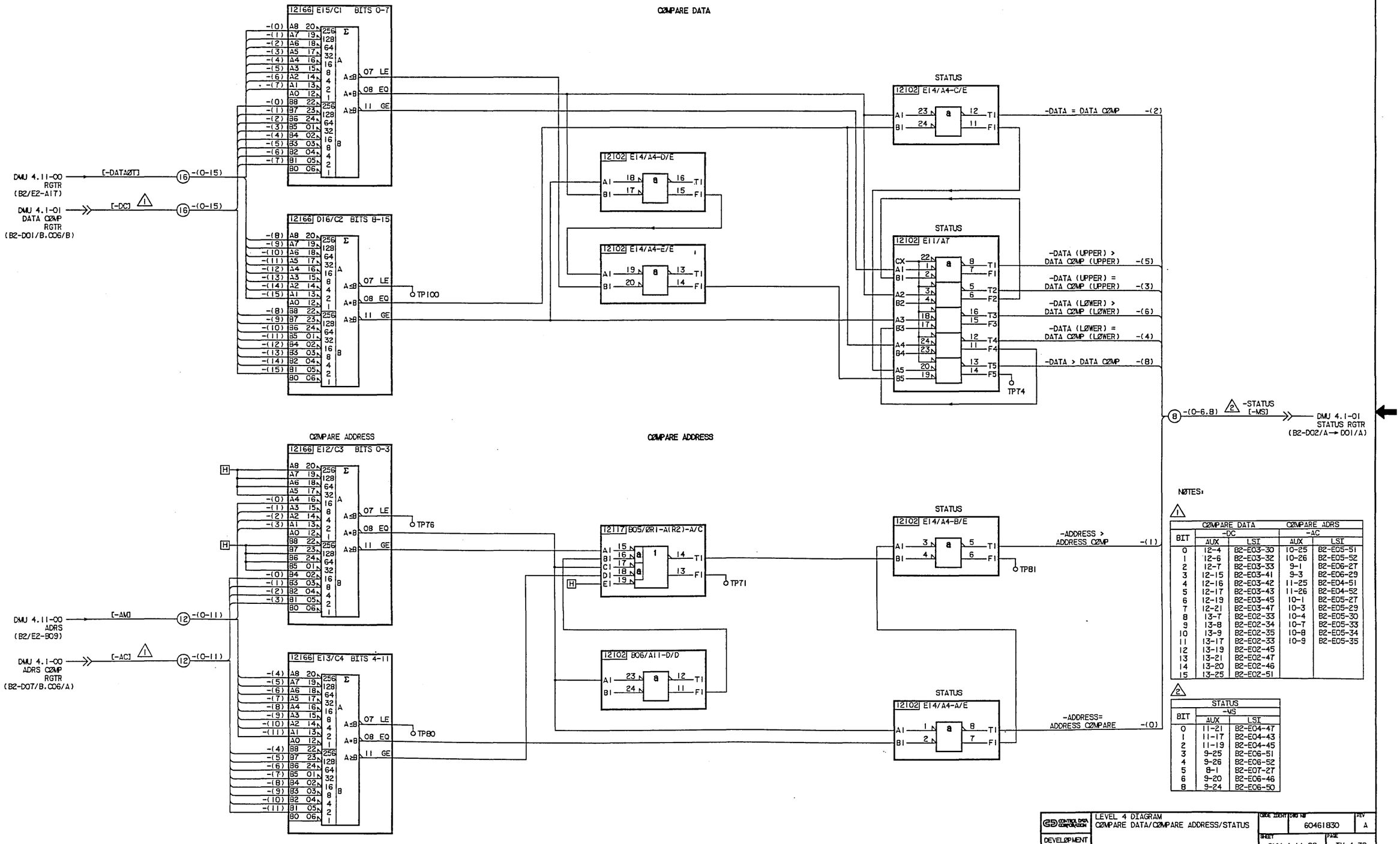
INPUT REGISTER				
BIT	-MA		-RD	
	AUX	LSI	AUX	LSI
0	7-9	B2-E08-35	6-6	B2-E09-32
1	7-8	B2-E08-34	6-8	B2-E09-34
2	7-10	B2-E08-36	6-7	B2-E09-33
3	7-4	B2-E08-30	6-1	B2-E09-27
4	7-7	B2-E08-33	7-26	B2-E08-52
5	7-15	B2-E08-41	6-3	B2-E09-29
6	7-17	B2-E08-43	6-10	B2-E09-36
7	7-6	B2-E08-32	6-9	B2-E09-35
8	7-3	B2-E08-29	7-25	B2-E08-51
9	7-16	B2-E08-42	7-24	B2-E08-50
10	7-19	B2-E08-45	6-16	B2-E09-42
11	7-1	B2-E08-27	6-20	B2-E09-48
12			7-21	B2-E08-47
13			7-20	B2-E08-46
14			6-24	B2-E09-50
15			6-15	B2-E09-41

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM DATA MEMØRY 1	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISION	DB-B240M1B2/B2	SHEET DMU 4.11-00	PAGE IV-4-35


INCREMENT RGTR I
12171 D01/X1 BITS 0-2
12171 C01/X2 3-5
12171 B01/X3 6-8
12171 A01/X4 BITS 9-11
+INCREMENT [-J]
-INCREMENT [-I]
DMU 4.1-00 INCREMENT RGTR (B2-D07/A→D12/A)
DMU 4.1-00 INCREMENT RGTR (B2-D07/A→D12/A)
[-M4]
[-M5]
DMU 4.11-03 (B2/E2-E03-08)
DMU 4.11-03 (B2/E2-E02-12)
MUX
INDEX ADDRESS MUX
12171 E04/L12 BITS 0-2
12171 D03/L13 BIT 3
RPU 4.2-10 (B2/F1-C15)
DMU 4.1-00 ADRS RGTR
DMU 4.1-00 CØNTRØL RGTR (B2-D15)
DMU 4.11-00 (B2/E2-D07-18)
DMU 4.11-03
[-DMIC(8-11)/-B]
[-C] -(8-11)
[-D]
[-FIØ]
[-MI6]
INDEX FILE
12145 D04/M1 BITS 0-3
12145 C04/M2 4-7
12145 B04/M3 8-11
12143 A04/M4 BITS 12-15
MEM
DMU 4.11-03 (B2/E2-E06-05)
DMU 4.11-03 (B2/E2-C06/A-12)
[-WEI]
[-CCKI]
TP9.10.16. 8.18.19. 21.20.31. 12.13.15
ADDER
12180 C05/AD1
12180 A05/AD2
ΣA.B
ΣA.B=63
ΣA.B>63
DMU 4.11-03 (B2/E2-B05/B-11)
[-CA2]
CARRY
12117 B05/ØR1-C(R9)-C/C
TP22
INDEX FILE LATCH
12150 D06/L27 BITS 0-3
12150 A10/L28 4-9
12150 A09/L29 BITS 10-15
RGTR
-INDEX FILE DATA [-IFD]
DMU 4.11-00 ADRS (B2/E2-B10)
-FILE DATA [-FD]
DMU 4.11-00 DATA ØUT (B2/E2-C16)
DMU 4.11-00 (B2/E2-D07-15)
DMU 4.11-03 (B2/E2-E05-02)
+SIØ [-NSIØ]
[-CLC]
12102 E09/E09-E/E
[-CLC+NSIØ]
DMU 4.11-03 (B2/E2-EC8-06.24)
12102 B06/A10-C/D
DMU 4.10-00
[-RD]
INDEX SELECT MUX
12171 C02/L30 BITS 0-1
12171 C03/L31 2-4
12171 B02/L32 BITS 5-7
12171 B03/L33 BITS 8-9
12171 A02/L34 10-12
12171 A03/L35 BITS 13-15
DMU 4.11-03 (B2/E2-E02-13)
[-M2]
DMU 4.11-03 (B2/E2-E02-14)
[-N2]
DMU 4.11-00
DMU 4.1-01 INPUT RGTR (B2-D11/B.D12/B)
[-XD]
12102 B06/A12-A/D
12102 B06/A13-B/D
DMU 4.11-03 (B2/E2-E07-06)
[-NCP2]
+CP2
NØTES:
1 ADDRESS INPUTS FØR D04 AND C04 ARE CØNNECTED IN THE SAME ØRDER AS FØR B04 AND A04.
2 12171 REAL PINS ARE AS FØLLØWS: A = 3.23.15 T = 7.11.14 B = 4.24.16 F = 8.12.13 C = 5.1.17 D = 6.2.18
3 12171 REAL PINS ARE AS FØLLØWS: A = 23.3.15 T = 11.7.14 B = 24.4.16 F = 12.8.13 C = 1.5.17 D = 2.6.18
8 MAKE FØIL 6 INCHES ±1 INCH AT 1 TØ 1.
4 ADDRESS MUX
BIT | -J AUX | -J LSI
BØ 4-6 B2-E11-32
B1 4-25 B2-E11-51
B2 4-16 B2-E11-16
B3 3-15 B2-E12-41
C0 4-8 B2-E11-34
C1 4-10 B2-E11-36
C2 4-19 B2-E11-45
C3 3-20 B2-E12-46
D0 4-7 B2-E11-33
D1 4-9 B2-E11-35
D2 4-15 B2-E11-41
D3 3-24 B2-E12-50
5 INDEX DATA
BIT | -J AUX | -J LSI | -I AUX | -I LSI
0 2-6 B2-E13-32 2-7 B2-E13-33
1 2-17 B2-E13-43 2-16 B2-E13-42
2 2-24 B2-E13-50 2-26 B2-E13-52
3 1-1 B2-E14-27 1-3 B2-E14-29
4 2-8 B2-E13-34 2-15 B2-E13-41
5 1-6 B2-E14-32 1-4 B2-E14-30
6 1-7 B2-E14-33 1-9 B2-E14-35
7 2-9 B2-E13-35 2-10 B2-E13-36
8 1-10 B2-E14-36 1-8 B2-E14-34
9 1-17 B2-E14-43 1-19 B2-E14-45
10 1-15 B2-E14-41 1-16 B2-E14-42
11 1-24 B2-E14-50 1-20 B2-E14-46
6 INDEX FILE DATA SELECT
BIT | -XD AUX | -XD LSI
0 5-26 B2-E10-52
1 4-1 B2-E11-27
2 4-3 B2-E11-29
3 5-18 B2-E10-44
4 3-9 B2-E12-35
5 3-8 B2-E12-34
6 3-17 B2-E12-43
7 3-10 B2-E12-36
8 4-26 B2-E11-52
9 3-7 B2-E12-33
10 4-24 B2-E11-50
11 4-20 B2-E11-46
12 5-10 B2-E10-36
13 5-7 B2-E10-33
14 5-17 B2-E10-43
15 5-8 B2-E10-34
7 IF LATCH
BIT | D | T
0 1 6
1 2 3
2 20 8
3 19 12
4 20 8
5 19 12
6 1 6
7 18 14
8 2 3
9 17 16
10 18 14
11 17 16
12 19 12
13 20 8
14 2 3
15 1 6
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
INDEX, DATA MEMØRY 1
DB-B24DM:B2/E2
CODE IDENT
DWG NO 60461830
REV A
SHEET DMU 4.11-01
PAGE IV-4-37

COMPARE DATA

COMPARE ADDRESS



NOTES:

1

BIT	COMPARE DATA -DC AUX	COMPARE DATA -DC LSI	COMPARE ADRS -AC AUX	COMPARE ADRS -AC LSI
0	12-4	B2-E03-30	10-25	B2-E05-51
1	12-6	B2-E03-32	10-26	B2-E05-52
2	12-7	B2-E03-33	9-1	B2-E06-27
3	12-15	B2-E03-41	9-3	B2-E06-29
4	12-16	B2-E03-42	11-25	B2-E04-51
5	12-17	B2-E03-43	11-26	B2-E04-52
6	12-19	B2-E03-45	10-1	B2-E05-27
7	12-21	B2-E03-47	10-3	B2-E05-29
8	13-7	B2-E02-33	10-4	B2-E05-30
9	13-8	B2-E02-34	10-7	B2-E05-33
10	13-9	B2-E02-35	10-8	B2-E05-34
11	13-17	B2-E02-33	10-9	B2-E05-35
12	13-19	B2-E02-45		
13	13-21	B2-E02-47		
14	13-20	B2-E02-46		
15	13-25	B2-E02-51		

2

BIT	STATUS -MS AUX	STATUS -MS LSI
0	11-21	B2-E04-47
1	11-17	B2-E04-43
2	11-19	B2-E04-45
3	9-25	B2-E06-51
4	9-26	B2-E06-52
5	8-1	B2-E07-27
6	9-20	B2-E06-46
8	9-24	B2-E06-50

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
COMPARE DATA/COMPARE ADDRESS/STATUS

DB-B24DM:B2/E2

CODE IDENT 60461830 REV A

SHEET DMU 4.11-02 PAGE IV-4-39

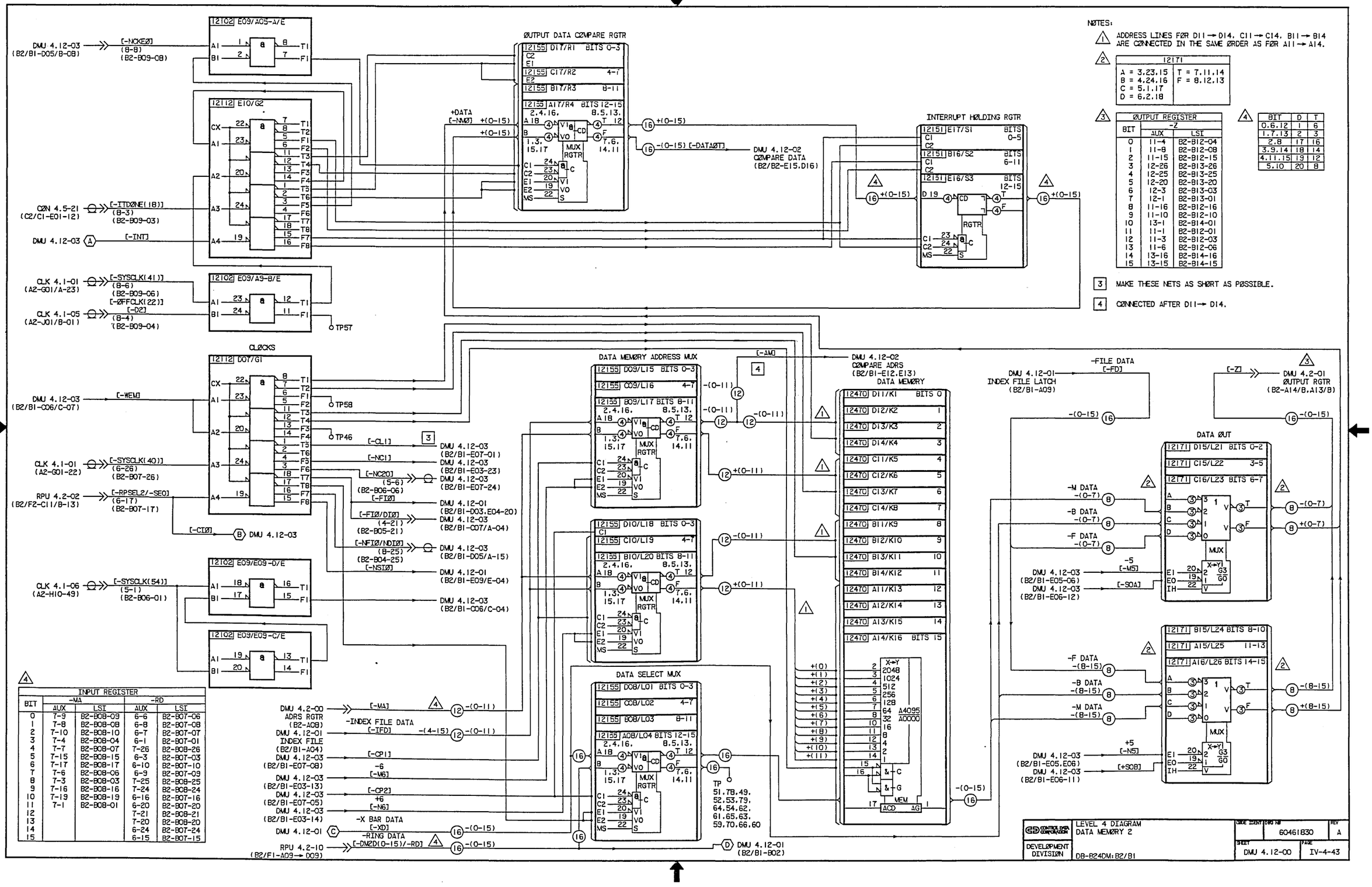
AS FØR A11 A14.

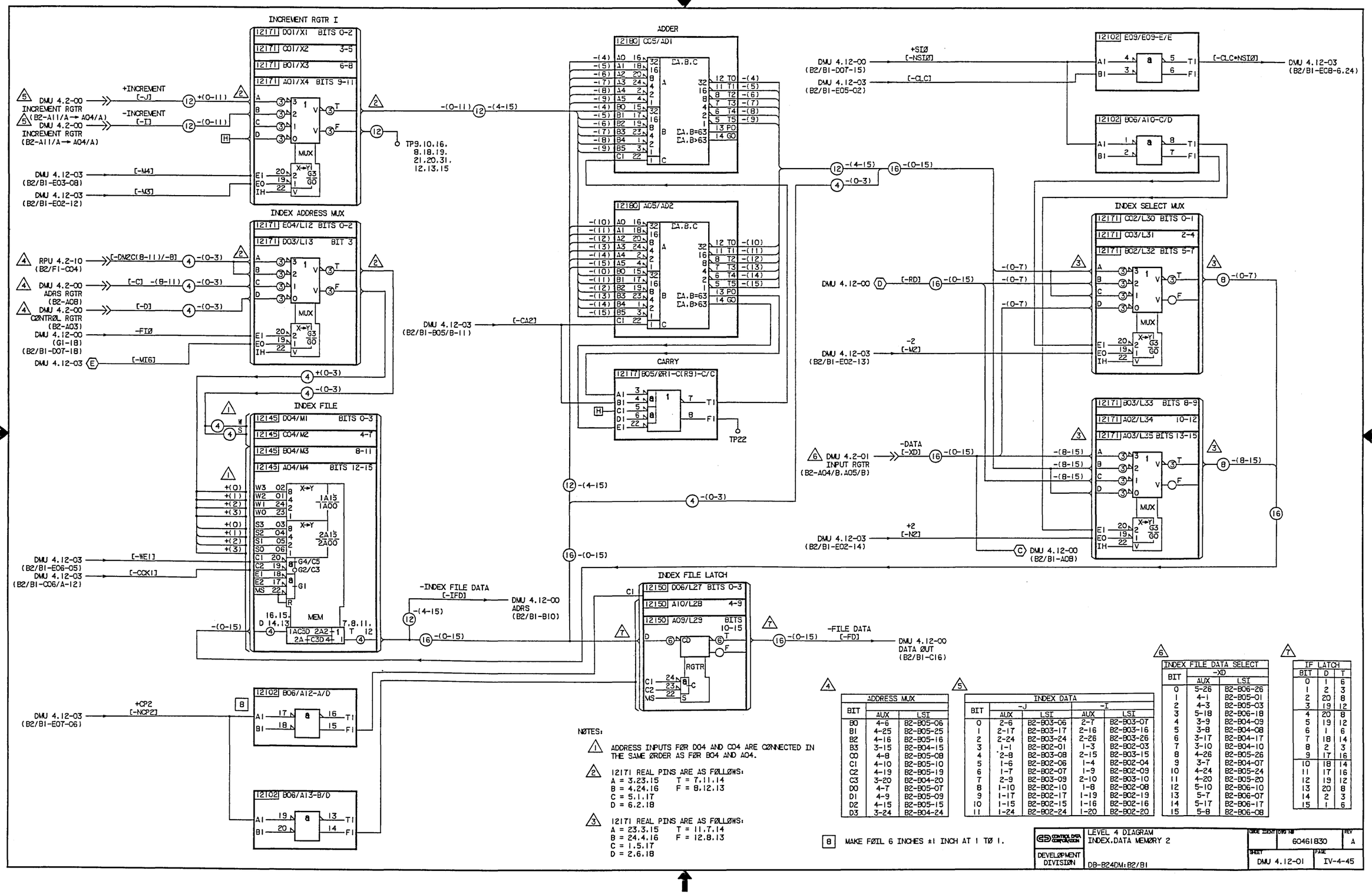
MICRØ INST RGTR				
BIT	-WI		-RI	
	AUX	LSI	AUX	LSI
0	2-1	B2-E13-27	2-3	B2-E13-29
1	2-4	B2-E13-30	3-26	B2-E12-52
2	2-25	B2-E13-51	2-20	B2-E13-46
3	2-19	B2-E13-45	2-21	B2-E13-47
4	3-1	B2-E12-27	3-6	B2-E12-32
5	3-3	B2-E12-29	3-4	B2-E12-30
6	3-25	B2-E12-51	3-16	B2-E12-42
7	3-21	B2-E12-47	3-19	B2-E12-45

NØTES:

1. MAKE NETS SHØRT AS PØSSIBLE.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM MICRØINSTRUCTIØN FANØUT/CLØCKS.	DRAWING NO 60461830	REV A
DEVELØPMENT DIVISIØN	DB-B24DM-B2/E2	SHEET DMU 4.11-03	PAGE IV-4-41


NOTES:
1 ADDRESS LINES FØR D11→D14, C11→C14, B11→B14 ARE CONNECTED IN THE SAME ØRDER AS FØR A11→A14.
2
12171
A = 3.23.15
B = 4.24.16
C = 5.1.17
D = 6.2.18
T = 7.11.14
F = 8.12.13
3
ØUTPUT REGISTER
BIT
-Z
AUX
LSI
0 11-4 B2-B12-04
1 11-8 B2-B12-08
2 11-15 B2-B12-15
3 12-26 B2-B13-26
4 12-25 B2-B13-25
5 12-20 B2-B13-20
6 12-3 B2-B13-03
7 12-1 B2-B13-01
8 11-16 B2-B12-16
9 11-10 B2-B12-10
10 13-1 B2-B14-01
11 11-1 B2-B12-01
12 11-3 B2-B12-03
13 11-6 B2-B12-06
14 13-16 B2-B14-16
15 13-15 B2-B14-15
4
BIT D T
0.6.12 1 6
1.7.13 2 3
2.8 17 16
3.9.14 18 14
4.11.15 19 12
5.10 20 8
3 MAKE THESE NETS AS SHØRT AS PØSSIBLE.
4 CØNNECTED AFTER D11→D14.
ØUTPUT DATA CØMPARE RGTR
INTERRUPT HØLDING RGTR
DMU 4.12-03 (B2/B1-D05/B-08)
[-NCKEØ] (8-8) (B2-B09-08)
CØN 4.5-21 (C2/C1-E01-12)
[-ITDØNE(18)] (8-3) (B2-B09-03)
DMU 4.12-03
[-INT]
CLK 4.1-01 (A2-G01/A-23)
[-SYSCLK(41)] (8-6) (B2-B09-06)
[-ØFFCLK(22)]
CLK 4.1-05 (A2-J01/B-01)
[-D2] (8-4) (B2-B09-04)
TP57
+DATA [-NMØ]
+(0-15)
-(0-15) [-DATAØT]
DMU 4.12-02 CØMPARE DATA (B2/B2-E15,D16)
CLØCKS
DMU 4.12-03 (B2/B1-C06/C-07)
[-WEM]
TP58
TP46
[-CL1]
DMU 4.12-03 (B2/B1-E07-01)
[-NC1]
DMU 4.12-03 (B2/B1-E03-23)
[-NC2Ø] (5-6) (B2-B06-06)
DMU 4.12-03 (B2/B1-E07-24)
CLK 4.1-01 (A2-G01-22)
[-SYSCLK(40)] (6-26) (B2-B07-26)
[-FIØ]
DMU 4.12-01 (B2/B1-D03,E04-20)
RPU 4.2-02 (B2/F2-C11/B-13)
[-RPSEL2/-SE0] (6-17) (B2-B07-17)
[-FIØ/DIØ] (4-21) (B2-B05-21)
DMU 4.12-03 (B2/B1-C07/A-04)
[-CIØ]
[-NFIØ/NDIØ] (B-25) (B2-B04-25)
DMU 4.12-03 (B2/B1-D05/A-15)
[-NSIØ]
DMU 4.12-01 (B2/B1-E09/E-04)
CLK 4.1-06 (A2-H10-49)
[-SYSCLK(54)] (5-1) (B2-B06-01)
DMU 4.12-03 (B2/B1-C06/C-04)
DATA MEMØRY ADDRESS MUX
DATA SELECT MUX
[-AMØ]
DMU 4.12-02 CØMPARE ADRS (B2/B1-E12,E13) DATA MEMØRY
-FILE DATA [-FD]
DMU 4.12-01 INDEX FILE LATCH (B2/B1-A09)
[-Z]
DMU 4.2-01 ØUTPUT RGTR (B2-A14/B,A13/B)
DATA ØUT
-M DATA -(0-7)
-B DATA -(0-7)
-F DATA -(0-7)
-5 [-M5]
DMU 4.12-03 (B2/B1-E05-06)
DMU 4.12-03 (B2/B1-E06-12)
[-SOA]
+(0-7)
-F DATA -(8-15)
-B DATA -(8-15)
-M DATA -(8-15)
+5 [-N5]
DMU 4.12-03 (B2/B1-E05,E06)
DMU 4.12-03 (B2/B1-E06-11)
[+SOB]
-(8-15)
+(8-15)
4
INPUT REGISTER
BIT
-MA AUX
-MA LSI
-RD AUX
-RD LSI
0 7-9 B2-B08-09 6-6 B2-B07-06
1 7-8 B2-B08-08 6-8 B2-B07-08
2 7-10 B2-B08-10 6-7 B2-B07-07
3 7-4 B2-B08-04 6-1 B2-B07-01
4 7-7 B2-B08-07 7-26 B2-B08-26
5 7-15 B2-B08-15 6-3 B2-B07-03
6 7-17 B2-B08-17 6-10 B2-B07-10
7 7-6 B2-B08-06 6-9 B2-B07-09
8 7-3 B2-B08-03 7-25 B2-B08-25
9 7-16 B2-B08-16 7-24 B2-B08-24
10 7-19 B2-B08-19 6-16 B2-B07-16
11 7-1 B2-B08-01 6-20 B2-B07-20
12 7-21 B2-B08-21
13 7-20 B2-B08-20
14 6-24 B2-B07-24
15 6-15 B2-B07-15
DMU 4.2-00 ADRS RGTR (B2-A08)
[-MA]
-INDEX FILE DATA
DMU 4.12-01 INDEX FILE (B2/B1-A04)
[-IFD]
DMU 4.12-03 (B2/B1-E07-08)
[-CP1]
-6
[-M6]
DMU 4.12-03 (B2/B1-E03-13)
DMU 4.12-03 (B2/B1-E07-05)
[-CP2]
+6
[-N6]
DMU 4.12-03 (B2/B1-E03-14)
-X BAR DATA
[-XD]
DMU 4.12-01
-RING DATA
[-DM2D(0-15)/-RD]
RPU 4.2-10 (B2/F1-A09→D09)
TP 51.78.49, 52.53.79, 64.54.62, 61.65.63, 59.70.66.60
DMU 4.12-01 (B2/B1-B02)
LEVEL 4 DIAGRAM
DATA MEMØRY 2
DEVELØPMENT DIVISIØN
DB-824DM; B2/B1
CODE IDENT
DWG NO
60461830
REV
A
SHEET
DMU 4.12-00
PAGE
IV-4-43



NØTES:

1. ADDRESS INPUTS FØR DØ4 AND CØ4 ARE CØNNECTED IN THE SAME ØRDER AS FØR BØ4 AND AØ4.
2. 12171 REAL PINS ARE AS FØLLØWS:
   A = 3,23,15 T = 7,11,14
   B = 4,24,16 F = 8,12,13
   C = 5,1,17
   D = 6,2,18
3. 12171 REAL PINS ARE AS FØLLØWS:
   A = 23,3,15 T = 11,7,14
   B = 24,4,16 F = 12,8,13
   C = 1,5,17
   D = 2,6,18

4. ADDRESS MUX

BIT	AUX	LSI
B0	4-6	B2-B05-06
B1	4-25	B2-B05-25
B2	4-16	B2-B05-16
B3	3-15	B2-B04-15
C0	4-8	B2-B05-08
C1	4-10	B2-B05-10
C2	4-19	B2-B05-19
C3	3-20	B2-B04-20
D0	4-7	B2-B05-07
D1	4-9	B2-B05-09
D2	4-15	B2-B05-15
D3	3-24	B2-B04-24

5. INDEX DATA

BIT	-J AUX	-J LSI	-I AUX	-I LSI
0	2-6	B2-B03-06	2-7	B2-B03-07
1	2-17	B2-B03-17	2-16	B2-B03-16
2	2-24	B2-B03-24	2-26	B2-B03-26
3	1-1	B2-B02-01	1-3	B2-B02-03
4	2-8	B2-B03-08	2-15	B2-B03-15
5	1-6	B2-B02-06	1-4	B2-B02-04
6	1-7	B2-B02-07	1-9	B2-B02-09
7	2-9	B2-B03-09	2-10	B2-B03-10
8	1-10	B2-B02-10	1-8	B2-B02-08
9	1-17	B2-B02-17	1-19	B2-B02-19
10	1-15	B2-B02-15	1-16	B2-B02-16
11	1-24	B2-B02-24	1-20	B2-B02-20

6. INDEX FILE DATA SELECT

BIT	-XD AUX	-XD LSI
0	5-26	B2-B06-26
1	4-1	B2-B05-01
2	4-3	B2-B05-03
3	5-18	B2-B06-18
4	3-9	B2-B04-09
5	3-8	B2-B04-08
6	3-17	B2-B04-17
7	3-10	B2-B04-10
8	4-26	B2-B05-26
9	3-7	B2-B04-07
10	4-24	B2-B05-24
11	4-20	B2-B05-20
12	5-10	B2-B06-10
13	5-7	B2-B06-07
14	5-17	B2-B06-17
15	5-8	B2-B06-08

7. IF LATCH

BIT	D	T
0	1	6
1	2	3
2	20	8
3	19	12
4	20	8
5	19	12
6	1	6
7	18	14
8	2	3
9	17	16
10	18	14
11	17	16
12	19	12
13	20	8
14	2	3
15	1	6

8 MAKE FØIL 6 INCHES ±1 INCH AT 1 TØ 1.

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
INDEX.DATA MEMØRY 2

DB-B24DM:B2/B1

CODE IDENT | DWG NO 60461830 | REV A
SHEET DMU 4.12-01 | PAGE IV-4-45

COMPARE DATA

12166 E15/C1 BITS 0-7

12166 D16/C2 BITS 8-15

12102 E14/A4-C/E

12102 E14/A4-D/E

12102 E14/A4-E/E

STATUS

12102 E17/A7

DMU 4.12-00 HOLDING RGTR (B2/B1-A17)

DMU 4.2-01 DATA COMP RGTR (B2-A15/B, A12/B)

-DATA = DATA COMP -(2)

-DATA (UPPER) > DATA COMP (UPPER) -(5)

-DATA (UPPER) = DATA COMP (UPPER) -(3)

-DATA (LOWER) > DATA COMP (LOWER) -(6)

-DATA (LOWER) = DATA COMP (LOWER) -(4)

-DATA > DATA COMP -(8)

TP100

TP74

-STATUS [-MS]

DMU 4.2-01 STATUS RGTR (B2-A14/A → A15/A)

COMPARE ADDRESS

12166 E12/C3 BITS 0-3

12166 E13/C4 BITS 4-11

12117 B05/0R1-A(R2)-A/C

12102 B06/A11-D/D

12102 E14/A4-B/E

12102 E14/A4-A/E

DMU 4.12-00 ADRS (B2/B1-B09)

DMU 4.2-00 ADRS COMP RGTR (B2-A11/B, A12/A)

-ADDRESS > ADDRESS COMP -(1)

-ADDRESS= ADDRESS COMPARE -(0)

TP76

TP80

TP71

TP81

NOTES:

1.

BIT	STATUS -MS AUX	STATUS -MS LSI
0	11-21	B2-B12-21
1	11-17	B2-B12-17
2	11-19	B2-B12-19
3	9-25	B2-B10-25
4	9-26	B2-B10-26
5	8-1	B2-B09-01
6	9-20	B2-B10-20
8	9-24	B2-B10-24

2.

BIT	COMPARE DATA -DC AUX	COMPARE DATA -DC LSI	COMPARE ADRS -AC AUX	COMPARE ADRS -AC LSI
0	12-4	B2-B13-04	10-25	B2-B11-25
1	12-6	B2-B13-06	10-26	B2-B11-26
2	12-7	B2-B13-07	9-1	B2-B10-01
3	12-15	B2-B13-15	9-3	B2-B10-03
4	12-16	B2-B13-16	11-25	B2-B12-25
5	12-17	B2-B13-17	11-26	B2-B12-26
6	12-19	B2-B13-19	10-1	B2-B11-01
7	12-21	B2-B13-21	10-3	B2-B11-03
8	13-7	B2-B14-07	10-4	B2-B11-04
9	13-8	B2-B14-08	10-7	B2-B11-07
10	13-9	B2-B14-09	10-8	B2-B11-08
11	13-17	B2-B14-07	10-9	B2-B11-09
12	13-19	B2-B14-19		
13	13-21	B2-B14-21		
14	13-20	B2-B14-20		
15	13-25	B2-B14-25		

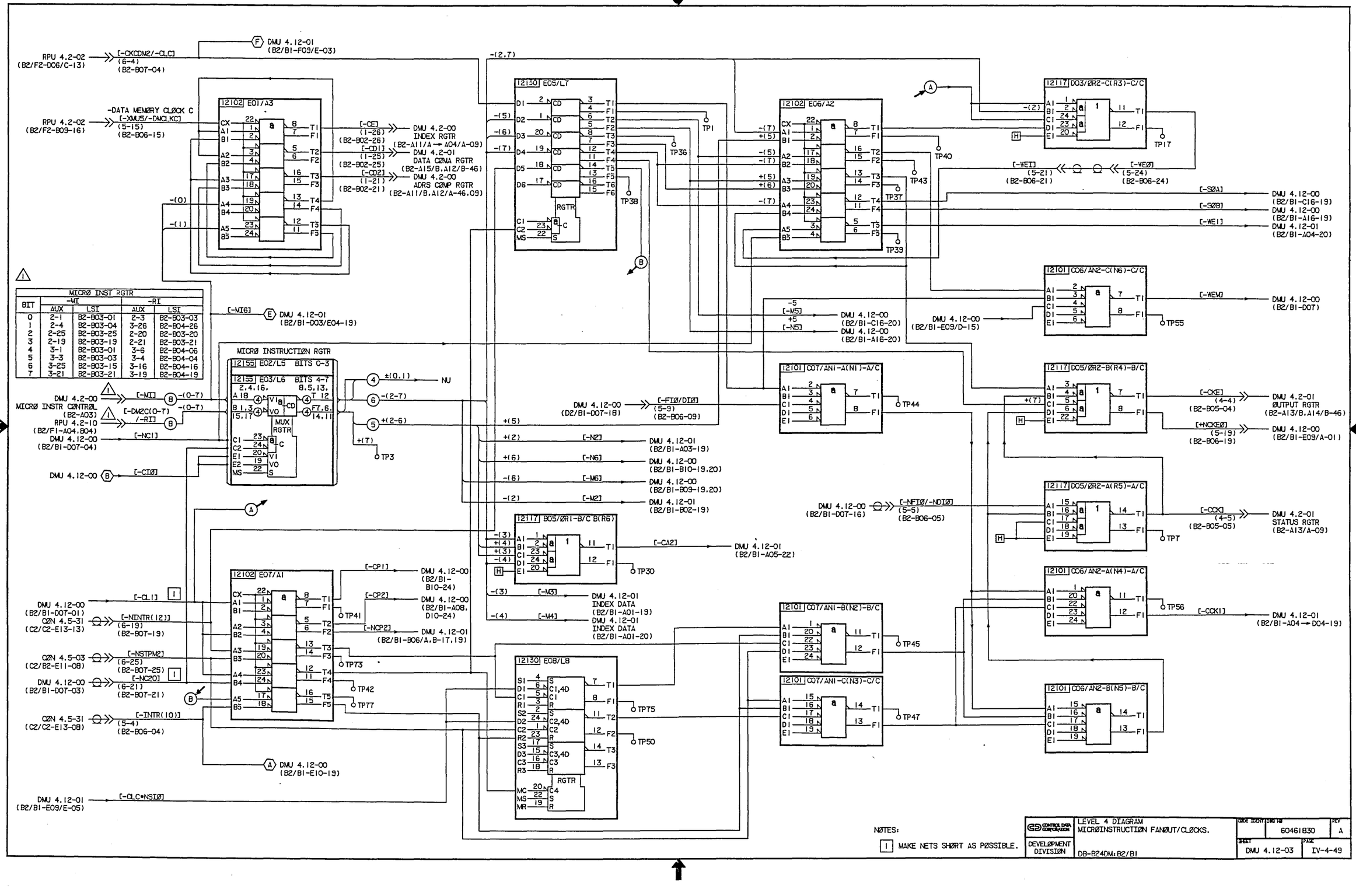
CONTROL DATA CORPORATION — DEVELOPMENT DIVISION

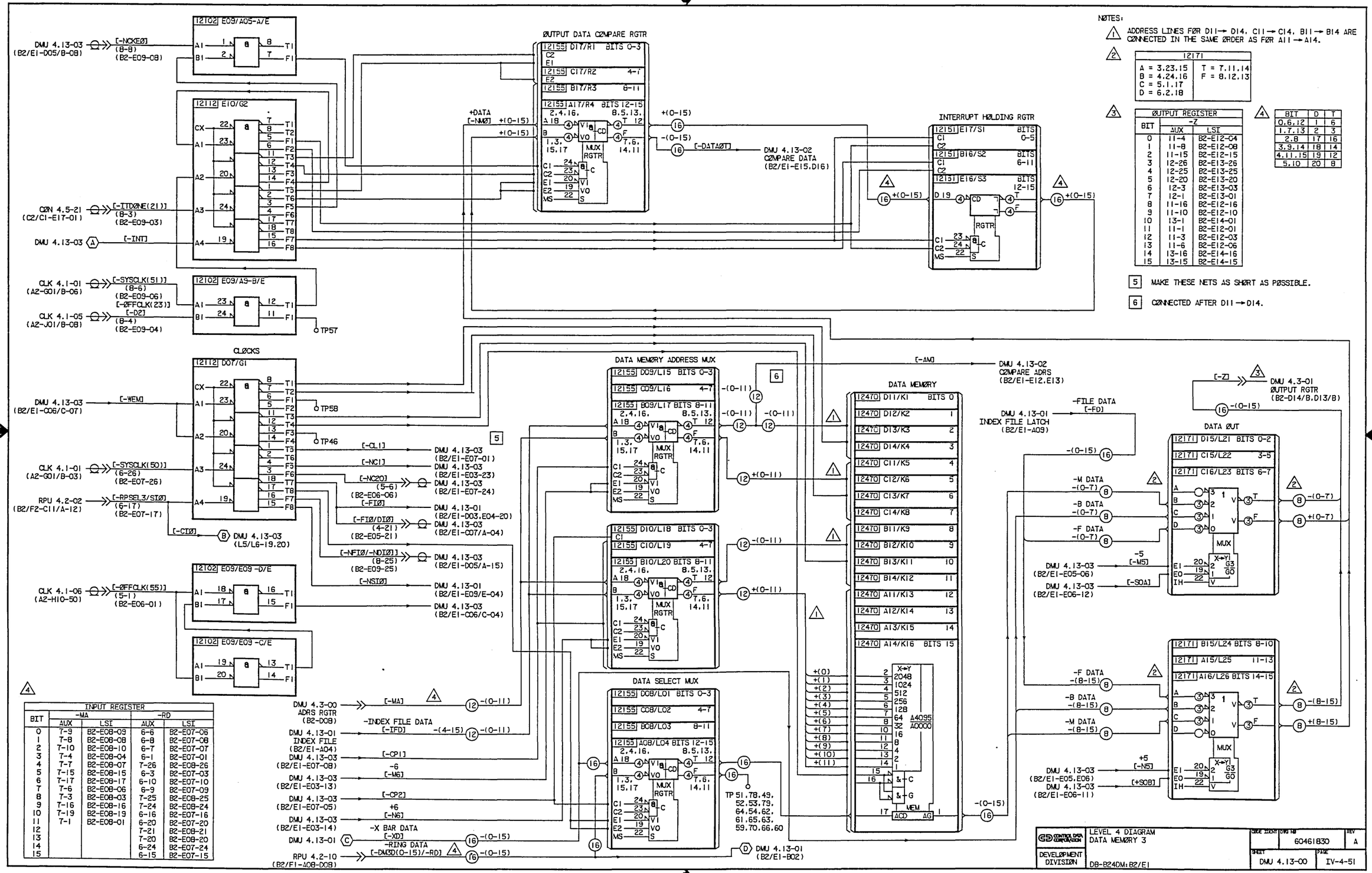
LEVEL 4 DIAGRAM
COMPARE DATA/COMPARE ADDRESS/STATUS

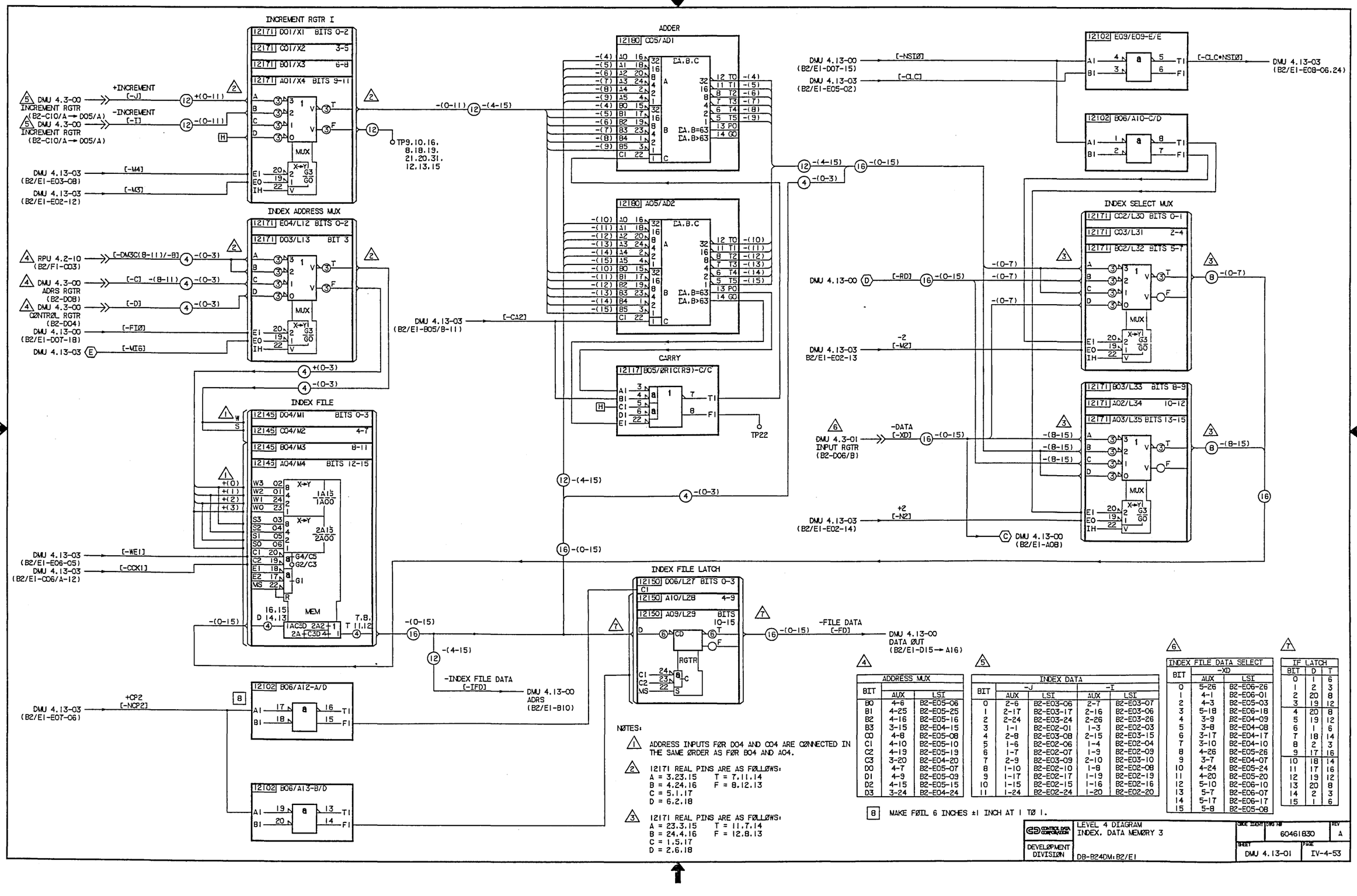
DB-B24DM:B2/B1

ORIG IDENT | DWG NO 60461830 | REV A

SHEET DMU 4.12-02 | PAGE IV-4-47


MICRØ INST RGTR
BIT | -MI AUX | -MI LSI | -RI AUX | -RI LSI
0 | 2-1 | B2-B03-01 | 2-3 | B2-B03-03
1 | 2-4 | B2-B03-04 | 3-26 | B2-B04-26
2 | 2-25 | B2-B03-25 | 2-20 | B2-B03-20
3 | 2-19 | B2-B03-19 | 2-21 | B2-B03-21
4 | 3-1 | B2-B03-01 | 3-6 | B2-B04-06
5 | 3-3 | B2-B03-03 | 3-4 | B2-B04-04
6 | 3-25 | B2-B03-15 | 3-16 | B2-B04-16
7 | 3-21 | B2-B03-21 | 3-19 | B2-B04-19
MICRØ INSTRUCTIØN RGTR
NØTES:
1 MAKE NETS SHØRT AS PØSSIBLE.
CONTROL DATA CORPORATION
DEVELØPMENT DIVISION
LEVEL 4 DIAGRAM
MICRØINSTRUCTIØN FANØUT/CLØCKS.
DB-824DM:B2/B1
60461830
A
DMU 4.12-03
IV-4-49


NOTES:
1 ADDRESS LINES FØR D11→D14, C11→C14, B11→B14 ARE CONNECTED IN THE SAME ØRDER AS FØR A11→A14.
2 12171: A = 3,23,15 B = 4,24,16 C = 5,1,17 D = 6,2,18 T = 7,11,14 F = 8,12,13
3 ØUTPUT REGISTER: BIT | -Z AUX | -Z LSI
0 11-4 B2-E12-C4
1 11-8 B2-E12-08
2 11-15 B2-E12-15
3 12-26 B2-E13-26
4 12-25 B2-E13-25
5 12-20 B2-E13-20
6 12-3 B2-E13-03
7 12-1 B2-E13-01
8 11-16 B2-E12-16
9 11-10 B2-E12-10
10 13-1 B2-E14-01
11 11-1 B2-E12-01
12 11-3 B2-E12-03
13 11-6 B2-E12-06
14 13-16 B2-E14-16
15 13-15 B2-E14-15
4 BIT | D | T: 0,6,12 | 1 | 6; 1,7,13 | 2 | 3; 2,8 | 17 | 16; 3,9,14 | 18 | 14; 4,11,15 | 19 | 12; 5,10 | 20 | 8
5 MAKE THESE NETS AS SHØRT AS PØSSIBLE.
6 CØNNECTED AFTER D11→D14.
12102 E09/A05-A/E
DMU 4.13-03 (B2/E1-D05/B-08)
[-NCKEØ] (8-8) (B2-E09-08)
12112 E10/G2
CØN 4.5-21 (C2/C1-E17-01)
[-ITDØNE(21)] (8-3) (B2-E09-03)
DMU 4.13-03
[-INT]
12102 E09/A5-B/E
CLK 4.1-01 (A2-G01/B-06)
[-SYSCLK(51)] (8-6) (B2-E09-06)
[-ØFFCLK(23)]
CLK 4.1-05 (A2-J01/B-08)
[-D2] (8-4) (B2-E09-04)
TP57
ØUTPUT DATA CØMPARE RGTR
12155 D17/R1 BITS 0-3
12155 C17/R2 4-7
12155 B17/R3 8-11
12155 A17/R4 BITS 12-15
+DATA [-NMØ] +(0-15) +(0-15)
+(0-15)
-(0-15)
[-DATAØT]
DMU 4.13-02 CØMPARE DATA (B2/E1-E15,D16)
INTERRUPT HØLDING RGTR
12151 E17/S1 BITS 0-5
12151 B16/S2 BITS 6-11
12131 E16/S3 BITS 12-15
+(0-15)
RGTR
CLØCKS
12112 D07/G1
DMU 4.13-03 (B2/E1-C06/C-07)
[-WEM]
TP58
TP46
CLK 4.1-01 (A2-G01/B-03)
[-SYSCLK(50)] (6-26) (B2-E07-26)
RPU 4.2-02 (B2/F2-C11/A-12)
[-RPSEL3/STIØ] (6-17) (B2-E07-17)
[-CIØ]
DMU 4.13-03 (L5/L6-19,20)
[-CL1] DMU 4.13-03 (B2/E1-E07-01)
[-NC1] DMU 4.13-03 (B2/E1-E03-23)
[-NC20] (5-6) (B2-E06-06) DMU 4.13-03 (B2/E1-E07-24)
[-FIØ]
[-FIØ/DIØ] (4-21) (B2-E05-21) DMU 4.13-01 (B2/E1-D03,E04-20) DMU 4.13-03 (B2/E1-C07/A-04)
[-NFIØ/-NDIØ] (8-25) (B2-E09-25) DMU 4.13-03 (B2/E1-D05/A-15)
[-NSIØ] DMU 4.13-01 (B2/E1-E09/E-04)
DMU 4.13-03 (B2/E1-C06/C-04)
12102 E09/E09-D/E
CLK 4.1-06 (A2-H10-50)
[-ØFFCLK(55)] (5-1) (B2-E06-01)
12102 E09/E09-C/E
DATA MEMØRY ADDRESS MUX
12155 D09/L15 BITS 0-3
12155 C09/L16 4-7
12155 B09/L17 BITS 8-11
12155 A09/L18 BITS 12-15
12155 D10/L18 BITS 0-3
12155 C10/L19 4-7
12155 B10/L20 BITS 8-11
12155 A10/L21 BITS 12-15
DATA SELECT MUX
12155 D08/L01 BITS 0-3
12155 C08/L02 4-7
12155 B08/L03 8-11
12155 A08/L04 BITS 12-15
TP 51,78,49, 52,53,79, 64,54,62, 61,65,63, 59,70,66,60
DATA MEMØRY
12470 D11/K1 BITS 0
12470 D12/K2 1
12470 C13/K3 2
12470 D14/K4 3
12470 C11/K5 4
12470 C12/K6 5
12470 C13/K7 6
12470 C14/K8 7
12470 B11/K9 8
12470 B12/K10 9
12470 B13/K11 10
12470 B14/K12 11
12470 A11/K13 12
12470 A12/K14 13
12470 A13/K15 14
12470 A14/K16 BITS 15
A4095 A0000
MEM
[-AM] DMU 4.13-02 CØMPARE ADRS (B2/E1-E12,E13)
-FILE DATA [-FD]
DMU 4.13-01 INDEX FILE LATCH (B2/E1-A09)
[-ZJ] DMU 4.3-01 ØUTPUT RGTR (B2-D14/B,D13/B)
DATA ØUT
12171 D15/L21 BITS 0-2
12171 C15/L22 3-5
12171 C16/L23 BITS 6-7
12171 B15/L24 BITS 8-10
12171 A15/L25 11-13
12171 A16/L26 BITS 14-15
-M DATA -(0-7)
-B DATA -(0-7)
-F DATA -(0-7)
-5 [-M5]
DMU 4.13-03 (B2/E1-E05-06)
[-SØA] DMU 4.13-03 (B2/E1-E06-12)
-F DATA -(8-15)
-B DATA -(8-15)
-M DATA -(8-15)
+5 [-N5]
DMU 4.13-03 (B2/E1-E05,E06)
[+SØB] DMU 4.13-03 (B2/E1-E06-11)
MUX
INPUT REGISTER: BIT | -MA AUX | -MA LSI | -RD AUX | -RD LSI
0 7-9 B2-E08-09 6-6 B2-E07-05
1 7-8 B2-E08-08 6-8 B2-E07-08
2 7-10 B2-E08-10 6-7 B2-E07-07
3 7-4 B2-E08-04 6-1 B2-E07-01
4 7-7 B2-E08-07 7-26 B2-E08-26
5 7-15 B2-E08-15 6-3 B2-E07-03
6 7-17 B2-E08-17 6-10 B2-E07-10
7 7-6 B2-E08-06 6-9 B2-E07-09
8 7-3 B2-E08-03 7-25 B2-E08-25
9 7-16 B2-E08-16 7-24 B2-E08-24
10 7-19 B2-E08-19 6-16 B2-E07-16
11 7-1 B2-E08-01 6-20 B2-E07-20
12 7-21 B2-E08-21
13 7-20 B2-E08-20
14 6-24 B2-E07-24
15 6-15 B2-E07-15
DMU 4.3-00 ADRS RGTR (B2-D08) [-MA] -(0-11)
-INDEX FILE DATA [-IFD] -(4-15) -(0-11)
DMU 4.13-01 INDEX FILE (B2/E1-A04)
DMU 4.13-03 (B2/E1-E07-08) [-CP1] -6 [-M6]
DMU 4.13-03 (B2/E1-E03-13)
DMU 4.13-03 (B2/E1-E07-05) [-CP2] +6 [-N6]
DMU 4.13-03 (B2/E1-E03-14)
-X BAR DATA [-XD1]
DMU 4.13-01
-RING DATA [-DM3D(0-15)/-RD]
RPU 4.2-10 (B2/F1-A08-D08)
DMU 4.13-01 (B2/E1-B02)
LEVEL 4 DIAGRAM DATA MEMØRY 3
DEVELOPMENT DIVISION
DØ-B24DM: B2/E1
CODE IDENT 60461830 REV A
SHEET DMU 4.13-00 PAGE IV-4-51



NØTES:

1. ADDRESS INPUTS FØR D04 AND C04 ARE CØNNECTED IN THE SAME ØRDER AS FØR B04 AND A04.
2. 12171 REAL PINS ARE AS FØLLØWS:
   A = 3.23.15 T = 7.11.14
   B = 4.24.16 F = 8.12.13
   C = 5.1.17
   D = 6.2.18
3. 12171 REAL PINS ARE AS FØLLØWS:
   A = 23.3.15 T = 11.7.14
   B = 24.4.16 F = 12.8.13
   C = 1.5.17
   D = 2.6.18

4

ADDRESS MUX		
BIT	AUX	LSI
B0	4-6	B2-E05-06
B1	4-25	B2-E05-25
B2	4-16	B2-E05-16
B3	3-15	B2-E04-15
C0	4-8	B2-E05-08
C1	4-10	B2-E05-10
C2	4-19	B2-E05-19
C3	3-20	B2-E04-20
D0	4-7	B2-E05-07
D1	4-9	B2-E05-09
D2	4-15	B2-E05-15
D3	3-24	B2-E04-24

5

INDEX DATA				
BIT	-J		-I	
	AUX	LSI	AUX	LSI
0	2-6	B2-E03-06	2-7	B2-E03-07
1	2-17	B2-E03-17	2-16	B2-E03-06
2	2-24	B2-E03-24	2-26	B2-E03-26
3	1-1	B2-E02-01	1-3	B2-E02-03
4	2-8	B2-E03-08	2-15	B2-E03-15
5	1-6	B2-E02-06	1-4	B2-E02-04
6	1-7	B2-E02-07	1-9	B2-E02-09
7	2-9	B2-E03-09	2-10	B2-E03-10
8	1-10	B2-E02-10	1-8	B2-E02-08
9	1-17	B2-E02-17	1-19	B2-E02-19
10	1-15	B2-E02-15	1-16	B2-E02-16
11	1-24	B2-E02-24	1-20	B2-E02-20

8 MAKE FØIL 6 INCHES ±1 INCH AT 1 TØ 1.

6

INDEX FILE DATA SELECT		
BIT	-XD	
	AUX	LSI
0	5-26	B2-E06-26
1	4-1	B2-E06-01
2	4-3	B2-E05-03
3	5-18	B2-E06-18
4	3-9	B2-E04-09
5	3-8	B2-E04-08
6	3-17	B2-E04-17
7	3-10	B2-E04-10
8	4-26	B2-E05-26
9	3-7	B2-E04-07
10	4-24	B2-E05-24
11	4-20	B2-E05-20
12	5-10	B2-E06-10
13	5-7	B2-E06-07
14	5-17	B2-E06-17
15	5-8	B2-E05-08

7

IF LATCH		
BIT	D	T
0	1	6
1	2	3
2	20	8
3	19	12
4	20	8
5	19	12
6	1	6
7	18	14
8	2	3
9	17	16
10	18	14
11	17	16
12	19	12
13	20	8
14	2	3
15	1	6

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
INDEX. DATA MEMØRY 3

DB-8240M: B2/E1

CAGE IDENT | DWG NO: 60461830 | REV: A
SHEET: DMU 4.13-01 | PAGE: IV-4-53

COMPARE DATA

12166 E15/C1 BITS 0-7

12166 D16/C2 BITS 8-15

12166 E12/C3 BITS 0-3

12166 E13/C4 BITS 4-11

DMU 4.13-00 HOLDING RGTR (B2/E1-A17) [-DATAØT] 16 -(0-15)

DMU 4.3-01 DATA COMP RGTR (B2-C14/B.D10/B) [-DC] 2 16 -(0-15)

DMU 4.13-00 ADRS (B2/E1-B09) [-AM] 12 -(0-11)

DMU 4.3-00 ADRS COMP RGTR (B2-C10/B.D10/B) [-AC] 2 12 -(0-11)

07 LE A≤B
08 EQ A=B
11 GE A≥B

TP100
TP76
TP80
TP71
TP81
TP74

12102 E14/A4-D/E
12102 E14/A4-E/E
12102 E14/A4-C/E
12102 E11/A7
12102 B06/A11-D/D
12117 B05/2R1-A(R2)-A/C
12102 E14/A4-B/E
12102 E14/A4-A/E

-DATA = DATA COMP -(2)
-DATA (UPPER) > DATA COMP (UPPER) -(5)
-DATA (UPPER) = DATA COMP (UPPER) -(3)
-DATA (LOWER) > DATA COMP (LOWER) -(6)
-DATA (LOWER) = DATA COMP (LOWER) -(4)
-DATA > DATA COMP -(8)

COMPARE ADDRESS

-ADDRESS > ADDRESS COMP -(1)
-ADDRESS= ADDRESS COMPARE -(0)

STATUS

B -(0-6,8) -STATUS [-MS] 1 DMU 4.3-01 STATUS RGTR (B2-D14/A→C14/A)

NOTES:

1

BIT	STATUS -MS AUX	STATUS -MS LSI
0	11-21	B2-E12-21
1	11-17	B2-E12-17
2	11-19	B2-E12-19
3	9-25	B2-E10-25
4	9-26	B2-E10-26
5	8-1	B2-E09-01
6	9-20	B2-E10-20
8	9-24	B2-E10-24

2

BIT	COMPARE DATA -DC AUX	COMPARE DATA -DC LSI	COMPARE ADRS -AC AUX	COMPARE ADRS -AC LSI
0	12-4	B2-E13-04	10-25	B2-E11-25
1	12-6	B2-E13-06	10-26	B2-E11-26
2	12-7	B2-E13-07	9-1	B2-E10-01
3	12-15	B2-E13-15	9-3	B2-E10-03
4	12-16	B2-E13-16	9-25	B2-E12-25
5	12-17	B2-E13-17	9-26	B2-E12-26
6	12-19	B2-E13-19	10-1	B2-E11-01
7	12-21	B2-E13-21	10-3	B2-E11-03
8	13-7	B2-E14-07	10-4	B2-E11-04
9	13-8	B2-E14-08	10-7	B2-E11-07
10	13-9	B2-E14-09	10-8	B2-E11-08
11	13-17	B2-E14-07	10-9	B2-E11-09
12	13-19	B2-E14-19		
13	13-21	B2-E14-21		
14	13-20	B2-E14-20		
15	13-25	B2-E14-25		

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
COMPARE DATA/COMPARE ADDRESS/STATUS
2M04

DB-B24DM:B2/E1

CAGE IDENT
DWG NO 60461830
REV A
SHEET DMU 4.13-02
PAGE IV-4-55

RPU 4.2-02 (B2/F2-D10/C-13) [-CKCDM3/-CLC] (6-4) (B2-E07-04)

RPU 4.2-02 (B2/F2-B09-13) -DATA MEMØRY CLØCK C [-XM(18)/-DMCLKC] (5-15) (B2-E06-15)

12102 E01/A3

[-CE] (1-26) (B2-E02-26) → DMU 4.3-00 INDEX RGTR (B2-C10/A → D05/A-09)

[-CD1] (1-25) (B2-E02-25) → DMU 4.3-01 DATA C2MA RGTR (B2-C14/B,D10/B-46)

[-CD2] (1-21) (B2-E02-21) → DMU 4.3-00 ADRS C2MP RGTR (B2-C10/B,D10/A-46.09)

-(0)

-(1)

NØTE:

1

MICRØ INST RGTR				
BIT	-MI		-RI	
	AUX	LSI	AUX	LSI
0	2-1	B2-E03-01	2-3	B2-E03-03
1	2-4	B2-E03-04	3-26	B2-E04-26
2	2-25	B2-E03-25	2-20	B2-E03-20
3	2-19	B2-E03-19	2-21	B2-E03-21
4	3-1	B2-E04-01	3-6	B2-E04-06
5	3-3	B2-E04-03	3-4	B2-E04-04
6	3-25	B2-E04-25	3-16	B2-E04-16
7	3-21	B2-E04-21	3-19	B2-E04-19

DMU 4.3-00 MICRØ INSTR CØNT (B2-D04) [-MI] (B) -(0-7)

RPU 4.2-10 (B2/F1-A03,B03) [-DM3C(0-7)/-RI] (B) -(0-7)

DMU 4.13-00 (B2/E1-D07-04) [-NCI]

DMU 4.13-00 (B) [-CIØ]

[MI6] (E) DMU 4.13-01 (B2/E1-D03,E04-19)

MICRØ INSTRUCTIØN RGTR

12155 E02/L5 BITS 0-3

12155 E03/L6 BITS 4-7

2,4,16, 8,5,13, T 12

A 18 B 1,3 15,17 F7,6, 14,11

MUX RGTR

(4) ±(0.1) → NU

(6) -(2-7)

(5) +(2-6)

+(7) → TP3

12130 E05/L7

D1 D2 D3 D4 D5 D6 → T1 F1 T2 F2 T3 F3 T4 F4 T5 F5 T6 F6

RGTR

C1 C2 MS

-(2,7)

-(5) -(6) -(7)

TP1 TP36 TP38

B

12102 E06/A2

-(7) +(5) -(5) -(7) +(5) +(6) -(7)

TP40 TP43 TP37 TP39

A

12117 D03/ØR5-C(R3)-C/C

-(2) H

TP17

[-WEI] (5-21) (B2-E06-21)

[-WEØ] (5-24) (B2-E06-24)

[-SØA] → DMU 4.13-00 (B2/E1-C16-19)

[-SØB] → DMU 4.13-00 (B2/E1-A16-19)

[-WEI] → DMU 4.13-01 (B2/E1-A04-20)

12101 C06/AN2-C(N6)-C/C

DMU 4.13-00 (B2/E1-E09/D-15)

TP55

[-WEW] → DMU 4.13-00 (B2/E1-D07)

-5 [-M5] → DMU 4.13-00 (B2/E1-C16-20)

+5 [-N5] → DMU 4.13-00 (B2/E1-A16-20)

12101 C07/AN1-A(N1)-A/C

DMU 4.13-00 (B2/E1-D07-18) [-FIØ/DIØ] (5-9) (B2-E06-09)

TP44

12117 D05/ØR2-B(R4)-B/C

+(7) H

[-CKE] (4-4) (B2-E05-04) → DMU 4.3-01 ØUTPUT RGTR (B2-D13/B,D14/B-46)

[+NCKEØ] (5-19) (B2-E06-19) → DMU 4.13-00 (A05-1) (B2/E1-E09/A-01)

+(5) +(2) [-N2] → DMU 4.13-01 (B2/E1-A03-19)

+(6) [-N6] → DMU 4.13-00 (B2/E1-B10-19,20)

-(6) [-M6] → DMU 4.13-00 (B2/E1-B09-19,20)

-(2) [-M2] → DMU 4.13-01 (B2/E1-B02-19)

12117 E05/ØR1-B/C B(R6)

-(3) +(4) +(3) -(4) H

[-CA2] → DMU 4.13-01 (B2/E1-A05-22)

TP30

-(3) [-M3] → DMU 4.13-01 INDEX DATA (B2/E1-A01-19)

-(4) [-M4] → DMU 4.13-01 INDEX DATA (B2/E1-A01-20)

DMU 4.13-00 (B2/E1-D07-16) [-NFIØ/-NDIØ] (5-5) (B2-E06-05)

12117 D05/ØR2-A(R5)-A/C

H

TP7

[-CCK] (4-5) (B2-E05-05) → DMU 4.3-01 STATUS RGTR (B2-D13/A-09)

12101 C06/AN2-A(N4)-A/C

TP56

[-CCK1] → DMU 4.13-01 (B2/E1-A04 → D04-19)

12102 E07/A1

DMU 4.13-00 (B2/E1-D07-01) [-CL1] 1

C2N 4.5-31 (C2/C2-E17-01) [-NINTR(16)] (6-19) (B2-E07-19)

C2N 4.5-03 (C2/B1-E11-07) [-NSTPM3] (6-25) (B2-E07-25) 1

DMU 4.13-00 (B2/E1-D07-03) [-NC20] (6-21) (B2-E07-21)

(B)

[-CP1] → DMU 4.13-00 (B2/E1-B10-24)

TP41

[-CP2] → DMU 4.13-00 (B2/E1-A08, D10-24)

+CP2 [-NCP2] → DMU 4.13-01 (B2/E1-B06/A,B-17,19)

TP73 TP42 TP77

12130 E08/L8

S1 D1 C1 R1 S2 D2 C2 R2 S3 D3 C3 R3 MC MS MR

C1,4D C2,4D C3,4D C4

RGTR

TP75 TP50

12101 C07/AN1-B(N2)-B/C

TP45

12101 C07/AN1-C(M3)-C/C

TP47

12101 C06/AN2-B(N5)-B/C

C2N 4.5-31 (C2/C2-E13-07) [-INTR(11)] (5-4) (B2-E06-04) → A DMU 4.13-00 (B2/E1-E10-19)

DMU 4.13-01 (B2/E1-E09/E-05) [-CLC*NSIØ]

NØTES:

1 MAKE NETS SHØRT AS PØSSIBLE.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM MICRØINSTRUCTIØN FANØUT/CLØCKS. 2MO4	DRAWING NO	REV
		60461830	A
DEVELØPMENT DIVISIØN	DB-B24DM:B2/E1	SHEET DMU 4.13-03	SIZE IV-4-57

5. FILE UNIT (FGU)

SYSTEM FUNCTION

The file unit, which is located in the base processor, provides temporary storage for operands and is used during processing to coordinate timing between data paths.

GENERAL DESCRIPTION

The file unit consists of two independent memories, or files, known as file F and file G. Each file is made up of sixteen 16-bit addressable memory locations divided into two groups of eight, the lower eight or the upper eight. The file unit takes one clock cycle for an operation.

One 16-bit data word may be written into one location, and the same data read from the same location or another 16-bit data word read from a different location each clock cycle, as long as the write and read addresses are from the same group of eight. During a clock cycle either one or both files may be used, but the addresses accessed in one file must come from the same numerical group of eight as in the other file.

LOCATION

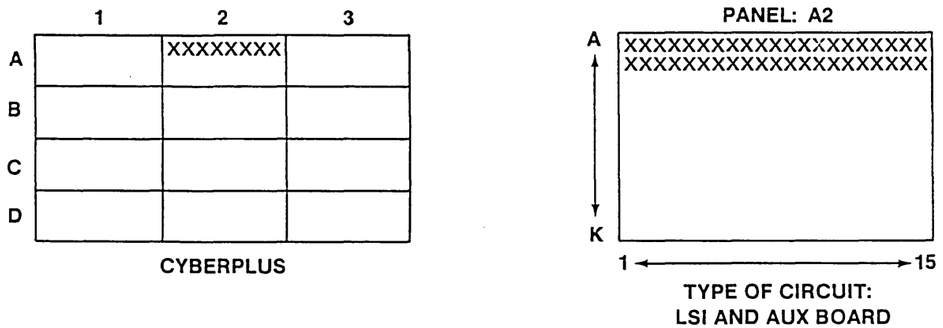


Figure IV-5-1. Location of File Unit Logic Circuits

FUNCTIONAL DESCRIPTION

The discussion in the following paragraphs refers to the simplified block diagram of the file unit as shown in figure IV-5-2 and the level 2 diagram FGU 2.0. The 13-bit control register receives the 12-bit operation code from the 16-bit dynamic control field of the instruction word and the additional bit from the file unit clock C (bit 47 of the clock control field). The data in the control register specify the read and write addresses for each of the two files. The clock C bit is appended to each file address to specify in which group of eight (0-7 or 8-F) the addresses reside. Therefore, because there is only one clock C, both files must be functioning in the same numerical group of eight address locations each cycle.

The F and G data registers receive data from the crossbar when enabled by the A and B clocks, respectively. The A and B clocks, bits 23 and 24, are set by the program into the clock control field of the instruction word. Bit 23, when set, gates data to the F data register from crossbar output 11, and bit 24, when set, gates data to the G data register from crossbar output 12. The clock bits gate the data at time 0 of clock cycle one when they are set. If the clock bits are clear, the contents of the file registers are not changed because no writing occurs.

The F and G data files (memories) receive two addresses from the file control logic each time the file unit is specified by the program in one of the dynamic control fields of the instruction word. One address is the write address, and the other address is the read address. If no address is specified, they default to address zero. During the first half of clock cycle one, the writes are performed, if the A and/or B clocks are present. If either or both of these clocks are missing, no write is performed in the corresponding file memory. During the second half of the clock cycle, the reads are performed. The read operation does not require any clocks, so everytime the file unit is addressed by the program, data is read from both files and entered into both output registers, respectively.

The status register records the sign (MSB) of the contents of the output registers and is available at the end of the second cycle.

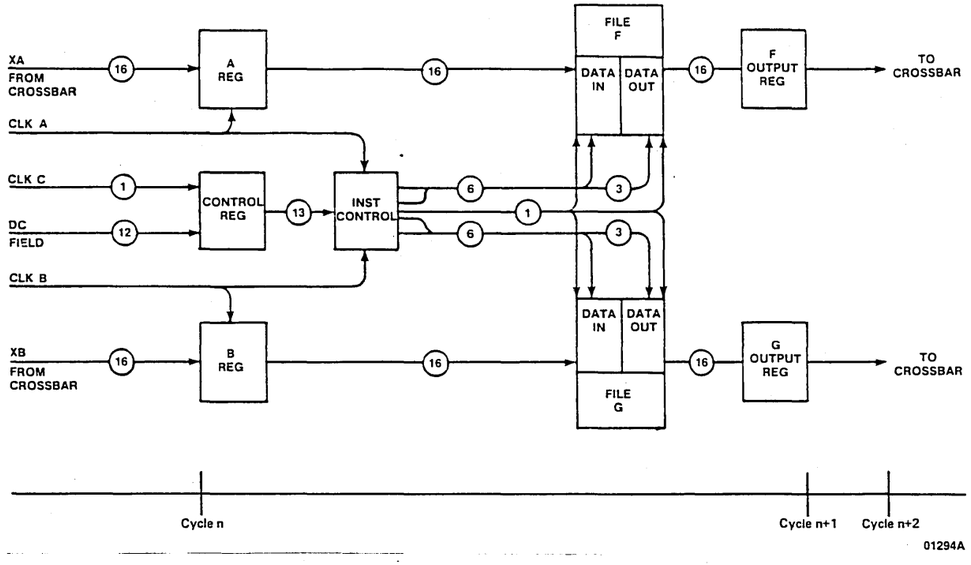


Figure IV-5-2. File Unit Block Diagram

TIMING

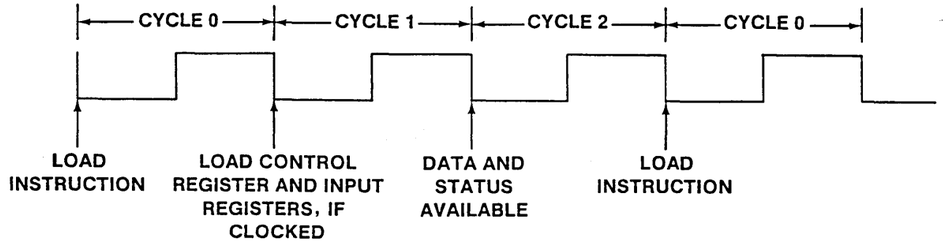


Figure IV-5-3. File Unit Instructions Timing

LSI A2

2A01
AUX A2/F1

LSI A2

CØN 2.0
DATA X BAR

F DATA

16

F
DATA
REGISTER
FGU 4.0-00

16

16

SHADØW

F
FILE
DATA
16 X 16

ADDRESS
FGU 4.1-00

CØN 2.0
CLØCK BITS FANØUT

FICLKA

WRITE ENABLE

16

F
ØUTPUT
REGISTER
FGU 4.0-01

16

16

SHADØW

CØN 2.0
DATA X BAR

CØN 3.0
CLØCK BITS FANØUT

FICLKC

EXTEND

4

3

STATUS
VECTØR
REGISTER
FGU 4.0-01

2

CØN 2.0

1

SHADØW

CØN 2.0
DC FIELDS FANØUT

FILE ØP

12

16

FILE
CØNTRØL
FGU 4.0-00

8

F ADDRESS

8

G ADDRESS

12

SHADØW

CØN 2.0
X BAR INPUT

SHADØW

16

SHADØW
WIRED
'AND' 12
⚠1
FGU 4.0-02

16

CØN 2.0

CØN 2.0
CLØCK BITS FANØUT

FICLKB

WRITE ENABLE

ADDRESS
16 X 16
G
FILE
DATA
FGU 4.1-00

CØN 2.0
DATA X BAR

G DATA

16

G
DATA
REGISTER
FGU 4.0-00

16

16

SHADØW

16

G
ØUTPUT
REGISTER
FGU 4.0-01

16

16

SHADØW

CØN 2.0
DATA X BAR

NØTE:

⚠1 SHADØW RGTR AND WIRED 'AND' DUPLICATED ØN SHA 2.0.

CONTROL DATA CORPORATION	LEVEL 2 DIAGRAM REGISTER FILE UNIT	CODE IDENT / DWG NO: 60461830	REV: A
DEVELØPMENT DIVISIØN		SHEET: FGU 2.0	PAGE: IV-5-3

CLK 4.1-00 (A2-K15/B-46.51.01.08)
CLK 4.1-02 (A2-A01/B-48)
CLK 4.1-02 (A2-A01/A-31)
CØN 4.5-21 (C2/C1-E05-12)
CØN 4.3-00 (A2-H10-19)
CØN 4.5-21 (C2/C1-E05-17)
CØN 4.1-00 (C2-E12/B-47)
CØN 4.1-00 DC FIELDS FANØUT (C2-E01/A→E15/A-23)
CØN 4.1-00 (C2-F09-04)
CØN 4.5-21 (C2/C1-E13-01)
SHA 4.0-01 (B2-C07/B-02)
CØN 4.3-00 (A2-H10-33)
CØN 4.2-01 DATA X BAR (C2-K07→G11-50)
CØN 4.5-01 (C2/B1-D02-05)
SHA 4.0-02 (B2-C09/A-28)
CØN 4.2-01 DATA X BAR (C2-K12-G15-24)
CØN 4.5-01 (C2/B1-D02-07)
SHA 4.0-02 (B2-C09/B-02)

-C0 [-8B41-C2] -C4 [-8B42-C1] -C8 [-8B43-C2] -C12 [-8B44-C2]
+C2 [+8B43-C1]
+C15 [+8B41-C1]
-INT DØNE [-ITDØNE(5)]
+INT RGTR [-NINTR(12)]
-INT DØNE [-ITDØNE(7)]
-CLØCK BIT 47 [-CLK47/FICLKC]
-FILE DC FIELD (0-11) [-FID(0-8)8/FILEØP]
-LØAD FILE CØNTRØL RGTR [-GØU(8)/GØFG]
-INT DØNE [-ITDØNE(8)]
-SHADØW RØW SELECT 1 [-URS1(6)]
+INT RGTR [-NINTR(15)]
-X BAR 11 ØUT (0-15) [-XBØB(0-15)(11)/FDATA]
-CLØCK BIT 23 [-CLK23/FICLKA]
-SHADØW RØW SELECT 2 [-URS2(6)]
-X BAR 12 ØUT (0-15) [-XBØC(0-15)(12)/GDATA]
-CLØCK BIT 24 [-CLK24/FICLKB]
-SHADØW RØW SELECT 3 [-URS3(6)]

EXTEND
-(0-3)
-(0-11)
-(4-15)
+(C2,C15),-(C4,C12)
-(C0,C4,C8,C12)
-(7,8)
-(7,8)
-(7)
-(8)
SBU 4.0-03
FGU 4.0-01 (A2-G15/A-08)
SBU 4.0-00 SBU 4.0-02 SBU 4.1-03
MPY 4.0-08
-(0)
-(C0.C4)
-(C8.C12)
-INT DØNE [-ITDØNE(7)]
-INT DØNE [-ITDØNE(8)]
-(1)
-(0,1)
-F/G CLK (0,1)
FGU 4.1-00 (A2/F1-E11-24,23)

FILE CØNTRØL

12DB HC8/8B41-A/B +C15 BITS 0,4-6
XFR
12DB JC8/8B42-A/B -C4 1,7-9
ENS
12DB HI4/8B43-A/B +C2 2,10-12
XFR
12DB JI4/8B44-A/B -C12 BITS 3,13-15
A(0-3) 17,18, 36,37
CI 3
ENI 9
XFR 8
GØI 35
ENS 10
MASTER SLAVE
CID C2D RGTR X→Y
23,27,30,33 26,28,31,34
D(0-3) C(0-3)
E(0-3) 24,25, 29,32
GI
2 ØØ

-(C26)
-(0) [-NFCLKC] → NU
-(2) -(3) +FICLC [-NFICLC] → FGU 4.0-01 G FILE DATA ØUTPUT RGTR (A2-H15/A-37)
-(0,1,4-9) -F ADDRESS → FGU 4.1-00 F FILE DATA (A2/F1-D09→E10)
-(0-15) -(2,3,10-15) -G ADDRESS → FGU 4.1-00 F FILE DATA (A2/F1-D12→E13)
-(4-15) -(0-11) -FILE CØNTRØL TØ SHADØW [-WAND12] → FGU 4.0-02

F DATA RGTR

12DB HC8/8B41-B/B -C0 BITS 0-7
XFR
12DB JC8/8B42-B/B -C4 BITS 8-15
B(0-7) 16,15,11, 12,44,38, 41,42
C2 2
EN2 46
XFR 8
G02 43
ENS 10
F(0-7) 22,21,6,4, 51,49,47, 45
G(0-7) 19,20,7,5, 1,52,50,48
1 ØØ

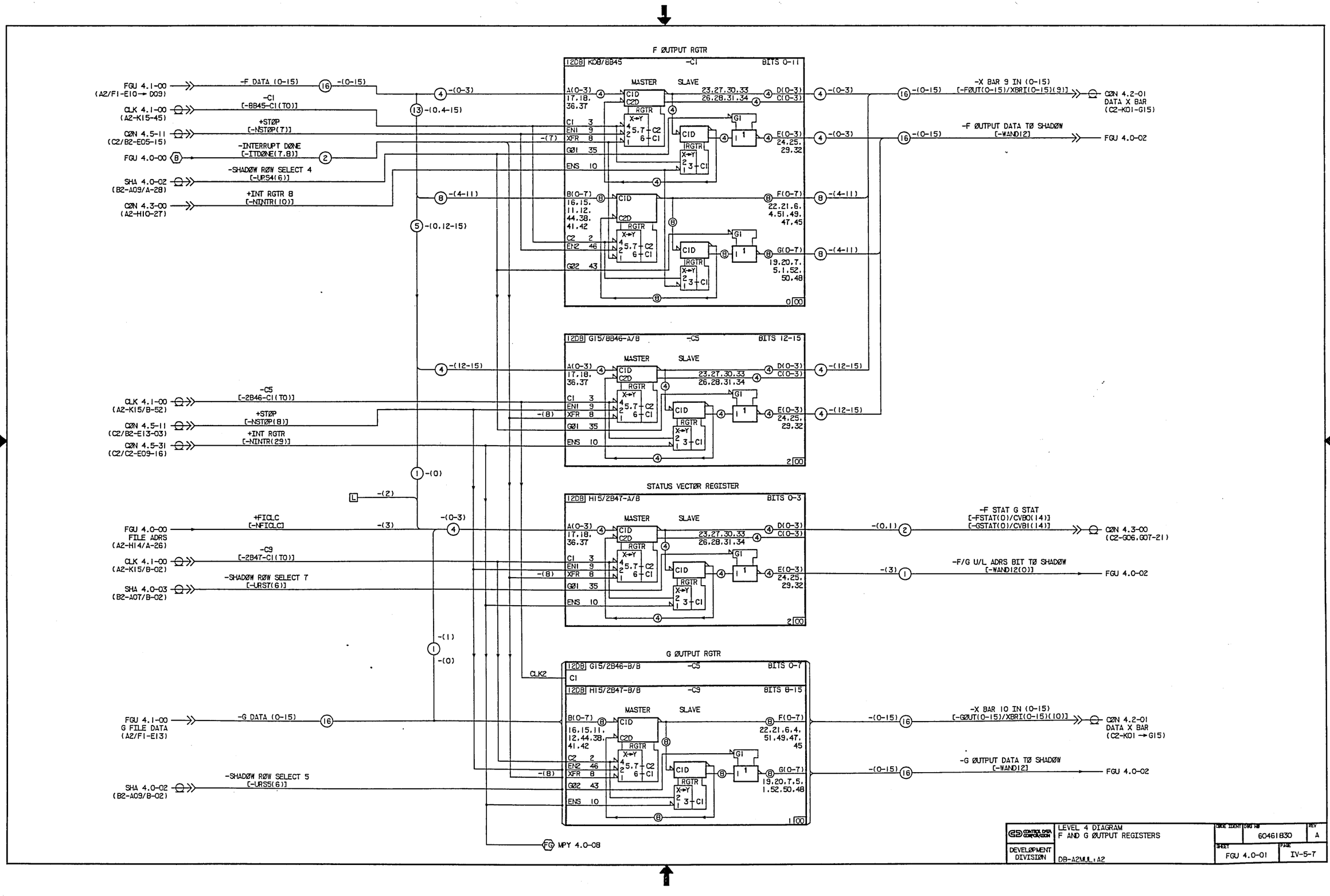
-(0-15) 16 -F DATA → FGU 4.1-00 F FILE DATA (A2/F1-D09→G10)
-(0-15) 16 -F DATA TØ SHADØW [-WAND12] → FGU 4.0-02

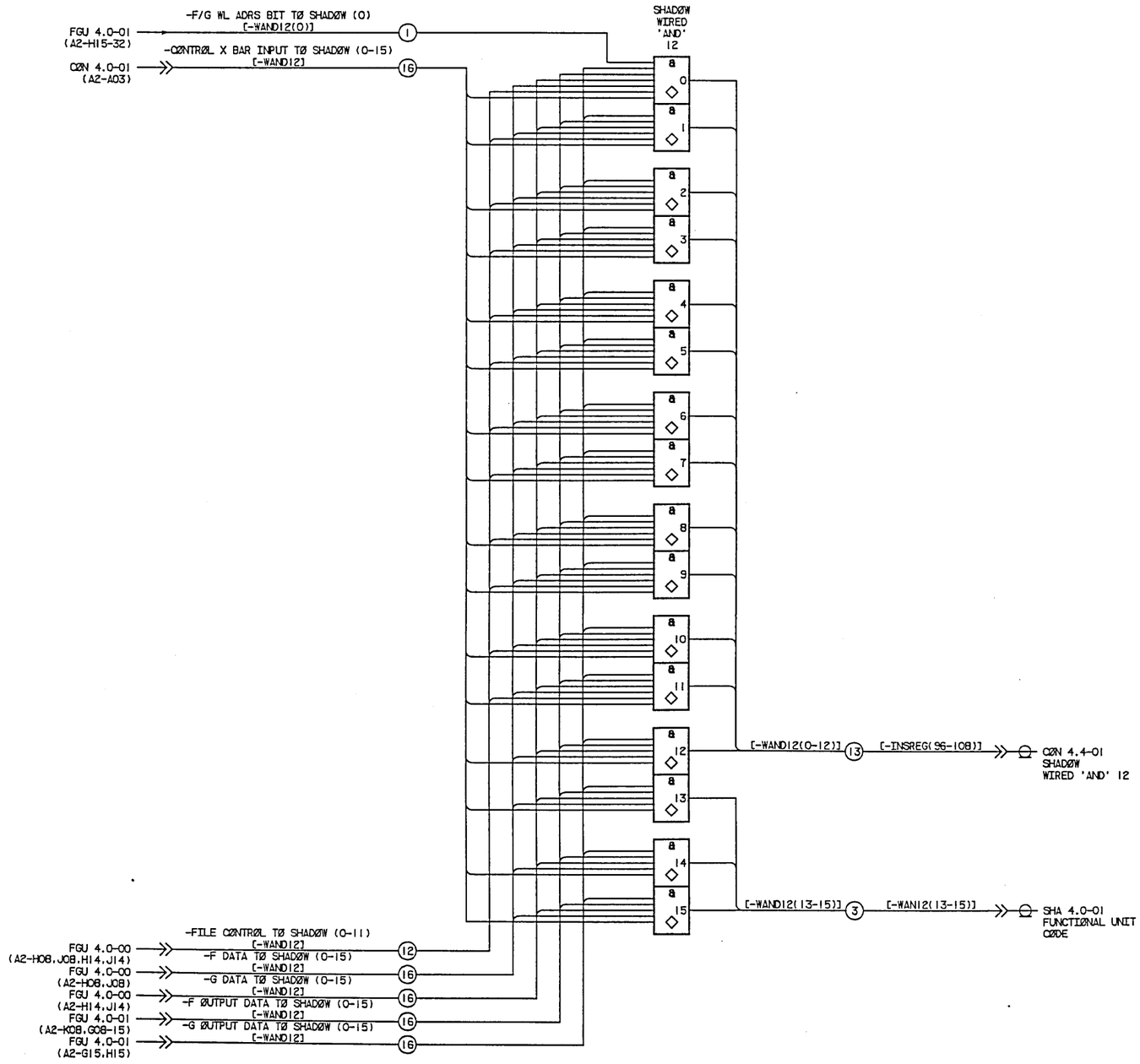
G DATA RGTR

12DB HI4/8B43-B/B -C8 BITS 0-7
12DB JI4/8B44-B/B -C12 BITS 8-15

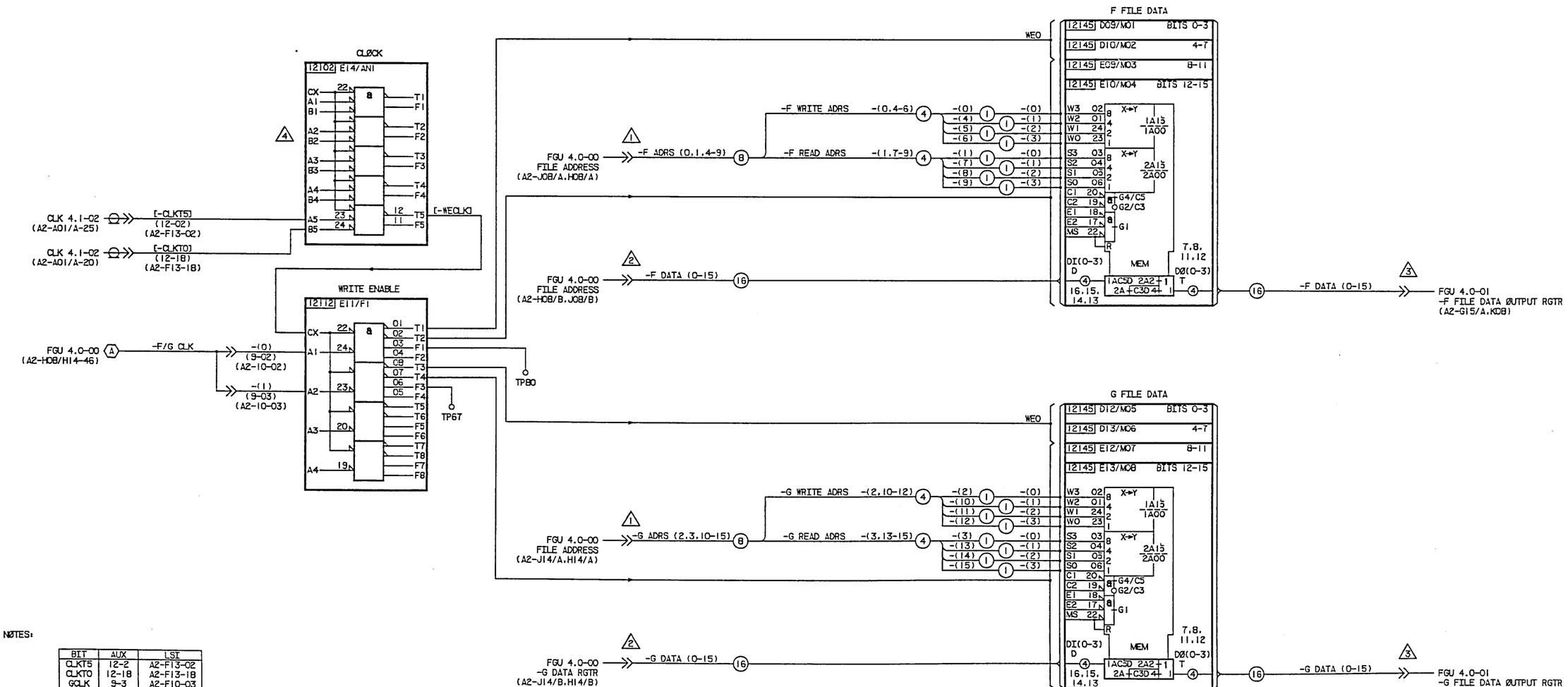
-(0-15) 16 -G DATA → FGU 4.1-00 G FILE DATA (A2/F1-D12→E13)
-(0-15) 16 -G DATA TØ SHADØW [-WAND12] → FGU 4.0-02

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 4 DIAGRAM
FILE ADDRESS/F AND G DATA REGISTERS
DB-A2MUL:A2
CAGE IDENT
DWG NO 60461830
REV A
SHEET FGU 4.0-00
PAGE IV-5-5


F ØUTPUT RGTR
I2DB KCØ/8B45 -C1 BITS 0-11
MASTER SLAVE
FGU 4.1-00 (A2/F1-E10→D09)
-F DATA (0-15)
-(0-15)
CLK 4.1-00 (A2-K15-45)
-C1 [-8B45-C1(TO)]
CØN 4.5-11 (C2/B2-E05-15)
+STØP [-NSTØP(7)]
FGU 4.0-00
-INTERRUPT DØNE [-ITDØNE(7,8)]
SHA 4.0-02 (B2-A09/A-28)
-SHADØW RØW SELECT 4 [-URS4(6)]
CØN 4.3-00 (A2-H10-27)
+INT RGTR 8 [-NINTR(10)]
-(0-3)
-(4-11)
-(0,12-15)
A(0-3) 17,18, 36,37
B(0-7) 16,15, 11,12, 44,38, 41,42
C1 3
ENI 9
XFR 8
GØ1 35
ENS 10
C2 2
EN2 46
GØ2 43
D(0-3) 23,27,30,33
C(0-3) 26,28,31,34
E(0-3) 24,25, 29,32
F(0-7) 22,21,6,4, 4,51,49, 47,45
G(0-7) 19,20,7, 5,1,52, 50,48
-X BAR 9 IN (0-15) [-FØUT(0-15)/XBRI(0-15)(9)]
CØN 4.2-01 DATA X BAR (C2-KØ1-G15)
-F ØUTPUT DATA TØ SHADØW [-WANDI2]
FGU 4.0-02
I2DB G15/8B46-A/B -C5 BITS 12-15
CLK 4.1-00 (A2-K15/B-52)
-C5 [-2B46-C1(TO)]
CØN 4.5-11 (C2/B2-E13-03)
+STØP [-NSTØP(8)]
CØN 4.5-31 (C2/C2-E09-16)
+INT RGTR [-NINTR(29)]
-(12-15)
-(8)
STATUS VECTØR REGISTER
I2DB H15/2B47-A/B BITS 0-3
FGU 4.0-00 FILE ADRS (A2-H14/A-26)
+FICLC [-NFICLC]
-(0-3)
-(3)
CLK 4.1-00 (A2-K15/B-02)
-C9 [-2B47-C1(TO)]
SHA 4.0-03 (B2-A07/B-02)
-SHADØW RØW SELECT 7 [-URS7(6)]
-(8)
-(0,1)
-F STAT G STAT [-FSTAT(0)/CVBO(14)] [-GSTAT(0)/CVBI(14)]
CØN 4.3-00 (C2-G06,G07-21)
-F/G U/L ADRS BIT TØ SHADØW [-WAND12(0)]
-(3)
FGU 4.0-02
G ØUTPUT RGTR
CLK2
I2DB G15/2B46-B/B -C5 BITS 0-7
CI
I2DB H15/2B47-B/B -C9 BITS 8-15
FGU 4.1-00 G FILE DATA (A2/F1-E13)
-G DATA (0-15)
SHA 4.0-02 (B2-A09/B-02)
-SHADØW RØW SELECT 5 [-URS5(6)]
-(0-15)
-X BAR 10 IN (0-15) [-GØUT(0-15)/XBRI(0-15)(10)]
CØN 4.2-01 DATA X BAR (C2-KØ1→G15)
-G ØUTPUT DATA TØ SHADØW [-WAND12]
FGU 4.0-02
-(0)
-(1)
-(2)
MPY 4.0-08
CONTROL DATA CORPORATION
DEVELOPMENT DIVISIØN
LEVEL 4 DIAGRAM
F AND G ØUTPUT REGISTERS
DB-A2MUL:A2
60461830
A
FGU 4.0-01
IV-5-7



CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM REGISTER FILE UNIT SHADØW WIRED 'AND'	CODE IDENT/DWG NO	REV
		60461830	A
DEVELØPMENT DIVISIØN	DB-A2MUL:A2	SHEET FGU 4.0-02	PAGE IV-5-9



NØTES:

BIT	AUX	LSI
CLKT5	12-2	A2-F13-02
CLKTØ	12-18	A2-F13-18
GCLK	9-3	A2-F10-03
FCLK	9-2	A2-F10-02

1

F ADDRESS		
BIT	AUX	LSI
0	6-6	A2-F07-06
1	6-4	A2-F07-04
4	9-22	A2-F10-22
5	9-19	A2-F10-19
6	9-25	A2-F10-25
7	9-26	A2-F10-26
8	9-20	A2-F10-20
9	9-24	A2-F10-24

G ADDRESS		
BIT	AUX	LSI
2	13-24	A2-F14-24
3	13-19	A2-F14-19
10	11-20	A2-F12-20
11	11-22	A2-F12-22
12	11-18	A2-F12-18
13	11-26	A2-F12-26
14	11-24	A2-F12-24
15	10-2	A2-F11-02

2

DATA IN				
BIT	F DATA		G DATA	
	AUX	LSI	AUX	LSI
0	9-18	A2-F10-18	10-8	A2-F11-08
1	9-17	A2-F10-17	10-9	A2-F11-09
2	9-21	A2-F10-21	10-10	A2-F11-10
3	9-16	A2-F10-16	10-5	A2-F11-05
4	9-15	A2-F10-15	11-4	A2-F12-04
5	9-10	A2-F10-10	11-3	A2-F12-03
6	9-9	A2-F10-09	11-2	A2-F12-02
7	9-8	A2-F10-08	11-1	A2-F12-01
8	9-4	A2-F10-04	10-22	A2-F11-22
9	8-1	A2-F09-01	10-19	A2-F11-19
10	8-2	A2-F09-02	10-21	A2-F11-21
11	7-8	A2-F08-08	10-20	A2-F11-20
12	8-8	A2-F09-08	11-17	A2-F12-17
13	8-5	A2-F09-05	11-15	A2-F12-15
14	8-6	A2-F09-06	11-10	A2-F12-10
15	8-3	A2-F09-03	11-8	A2-F12-08

3

DATA ØUT				
BIT	-F DATA		-G DATA	
	AUX	LSI	AUX	LSI
0	7-6	A2-F08-06	10-17	A2-F11-17
1	7-5	A2-F08-05	10-18	A2-F11-18
2	7-1	A2-F08-01	10-15	A2-F11-15
3	7-3	A2-F08-03	10-16	A2-F11-16
4	9-4	A2-F10-04	11-9	A2-F12-09
5	9-5	A2-F10-05	11-7	A2-F12-07
6	9-6	A2-F10-06	11-6	A2-F12-06
7	9-7	A2-F10-07	11-5	A2-F12-05
8	6-1	A2-F07-01	9-1	A2-F10-01
9	6-3	A2-F07-03	10-26	A2-F11-26
10	7-22	A2-F08-22	10-25	A2-F11-25
11	7-18	A2-F08-18	10-24	A2-F11-24
12	7-4	A2-F08-04	11-16	A2-F12-16
13	7-2	A2-F08-02	11-25	A2-F12-25
14	8-22	A2-F09-22	11-21	A2-F12-21
15	8-18	A2-F09-18	11-19	A2-F12-19

4 THIS SECTIØN ØF CHIP SHØWN ØN MUL 4.1-00.

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
F AND G MEMØRY REGISTERS
2A01

DB-A2MFL:A2/F1

CODE IDENT:
DWG NØ: 60461830
REV: A
SHEET: FGU 4.1-00
PAGE: IV-5-11

6. MULTIPLY UNIT (MUL)

SYSTEM FUNCTION

The integer multiply functional unit, which is located in the base processor, performs multiplication and other operations on operands taken from the crossbar and returns the results to the crossbar.

GENERAL DESCRIPTION

The multiplier performs 8- and 16-bit integer multiplications to produce 16- and 32-bit results, respectively. The multiply unit also performs population count, significance count, bit reversal, and pass operations. The multiply unit is segmented to allow new operands to be presented and new results to be obtained each clock cycle. After the load cycle, all operations, except multiplication, take only one clock cycle before the results are available; multiplication takes two. All operations, except byte mulitplication, are on 16-bit operands.

LOCATION

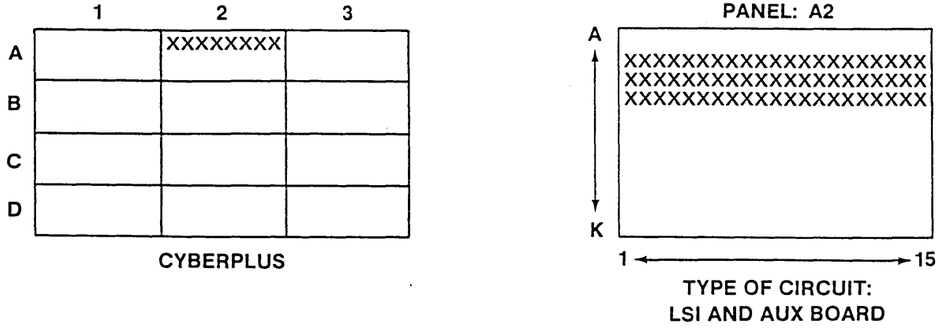


Figure IV-6-1. Location of Multiply Unit Logic Circuits

FUNCTIONAL DESCRIPTION

The discussion in the following paragraphs refers to the simplified block diagram of the multiple unit as shown in figure IV-6-2 and the level 2 diagram MUL 2.0. The control register receives the 12-bit operation code from the 16-bit dynamic control field of the instruction word. The bits of the operation code determine what function the multiplier will perform, and which of the available outputs will be gated to the results register.

The A and B operand registers receive data from the crossbar when enabled by the A and B clocks, respectively. The A and B clocks are set by the program into the clock control field of the instruction word, bits 5 and 6. Bit 5, when set, gates the A multiplicand input, and bit 6, when set, gates the B multiplier input. The clock bits gate the data at time 0 of clock cycle one when they are set. If the clock bits are clear, the contents of the operand registers are not changed. Because of the fanouts required, there are duplicate A and B registers.

Multiplication is done in two stages, each taking a clock cycle. In the first stage, the multiplier network uses the A multiplicand and the B multiplier to form partial sums from partial products, which are held in the intermediate register at the end of the first clock cycle. It is during this first cycle when the operands are considered as 16-bit or 8-bit integers for whole or half word operations.

At the start of the next cycle, the partial sums being held in the intermediate register are input to the adder network to form the final product. The multiplication is done either in 2's complement mode or in the magnitude mode. In 2's complement mode, the multiplier generates a signed 32-bit product from two signed 16-bit integers. In magnitude mode, the multiplier generates either one positive 32-bit product or two, independent, positive 16-bit products. (Half words are always considered positive.)

During the clock cycle one, the population count, bit reversal, and significance count functions are performed by the multiply unit. The population count is a binary count of the logical 1 bits in either input register. A separate count of both registers (A and B) is performed and can be separately available each clock cycle.

The bit reversal function is performed on the contents of the A input register each clock cycle. Bit reversal is achieved by wiring bit 15 of the input register to the bit 0 position in the output selector, bit 14 to bit 1, and so forth, until all the bits have a reversed position.

The significance count is a binary number indicating the bit position of the most significant digit in the B input register, starting with the LSB position (bit 15) equal to 0. It is performed each clock cycle.

Two compare registers, compare upper and compare lower, are loaded directly from crossbar outputs, XA and XB, respectively. This occurs only when a compare function is loaded into the control register. The XA and XB contents are compared to the multiply results in the upper and lower output registers, respectively, every clock cycle after the initial register values are available for comparison. The resulting status bits become condition vectors.

The upper (U) and lower (L) output selectors gate the appropriate data to the U and L output registers, comparators, and in the case of the MSBs, to the status register. Once the data is in the output registers it is available to the crossbar input lines. The upper output register receives data from the A input register (pass operation), A input population count, A input bit reversal, or the upper 16 bits of the multiply result. The lower output register receives data from the B input register (pass operation), B input population count, significance count, or the lower 16 bits of the multiply result.

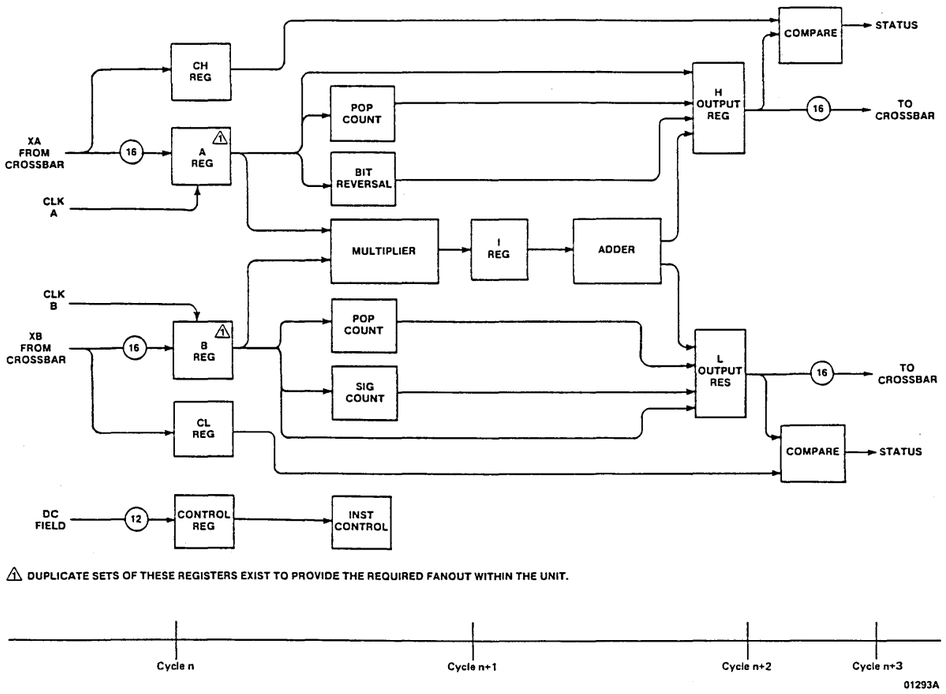


Figure IV-6-2. Multiply Unit Block Diagram

TIMING

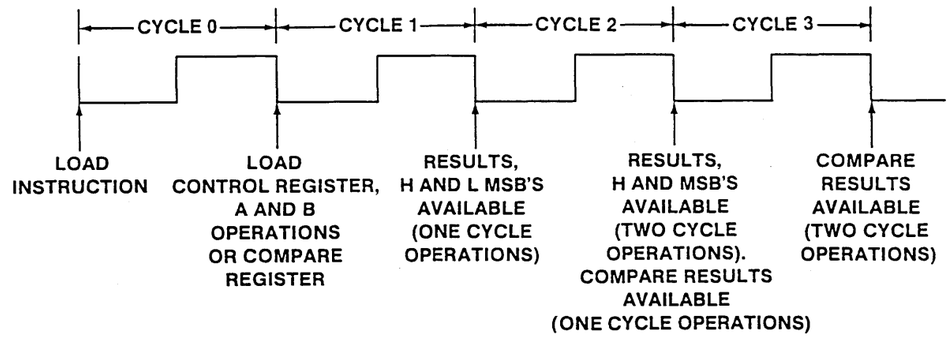

CYCLE 0
CYCLE 1
CYCLE 2
CYCLE 3
LOAD INSTRUCTION
LOAD CONTROL REGISTER, A AND B OPERATIONS OR COMPARE REGISTER
RESULTS, H AND L MSB'S AVAILABLE (ONE CYCLE OPERATIONS)
RESULTS, H AND MSB'S AVAILABLE (TWO CYCLE OPERATIONS). COMPARE RESULTS AVAILABLE (ONE CYCLE OPERATIONS)
COMPARE RESULTS AVAILABLE (TWO CYCLE OPERATIONS)

Figure IV-6-3. Multiply Unit Instructions Timing

CØMPARE UPPER
E08 E10
E09 E11
MUL 4.0-08

A RGTR
E10
E11
MUL 4.0-07

A ØPERAND
E04
E09
MUL 4.0-00

PØP CØUNT A
E12
E13
2A01
MUL 4.0-07
MUL 4.1-00

MULTIPLIER
MUL 4.0-00
MUL 4.0-01
MUL 4.0-03
MUL 4.0-04
MUL 4.0-05
MUL 4.1-00

UPPER INTERMEDIATE PRØDUCT RGTR
MUL 4.0-06

LØWER INTERMEDIATE PRØDUCT RGTR
MUL 4.0-06

INTERMEDIATE PRØDUCT ADDERS
MUL 4.0-06

PØP CØUNT B
E02
E01
MUL 4.0-07

2A01
MUL 4.1-00

SIGNIFICANCE CØUNT
E06
MUL 4.0-07

B ØPERAND
E08
E07
MUL 4.0-00

B RGTR
D02
D01
MUL 4.0-07

CØMPARE LØWER
A04 E04
D02
MUL 4.0-08

CØNTRØL RGTR
E05.E07.A06
MUL 4.0-07

A14
UPPER ØUTPUT SELECTØR
D13
MUL 4.0-08

A15
UPPER ØUTPUT RGTR
E15

A05
LØWER ØUTPUT SELECTØR
E03
MUL 4.0-08

A06
LØWER ØUTPUT RGTR
E05

CØMPARATØR UPPER
D15
D14
MUL 4.0-08

CØMPARATØR LØWER
B15
E14
MUL 4.0-08

CØMPARE STATUS
2A01
MUL 4.1-00

A15
STATUS RGTR
E15
MUL 4.0-08

PART ØF SHADØW WIRED 'AND' 13
MUL 2.0

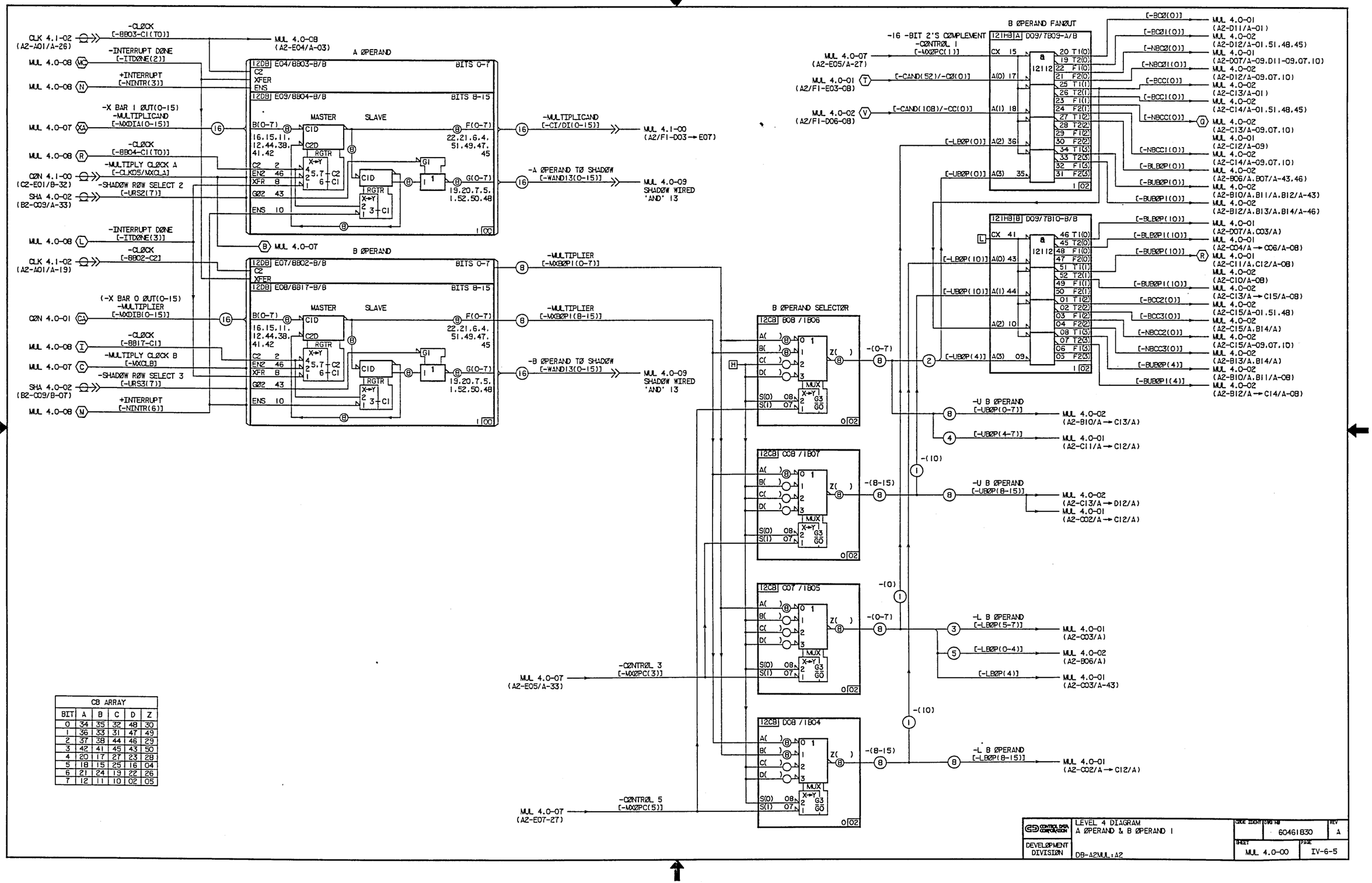
PART ØF SHADØW WIRED 'AND' 20
MUL 2.0

PART ØF SHADØW WIRED 'AND' 20
MUL 2.0

PART ØF SHADØW WIRED 'AND' 13
MUL 2.0

NØTE:
1. SHADØW RGTR AND WIRED 'AND' DUPLICATED ØN SHA 2.0.

CONTROL DATA CORPORATION	LEVEL 2 DIAGRAM A2 MULTIPLY UNIT	CODE IDENT	DWG NO 60461830 REV A
DEVELOPMENT DIVISIØN		SHEET MUL 2.0	PAGE IV-6-3



CB ARRAY					
BIT	A	B	C	D	Z
0	34	35	32	48	30
1	36	33	31	47	49
2	37	38	44	46	29
3	42	41	45	43	50
4	20	17	27	23	28
5	18	15	25	16	04
6	21	24	19	22	26
7	12	11	10	02	05

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM A ØPERAND & B ØPERAND 1	CODE IDENT	DWG NO 60461830
DEVELØPMENT DIVISIØN	DB-A2MUL:A2	SHEET MUL 4.0-00	PAGE IV-6-5
			REV A

MULTIPLE FØRMATIØN (0-38)

12SB	CC2/9B01-A/B	IN:CAND(0-7) PLIER(0-6)	BITS 0-2
12SB	D03/9B02-A/B	CAND(8-15) PLIER(7-13)	3-5
12SB	D04/9B03-A/B	CAND(16-23) PLIER(14-20)	6-8
12SB	D05/9B04-A/B	CAND(24-31) PLIER(21-27)	9-11
12SB	D06/9B05-A/B	CAND(32-39) PLIER(28-34)	12-14
12SB	D07/9B06-A/B	CAND(40-47) PLIER(35-41)	15-17
12SB	D11/9B07-A/B	CAND(48-55) PLIER(42-48)	18-20
12SB	C03/9B08-A/B	CAND(56-63) PLIER(49-55)	21-23
12SB	C04/9B09-A/B	CAND(64-71) PLIER(56-62)	24-26
12SB	C05/9B10-A/B	CAND(72-79) PLIER(63-69)	27-29
12SB	C06/9B11-A/B	CAND(80-87) PLIER(70-76)	30-32
12SB	C11/9B12-A/B	CAND(88-95) PLIER(77-83)	33-35
12SB	C12/9B13-A/B	CAND(96-103)	BITS 36-38

NØTE: ⚠ M AND P BITS ARE NØT TRUE VIRTUAL NAMES.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM MULTIPLY FØRMATIØN	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISION	DB-A2MUL:A2	SHEET MUL 4.0-01	PAGE IV-6-7

MUL 4.0-00 (A2-D09/A-23) Q +B ØPERAND [-NBCC(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/A-25) -B ØPERAND [-BCC(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/A-24) +B ØPERAND [-NBCC1(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/A-26) -B ØPERAND [-BCC1(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/B-03) +B ØPERAND [-NBCC2(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/B-01) -B ØPERAND [-BCC2(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/B-02) -B ØPERAND [-BCC3(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/B-04) +B ØPERAND [-NBCC3(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/A-21) +B ØPERAND [-NBCØI(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/A-19) -B ØPERAND [-BCØI(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-B08) -UB ØPERAND [-UBØP(0-7)] 8 [-UBØP(4-7)] 4
MUL 4.0-00 (A2-C08) -UB ØPERAND [-UBØP(8-15)] 8 [-UBØP(8-9)] 2
MUL 4.0-00 (A2-D09/B-52) -UB ØPERAND [-BUBØPI(10)] 1
MUL 4.0-00 (A2-D09/B-51) R -UB ØPERAND [-BUBØP(10)] 1
MUL 4.0-00 (A2-D09/A-27) -LB ØPERAND [-BLBØP(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-C07) -LB ØPERAND [-LBØP(0-4)] 5
MUL 4.0-00 (A2-D09/A-34) -UB ØPERAND [-BUBØP(0)] 1 -(0) EXTEND
[-UBØP(0-3)] 4
MUL 4.0-00 (A2-D09/B-08) -UB ØPERAND [-BUBØP(4)] 1
MUL 4.0-00 (A2-D09/A-33) -UB ØPERAND [-BUBØPI(0)] 1 -(0) EXTEND
MUL 4.0-00 (A2-D09/B-07) -UB ØPERAND [-BUBØPI(4)] 1
[-UBØP(10-15)] 6
MUL 4.1-00 (A2/FI-D03→ EOT) -MULTIPLICAND [-CAND(104-199)]
[-CAND(108)/-CC(0)] V MUL 4.0-00 (A2-D09/A-18)

-(104-106) -(0) -(107) -(108-111) -(112-114) -(115-118) -(119) -(120-122) -(123-125) -(126-127) -(128-130) -(131-135) -(136-137) -(138) L H -(139-143) -(144-146) -(147-148) H -(149-151) -(152-154) -(155-159) -(160-162) -(163-167) -(168-170) -(171-173) -(174-175) -(176) -(177-178) -(179-183) -(184-186) -(0) -(187) -(188-191) -(192-194) -(195-198) -(199) -CAND(104-199) 36

-(4-7) -(8-9) -(10) -(4-7) -(8-9) -(10) -(4-7) -(8-9) -(10) -(4-7) -(8-9) -(10) -(4-7) -(8-9) -(10) -(0-4) -(0-4) -(0-4) -(0-3) -(4) -(0-3) -(4) -(0-3) -(4) -(0-3) -(4) -(0-3) -(4) -(10-15) 6 H
-(91-94) -(95-96) -(97) -(98-101) -(102-103) -(104) -(105-108) -(109-110) -(111) -(112-115) -(116-117) -(118) -(119-120) -(121-125) -(126-127) -(128-132) -(133-134) -(135-138) -(139) -(140-141) -(142-145) -(146) -(147) -(148) -(149-152) -(153) -(154-155) -(156-159) -(160) -(161-162) -(163-166) -(167) -(168-173) -(174)
-PLIER(91-174) 36

MULTIPLE FØRMATIØN (39-74)

12SB C13/9B14-A/B	IN:CAND(104-111) PLIER(91-97)	BITS 39-41
12SB C14/9B15-A/B	CAND(112-119) PLIER(98-104)	42-44
12SB C15/9B16-A/B	CAND(120-127) PLIER(105-111)	45-47
12SB C10/9B17-A/B	CAND(128-135) PLIER(112-118)	48-50
12SB B06/9B18-A/B	CAND(136-143) PLIER(119-125)	51-53
12SB B07/9B19-A/B	CAND(144-151) PLIER(126-132)	54-56
12SB B10/9B20-A/B	CAND(152-159) PLIER(133-139)	57-59
12SB B11/9B21-A/B	CAND(160-167) PLIER(140-146)	60-62
12SB B12/9B22-A/B	CAND(168-175) PLIER(147-153)	63-65
12SB B13/9B23-A/B	CAND(176-183) PLIER(154-160)	66-68
12SB B14/9B24-A/B	CAND(184-191) PLIER(161-167)	69-71
12SB D12/9B25-A/B	CAND(192-199) IN:PLIER(168-174)	BITS 72-74

09.07, 10.01.51, 48.45.44 B M(3-7) 5 B
43.46.15.03 06.12.08 7 P(0-6)
SIGN 11
22-20 47 G7
25-20 37 G8
+M(0-2) 3 1
M(0-2) M(1-3) M(2) M(3) M(3,4) M(4,5) M(4,5) M(5,6) M(6) M(7)
11 12 21 22 21 22 31 32 31 32
1 1 1 3 3 5 5 1 1 1 1 1 1 1
1 2 4 7.4 7.6 8.6
P(0) P(1) P(2) P(3) P(4) P(5) P(6) P(0) P(2) P(4)
8 8 8 8 4 4 4 4
G32 G31 G22 G21 G12 G11 G6 G5 G4 G3 G2 G1
A1,A2,A3 3
B1, B2, B3 3 B1
B3,B4 2 B3,B4
C1, C2, C3 3 C1,C2
C3
9
A1, B1, C1 3 A2, B2, C2 3 A3, B3, C3 3
≥2 2K+1 ≥2 2K+1 ≥2 2K+1
+MPC 3 05, 52.49
MPS 3 04, 02.50
0 06

NØTE: ⚠ M AND P BITS ARE NØT TRUE VIRTUAL NAMES.

+MPC(39-44) [+9B14NMPC(39-44)] 6 → MUL 4.0-04 (A2-C14/B.C13/B)
+MPC(46-47) [+9B16NMPC(46-47)] 2 → MUL 4.0-04 (A2-C15/B-41,19)
+MPC(48-49) [+9B17NMPC(48-49)] 2 → MUL 4.0-05 (A2-B09-36,12)
+MPC(51-53) [+9B18NMPC(51-53)] 3 → MUL 4.0-04 (A2-B07/B-36,34,29)
+MPC(54-55) [+9B19NMPC(54-55)] 2 → MUL 4.0-05 (A2-B09,C09-31,27)
+MPC(59) [+9B20NMPC(59)] 1 → MUL 4.0-05 (A2-B09-34)
+MPC (72) [+9B25NMPC(72)/-PP] 1 → MUL 4.1-00 (A2/FI-E14-01,03,17)
+MPC(73-74) [+9B25NMPC(73-74)] 2 → MUL 4.0-05 (A2-D12/B-41,19)
+MPC(55-68) [+9BXXNMPC(55-68)] 14 → MUL 4.0-04 (A2-C12/B→ C14/B,C15/B→ B10/B)
+MPC 36

-MPS(48-49) [-9B17MPS(48-49)] 2 → MUL 4.0-05 (A2-B09-37,20)
-MPS(54) [-9B19MPS(54)] 1 → MUL 4.0-05 (A2-B09-44)
-MPS(59) [-9B20MPS(59)] 1 → MUL 4.0-05 (A2-B09-42)
-MPS (72) [-9B25MPS(72)/-PS] 1 → MUL 4.1-00 (A2/FI-E14-19)
-MPS(72-74) [-9B25MPS(72-74)] 3 → MUL 4.0-05 (A2-D12/B-16,18,33)
-MPS(39-49,51-71) [-9BXXMPS(39-49,51-71)] 32 → MUL 4.0-04 PARTIAL ADDER (30-59) (A2-C06/B→ C14/B,C15/B→ B10/B)
-MPS 36

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM MULTIPLE FØRMATIØN	DRAWING NUMBER 60461830	REV A
DEVELØPMENT DIVISIØN	DB-A2MUL:A2	SHEET MUL 4.0-02	PAGE IV-6-9

PARTIAL ADDER (15-29)

12SB DO7/9B06-B/B IN: 20-23 ØUT: 15-17
12SB D11/9B07-B/B IN: 24-27 ØUT: 18-20
12SB C03/9B08-B/B IN: 28-31 ØUT: 21-23
12SB C04/9B09-B/B IN: 32-35 ØUT: 24-26
12SB C05/9B10-B/B IN: 36-39 ØUT: 27-29

20.22.
32.29 +A3 +A3
23.17. +A0 +A1
35.38 C3 C3
41.19. CO CI
36.34 +B3 +B3
16.18. +BO +BI
33.42 D3 D3
DO DI
+A3
+A1
C3
CI
+B3
+BI
D3
DI
+A2
+AO
C2
CO
+B2
+BO
D2
DO
2K+1
≥2
a 1
a
PS3 PSI APS
+PC3 +PCI +APC
27, 24,31
25, 21,30
1 03

PARTIAL ADDER (0-14)

12SB CO2/9B01-B/B IN: 0-3 ØUT: 0-2
12SB DO3/9B02-B/B IN: 4-7 ØUT: 3-5
12SB DO4/9B03-B/B IN: 8-11 ØUT: 6-8
12SB DO5/9B04-B/B IN: 12-15 ØUT: 9-11
12SB DO6/9B05-B/B IN: 16-19 ØUT: 12-14

20.22.
32.29 +A3 +A3
23.17. +AO +A1
35.38 C3 C3
41.19. CO CI
36.34 +B3 +B3
16.18. +BO +BI
33.42 D3 D3
DO DI
+A3
+A1
C3
CI
+B3
+BI
D3
DI
+A2
+AO
C2
CO
+B2
+BO
D2
DO
2K+1
≥2
a 1
a
PS3 PSI APS
+PC3 +PCI +APC
27, 24,31
25, 21,30
1 03

MUL 4.0-04 (A2-B06/B-27)
+PC (52) [-9B18NPC(52)]
(A2-C04/B-27.24)
+PC (24-25) [-9B09NPC(24-25)]
(A2-D06/B-25.21.30)
(A2-D06/B-24.31)
MUL 4.0-05 (A2-D10)
[-1B01Z(0-5)]
MUL 4.0-04 (A2-B06/B-25.21)
-PS (51-52) [-9B18PS(51-52)]
MUL 4.0-01 (A2-C02/A→C12/A) (+MPC)
+MPC (0-35) [-9BXXNMPC(0-35)]
MUL 4.0-01 (A2-C02/A→C12/A) (MPS)
-MPS (0-35) [-9BXXMPS(0-35)]
(A2-C05/B-32.29)
-PC(24,25) [-9B09NPC(24,25)]
-(21-22,24-26)
-(24)
-(25)
(A2-C05/B-23.17.35)
(A2-C05/B-41.19)

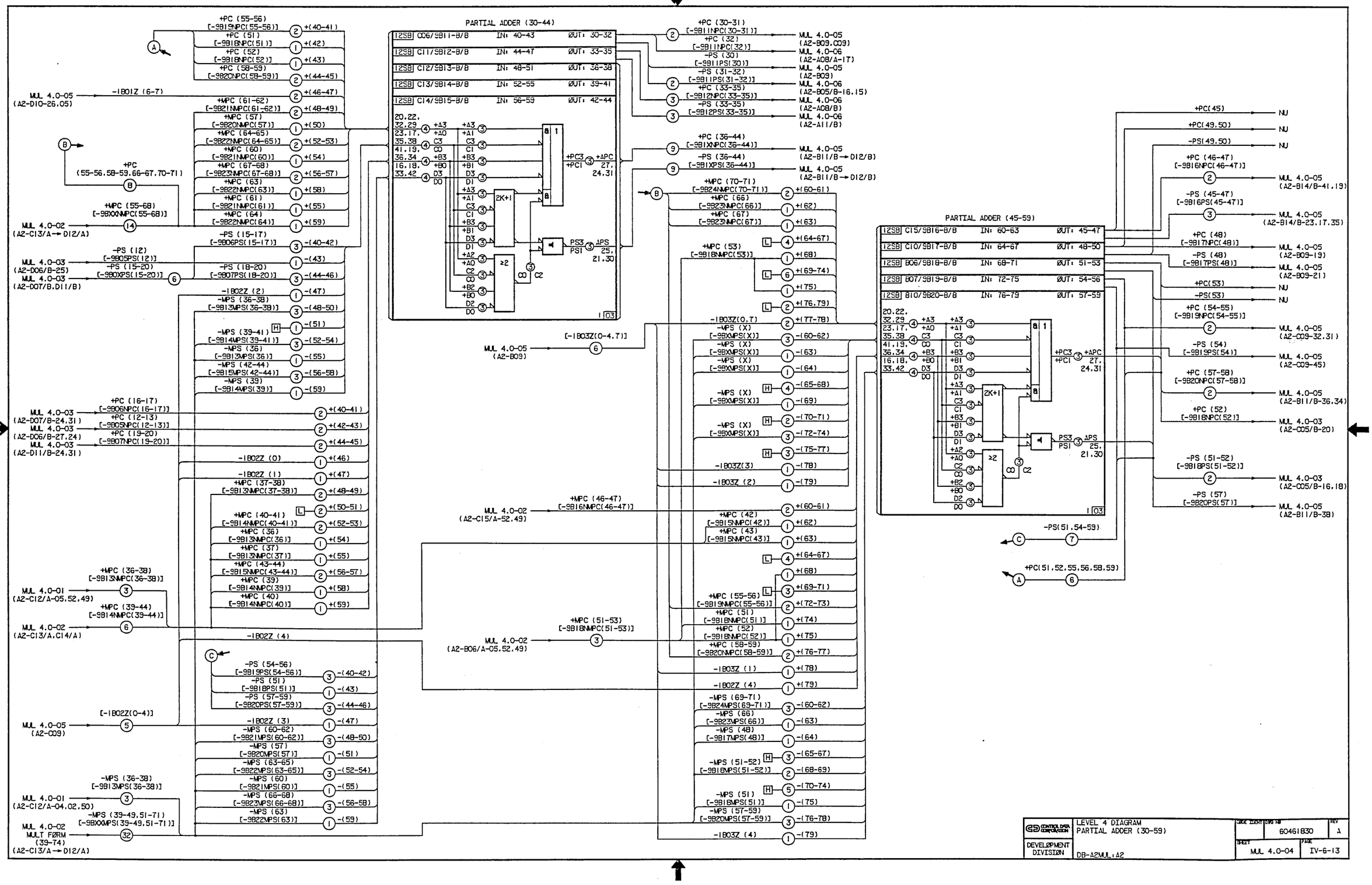
+MPC (31-32) [-9B11NMPC(31-32)] +(20-21)
+MPC (27-28) [-9B10NMPC(27-28)] +(22-23)
+MPC (34-35) [-9B12NMPC(34-35)] +(24-25)
-1B01Z (0) -(26)
-1B01Z (1) -(27)
+MPC (23) [-9B08NMPC(23)] +(28.35)
+(29-34.37)
+(36)
+(38-39)
-MPS (15-17) [-9B06MPS(15-17)] -(20-22)
-MPS (12) [-9B05MPS(12)] -(23)
-MPS (18-20) [-9B07MPS(18-20)] -(24-26)
-1B01Z (4) -(27)
-(28.30.31.35)
-MPS (23) [-9B08MPS(23)] -(29)
-MPS (24-26) [-9B09MPS(24-26)] -(32.34)
-PS (12-14) [-9B05PS(12-14)] -(36-38)
-MPS (9) [-9B04MPS(9)] -(39)
+MPC (16-17) [-9B06NMPC(16-17)] +(20-21)
+MPC (12) [-9B05NMPC(12)] +(22)
+MPC (19-20) [-9B07NMPC(19-20)] +(24-25)
-1B01Z (2) -(26)
-1B01Z (3) -(27)
+MPC (22) [-9B08NMPC(22)] +(28.35)
+(29-31)
+MPC (25-26) [-9B09NMPC(25-26)] +(32-33)
+MPC (21) [-9B08NMPC(21)] +(+(34)
+PC (13-14) [-9B05NPC(13-14)] +(36-37)
+MPC (9-10) [-9B04NMPC(9-10)] +(38-39)
-MPS (30-32) [-9B11MPS(30-32)] -(20-22)
-MPS (27) [-9B10MPS(27)] -(23)
-MPS (33-35) [-9B12MPS(33-35)] -(24-26)
-1B01Z (5) -(27)
-MPS (21-22) [-9B08MPS(21-22)] -(28-29)
-MPS (21) [-9B06MPS(21)] -(30-34.38)
-(35)
-(36-37)
-PS (24) [-9B09PS(24)] -(39)

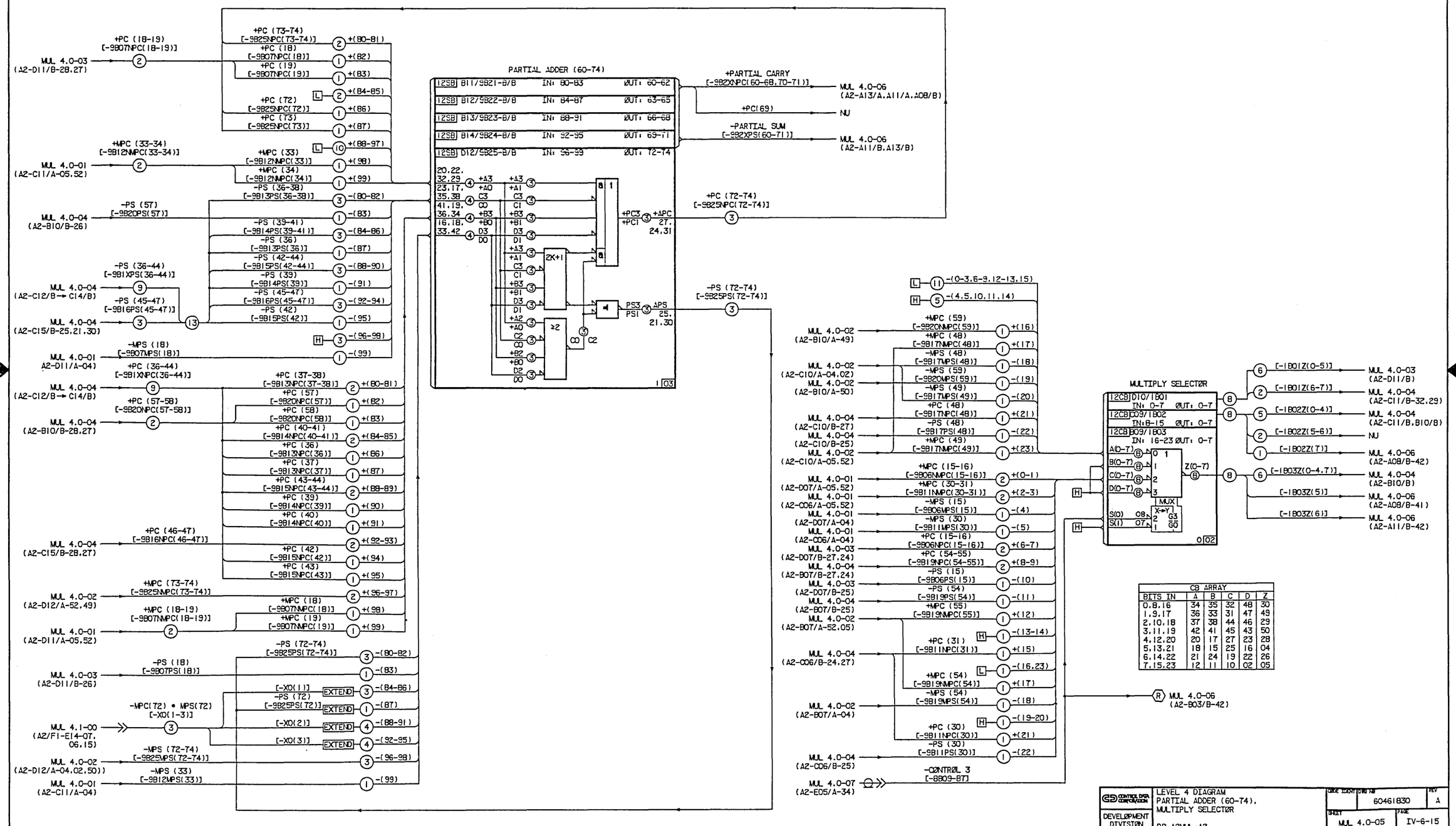
+PC (15-16) [-9B06NPC(15-16)] MUL 4.0-05 (A2-D10-19.10)
+PC (16-17) [-9B06NPC(16-17)] MUL 4.0-04 (A2-C06/B-41.19)
+PC (18-19) [-9B07NPC(18-19)] MUL 4.0-05 (A2-B11/B-32.39)
+PC (19-20) [-9B07NPC(19-20)] MUL 4.0-04 (A2-C11/B-41.19)
-PS (15-20) [-9B0XPS(15-20)] MUL 4.0-04 (A2-C06/B.C11/B)
-PS (15) [-9B06PS(15)] MUL 4.0-05 (A2-C09-44)
-PS (18) [-9B07PS(18)] MUL 4.0-05 (A2-B11/B-42)
+PC (27-29) [-9B10NPC(27-29)] MUL 4.0-06 (A2-A08/A-18.36.37)
-PS (27-29) [-9B10PS(27-29)] MUL 4.0-06 (A2-B05/B-11.12.44)

+MPC (2) [-9B01NMPC(2)] +(0)
+(1-6)
+(7)
+PC (21-22,25-26) [-9B0XNPC(21-22,25-26)] +(8)
+(9-11)
+(12-13)
+(14)
+(15)
+(16-17)
+(18-19)
-(0.2-3)
-MPS (2) [-9B01MPS(2)] -(1)
-MPS (3-5) [-9B02MPS(3-5)] -(4-6)
-MPS (0) [-9B01MPS(0)] -(7)
-MPS (6-8) [-9B03MPS(6-8)] -(8-10)
-MPS (3) [-9B02MPS(3)] -(11)
-MPS (9-11) [-9B04MPS(9-11)] -(12-14)
-MPS (6) [-9B03MPS(6)] -(15)
-MPS (12-14) [-9B05MPS(12-14)] -(16-18)
-MPS (24) [-9B09MPS(24)] -(19)
+MPC (1) [-9B01NMPC(1)] +(0)
+(1-3)
+MPC (4-5) [-9B02NMPC(4-5)] +(4-5)
+MPC (0) [-9B01NMPC(0)] +(6)
+MPC (1) [-9B01NMPC(1)] +(7)
+MPC (7-8) [-9B03NMPC(7-8)] +(8-9)
+MPC (3) [-9B02NMPC(3)] +(10)
+MPC (4) [-9B02NMPC(4)] +(11)
+MPC (10-11) [-9B04NMPC(10-11)] +(12-13)
+MPC (6) [-9B03NMPC(6)] +(14)
+MPC (7) [-9B03NMPC(7)] +(15)
+MPC (13-14) [-9B05NMPC(13-14)] +(16-17)
+MPC (24) [-9B09NMPC(24)] +(18)
+MPC (25) [-9B09NMPC(25)] +(19)
-MPS (0-1) [-9B01MPS(0-1)] -(0-1)
-(2-7. 10-11.19)
-PS (21-22) [-9B08PS(21-22)] -(8-9)
-PS (24-26) [-9B09PS(24-26)] -(12-14)
-PS (21) [-9B08PS(21)] -(15)
-MPS (27-29) [-9B10MPS(27-29)] -(16-18)

-PC (0-1,3-11) [-9B0XNPC(0-1,3-11)] MUL 4.0-06 (A2-B05/A→B03/B)
-(2) NU
-PS (0-1,3-11) [-9B0XPS(0-1,3-11)] MUL 4.0-06 (A2-B05/B→A04/A)
-(2) NU
+PC (12-13) [-9B05NPC(12-13)] MUL 4.0-04 (A2-C06/B-36.34)
-(14)
-(13)
-PS (12) [-9B05PS(12)] MUL 4.0-04 (A2-C06/B-38)
-PS (12-14) [-9B05PS(12-14)]
+PC (13-14) [-9B05NPC(13-14)]

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM PARTIAL ADDER (0-29)	CODE IDENT	DWG NO 60461830 REV A
DEVELOPMENT DIVISION	DB-A2MUL:A2	SHEET MUL 4.0-03	PAGE IV-6-11


PARTIAL ADDER (30-44)
PARTIAL ADDER (45-59)
LEVEL 4 DIAGRAM
PARTIAL ADDER (30-59)
DEVELOPMENT DIVISION
DB-A2MUL:A2
60461830
A
MUL 4.0-04
IV-6-13


PARTIAL ADDER (60-74)
12SB B11/SB21-B/B IN: 80-83 ØUT: 60-62
12SB B12/SB22-B/B IN: 84-87 ØUT: 63-65
12SB B13/SB23-B/B IN: 88-91 ØUT: 66-68
12SB B14/SB24-B/B IN: 92-95 ØUT: 69-71
12SB D12/SB25-B/B IN: 96-99 ØUT: 72-74
+PARTIAL CARRY [-9820XNPC(60-68,70-71)]
+PC(69)
-PARTIAL SUM [-992XPS(60-71)]
MUL 4.0-06 (A2-A13/A.A11/A.A08/B)
NU
MUL 4.0-06 (A2-A11/B.A13/B)
+PC (72-74) [-9825NPC(72-74)]
-PS (72-74) [-9825PS(72-74)]
2K+1
MULTIPLY SELECTOR
MUX
CB ARRAY
BITS IN | A | B | C | D | Z
0,8,16 | 34 | 35 | 32 | 48 | 30
1,9,17 | 36 | 33 | 31 | 47 | 49
2,10,18 | 37 | 38 | 44 | 46 | 29
3,11,19 | 42 | 41 | 45 | 43 | 50
4,12,20 | 20 | 17 | 27 | 23 | 28
5,13,21 | 18 | 15 | 25 | 16 | 04
6,14,22 | 21 | 24 | 19 | 22 | 26
7,15,23 | 12 | 11 | 10 | 02 | 05
LEVEL 4 DIAGRAM
PARTIAL ADDER (60-74), MULTIPLY SELECTOR
DEVELOPMENT DIVISION
D8-A2MUL:A2
60461830
A
MUL 4.0-05
IV-6-15

PARTIAL CARRY LOWER

PARTIAL SUM LOWER

PARTIAL SUM UPPER

PARTIAL CARRY UPPER

MULTIPLY ADDER UPPER

MULTIPLY ADDER LOWER

CARRY

SA ARRAY				
BIT	A	B	C	SUM
0	05	09	07	26
1	08	04	02	25
2	15	16	20	23
3	12	11	33	24
4	38	35	37	30
5	42	41	44	29
6	45	43	46	31
7	48	47	52	32

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
INTERMEDIATE AND MULTIPLY ADDER

DB-A2MUL:A2

SIZE: E | DWG NO: 60461830 | REV: A
SHEET: MUL 4.0-06 | PAGE: IV-6-17

A RGTR

B RGTR

CØNTRØL

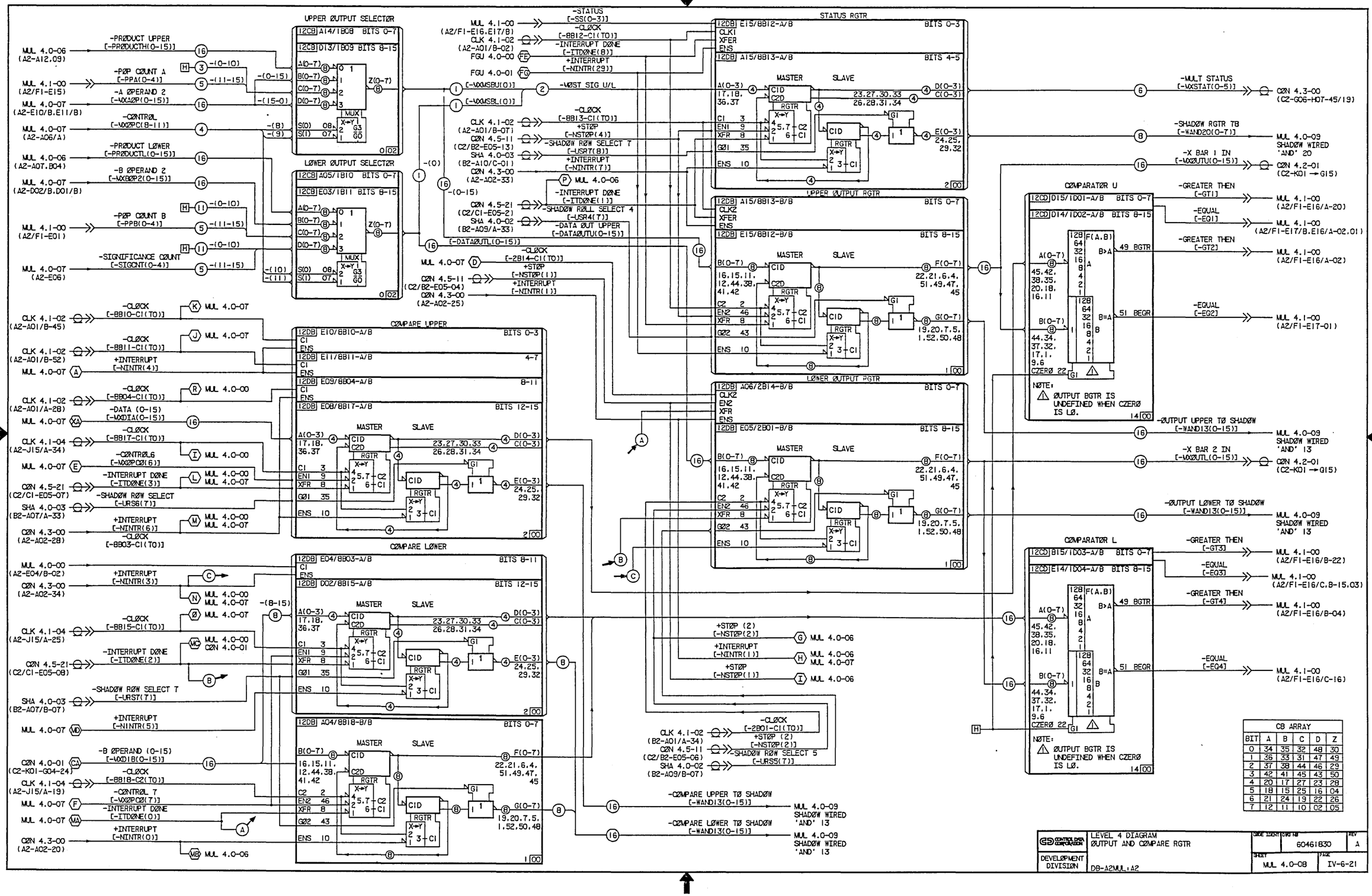
SU ARRAY

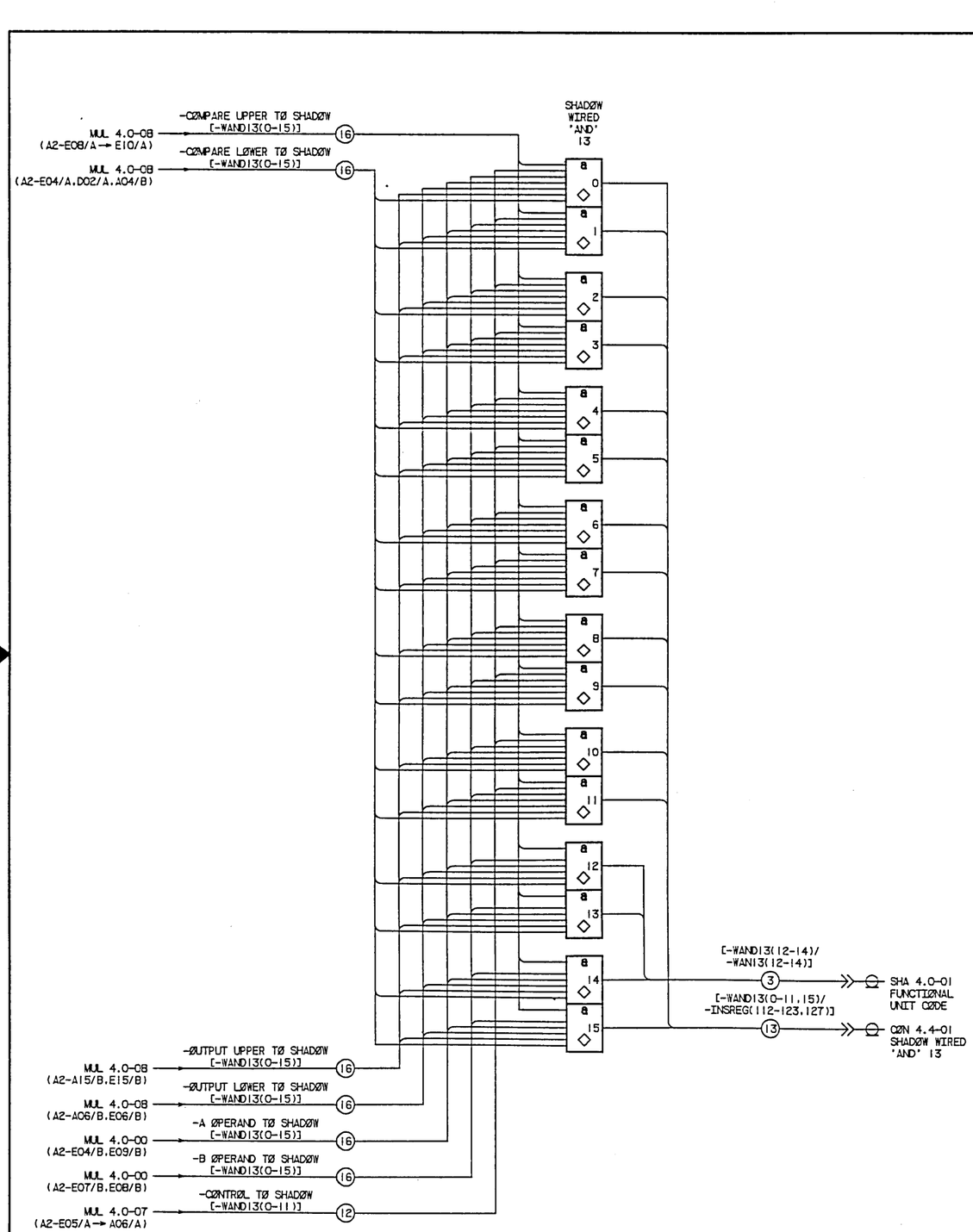
BIT	Z
0	15
1	16
2	11
3	12
4	09
5	02
6	37
7	38

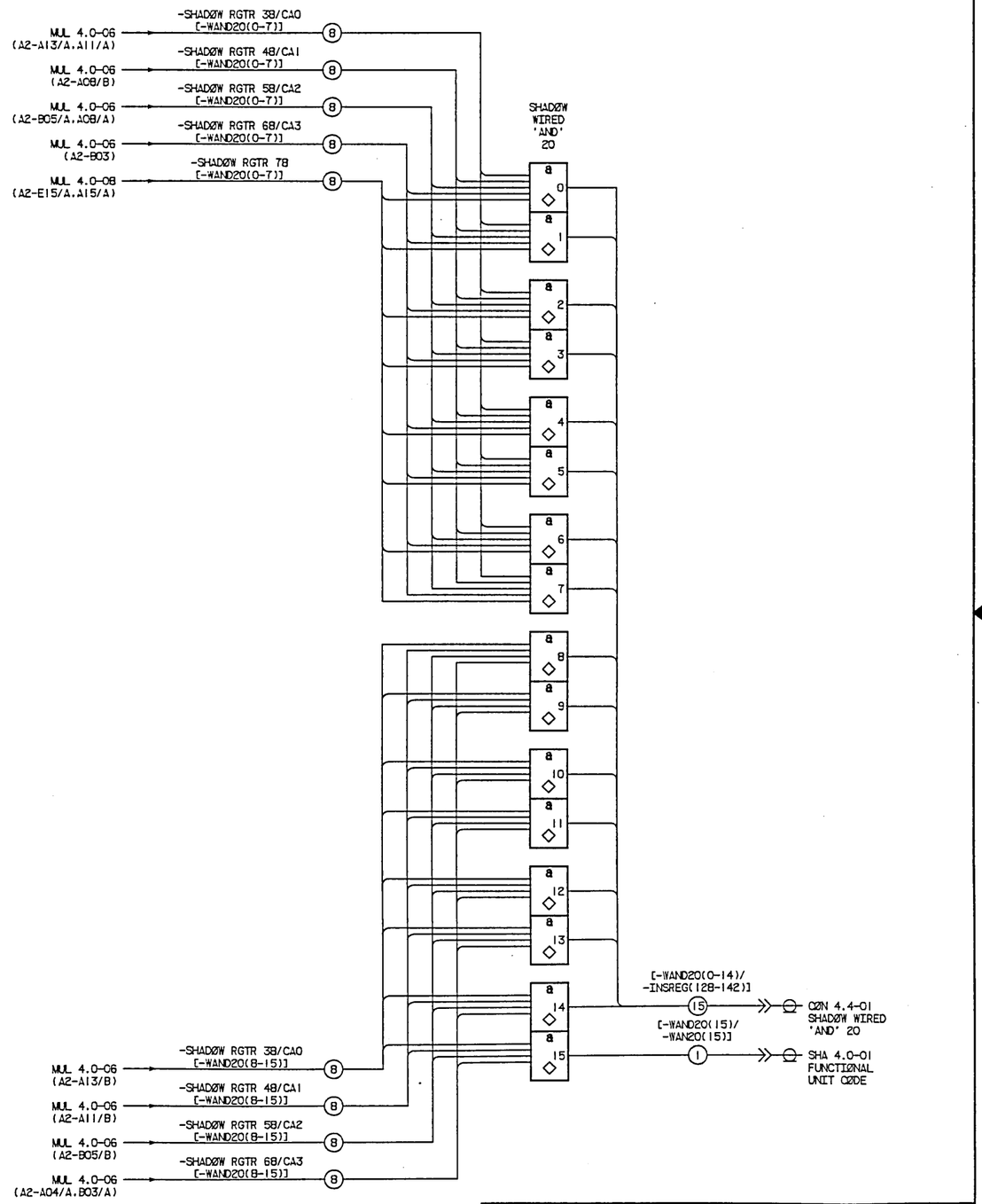
SD SIGNIFICANCE CØUNT

INPUT	PINS	INPUT	PINS
MXBØP2(0)	34	MXBØP2(8)	10
MXBØP2(1)	35	MXBØP2(9)	9
MXBØP2(2)	37	MXBØP2(10)	7,8
MXBØP2(3)	42	MXBØP2(11)	44
MXBØP2(4)	46	MXBØP2(12)	32,36
MXBØP2(5)	45	MXBØP2(13)	38,41
MXBØP2(6)	19,20	MXBØP2(14)	43,48
MXBØP2(7)	11,17	MXBØP2(15)	51

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM INPUT REGISTER	DRAWING NO	60461830 REV A
DEVELOPMENT DIVISION	DB-A2MUL:A2	SHEET	MUL 4.0-07 PAGE IV-6-19


UPPER ØUTPUT SELECTØR
LØWER ØUTPUT SELECTØR
STATUS RGTR
UPPER ØUTPUT RGTR
LØWER ØUTPUT RGTR
CØMPARE UPPER
CØMPARE LØWER
CØMPARATØR U
CØMPARATØR L
MASTER
SLAVE
-PRØDUCT UPPER [-PRØDUCTH(0-15)]
-PØP CØUNT A [-PPA(0-4)]
-A ØPERAND 2 [-WXAØP(0-15)]
-CØNTRØL [-WXØPC(8-11)]
-PRØDUCT LØWER [-PRØDUCTL(0-15)]
-B ØPERAND 2 [-WXBØP2(0-15)]
-PØP CØUNT B [-PPB(0-4)]
-SIGNIFICANCE CØUNT [-SIGCNT(0-4)]
-STATUS [-SS(0-3)]
-CLØCK [-8B12-CI(TO)]
-INTERRUPT DØNE [-ITDØNE(8)]
+INTERRUPT [-NINTR(29)]
-WØST SIG U/L
-CLØCK [-8B13-CI(TO)]
+STØP [-NSTØP(4)]
-SHADØW RØW SELECT 7 [-USR7(8)]
+INTERRUPT [-NINTR(7)]
-INTERRUPT DØNE [-ITDØNE(1)]
-SHADØW RØW SELECT 4 [-USR4(7)]
-DATA ØUT UPPER [-DATAØUTU(0-15)]
-CLØCK [-2B14-CI(TO)]
+STØP [-NSTØP(1)]
+INTERRUPT [-NINTR(1)]
-CLØCK [-8B10-CI(TO)]
-CLØCK [-8B11-CI(TO)]
+INTERRUPT [-NINTR(4)]
-CLØCK [-8B04-CI(TO)]
-DATA (0-15) [-WXDIA(0-15)]
-CLØCK [-8B17-CI(TO)]
-CØNTRØL6 [-WXØPC0(6)]
-INTERRUPT DØNE [-ITDØNE(3)]
-SHADØW RØW SELECT [-URS6(7)]
+INTERRUPT [-NINTR(6)]
-CLØCK [-8B03-CI(TO)]
+INTERRUPT [-NINTR(3)]
-CLØCK [-8B15-CI(TO)]
-INTERRUPT DØNE [-ITDØNE(2)]
-SHADØW RØW SELECT 7 [-URS7(7)]
+INTERRUPT [-NINTR(5)]
-B ØPERAND (0-15) [-WXDIB(0-15)]
-CLØCK [-8B18-C2(TO)]
-CØNTRØL 7 [-WXØPC0(7)]
-INTERRUPT DØNE [-ITDØNE(0)]
+INTERRUPT [-NINTR(0)]
-CLØCK [-2B01-CI(TO)]
+STØP (2) [-NSTØP(2)]
-SHADØW RØW SELECT 5 [-URS5(7)]
-CØMPARE UPPER TØ SHADØW [-WAND13(0-15)]
-CØMPARE LØWER TØ SHADØW [-WAND13(0-15)]
-MULT STATUS [-WXSTAT(0-5)]
-SHADØW RGTR TB [-WAND20(0-7)]
-X BAR 1 IN [-WXØUTU(0-15)]
-GREATER THEN [-GT1]
-EQUAL [-EQ1]
-GREATER THEN [-GT2]
-EQUAL [-EQ2]
-ØUTPUT UPPER TØ SHADØW [-WAND13(0-15)]
-X BAR 2 IN [-WXØUTL(0-15)]
-ØUTPUT LØWER TØ SHADØW [-WAND13(0-15)]
-GREATER THEN [-GT3]
-EQUAL [-EQ3]
-GREATER THEN [-GT4]
-EQUAL [-EQ4]
NØTE: ⚠ ØUTPUT BGTR IS UNDEFINED WHEN CZERØ IS LØ.
CB ARRAY
LEVEL 4 DIAGRAM ØUTPUT AND CØMPARE RGTR
DEVELOPMENT DIVISION
DB-A2MUL:A2
60461830
REV A
MUL 4.0-08
IV-6-21



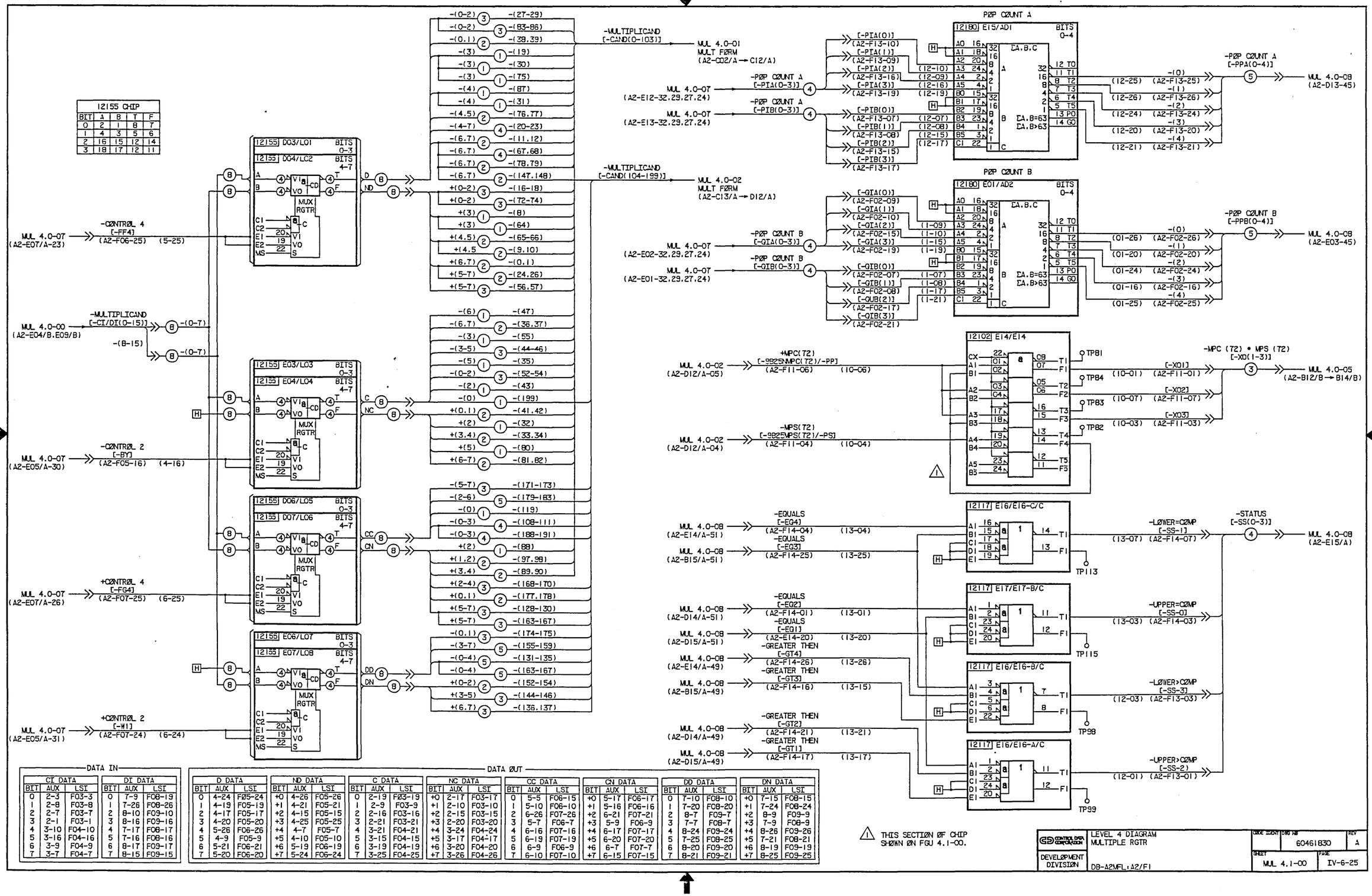


CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
MULTIPLY
SHADØW WIRED 'AND' 13 & 20

D8-A2MUL:A2

CODE IDENT | DWG NO: 60461830 | REV: A
SHEET: MUL 4.0-09 | PAGE: IV-6-23


12155 CHIP
BIT A B T F
0 2 1 8 7
1 4 3 5 6
2 16 15 12 14
3 18 17 12 11
MUL 4.0-07 (A2-E07/A-23)
-CONTRØL 4 [-FF4] (A2-F06-25) (5-25)
MUL 4.0-07 (A2-E05/A-30)
-CONTRØL 2 [-BY] (A2-F05-16) (4-16)
MUL 4.0-07 (A2-E07/A-26)
+CONTRØL 4 [-FG4] (A2-F07-25) (6-25)
MUL 4.0-07 (A2-E05/A-31)
+CONTRØL 2 [-WI] (A2-F07-24) (6-24)
MUL 4.0-00 (A2-E04/B.E09/B)
-MULTIPLICAND [-CI/DI(0-15)]
-(0-7)
-(8-15)
12155 D03/L01 BITS 0-3
12155 D04/L02 BITS 4-7
12155 E03/L03 BITS 0-3
12155 E04/L04 BITS 4-7
12155 D06/L05 BITS 0-3
12155 D07/L06 BITS 4-7
12155 E06/L07 BITS 0-3
12155 E07/L08 BITS 4-7
MUX RGTR
-MULTIPLICAND [-CAND(0-103)]
-MULTIPLICAND [-CAND(104-199)]
MUL 4.0-01 MULT FØRM (A2-C02/A→C12/A)
MUL 4.0-02 MULT FØRM (A2-C13/A→D12/A)
-PØP CØUNT A [-PIA(0-3)]
-PØP CØUNT A [-PIB(0-3)]
-PØP CØUNT B [-QIA(0-3)]
-PØP CØUNT B [-QIB(0-3)]
MUL 4.0-07 (A2-E12-32.29.27.24)
MUL 4.0-07 (A2-E13-32.29.27.24)
MUL 4.0-07 (A2-E02-32.29.27.24)
MUL 4.0-07 (A2-E01-32.29.27.24)
12180 E15/AD1
12180 E01/AD2
EA.B.C
EA.B=63
EA.B>63
PØP CØUNT A
PØP CØUNT B
-PØP CØUNT A [-PPA(0-4)]
-PØP CØUNT B [-PPB(0-4)]
MUL 4.0-08 (A2-D13-45)
MUL 4.0-08 (A2-E03-45)
MUL 4.0-02 (A2-D12/A-05)
MUL 4.0-02 (A2-D12/A-04)
+MPC(72) [-9825MPC(72)/-PP] (A2-F11-06) (10-06)
-MPS(72) [-9825MPS(72)/-PS] (A2-F11-04) (10-04)
12102 E14/E14
-MPC (72) • MPS (72) [-XO(1-3)]
MUL 4.0-05 (A2-B12/B→B14/B)
TP81
TP84
TP83
TP82
[-XO1] (A2-F11-01)
[-XO2] (A2-F11-07)
[-XO3] (A2-F11-03)
MUL 4.0-08 (A2-E14/A-51)
MUL 4.0-08 (A2-B15/A-51)
MUL 4.0-08 (A2-D14/A-51)
MUL 4.0-08 (A2-D15/A-51)
MUL 4.0-08 (A2-E14/A-49)
MUL 4.0-08 (A2-B15/A-49)
MUL 4.0-08 (A2-D14/A-49)
MUL 4.0-08 (A2-D15/A-49)
-EQUALS [-EQ4] (A2-F14-04) (13-04)
-EQUALS [-EQ3] (A2-F14-25) (13-25)
-EQUALS [-EQ2] (A2-F14-01) (13-01)
-EQUALS [-EQ1] (A2-E14-20) (13-20)
-GREATER THEN [-GT4] (A2-F14-26) (13-26)
-GREATER THEN [-GT3] (A2-F14-16) (13-15)
-GREATER THEN [-GT2] (A2-F14-21) (13-21)
-GREATER THEN [-GT1] (A2-F14-17) (13-17)
12117 E16/E16-C/C
12117 E17/E17-B/C
12117 E16/E16-B/C
12117 E16/E16-A/C
-LØWER=CØMP [-SS-1] (13-07) (A2-F14-07)
-UPPER=CØMP [-SS-0] (13-03) (A2-F14-03)
-LØWER>CØMP [-SS-3] (12-03) (A2-F13-03)
-UPPER>CØMP [-SS-2] (12-01) (A2-F13-01)
-STATUS [-SS(0-3)]
MUL 4.0-08 (A2-E15/A)
TP113
TP115
TP98
TP99
THIS SECTIØN ØF CHIP SHØWN ØN FGU 4.1-00.
DATA IN
CI DATA
DI DATA
DATA ØUT
D DATA
ND DATA
C DATA
NC DATA
CC DATA
CN DATA
DD DATA
DN DATA
CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 4 DIAGRAM MULTIPLE RGTR
DB-A2MFL:A2/F1
60461830
REV A
SHEET MUL 4.1-00
PAGE IV-6-25

7. RING PORT UNIT (RPU)

SYSTEM FUNCTION

The ring port units (RPUs), which are located with the base processor, provide the interface between the base processor and any other unit on the system ring (RP0) or application ring (RP1). The ring ports are used to transfer data, synchronize programs, and provide control for and access to the base processor. The system and application rings are high-speed, uni-directional, parallel channels which transmit data and associated control and addressing information in specially formatted parcels called ring packets. The shadow matrix is part of ring port 0, but, because of its complexity, is shown and discussed separately in the next section of this document.

GENERAL DESCRIPTION

There are two ring port units with a base processor. Each performs ring communication functions for the base processor. Ring port 0 interfaces the base processor to the system ring, which must include a CYBER channel ring port, and may include other base processors and the system ring interface of the DMAU. Ring port 1 interfaces the base processor to the application ring, which must include other base processors. Of the two ring ports, only RP0 contains the shadow matrix control logic.

LOCATION

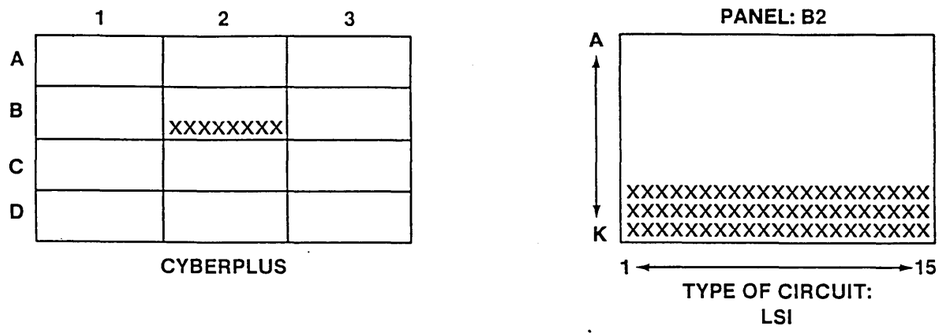


Figure IV-7-1. Location of Ring Port Unit Logic Circuits

FUNCTIONAL DESCRIPTION

The discussion in the following paragraphs refers to the simplified block diagram of the ring port units as shown in figure IV-7-2 and the level 2 diagrams RPU 2.0 and RPU 2.1. The 29-bit ring input registers receive a new ring packet from a ring each clock cycle. Some of the packets contain control information for the ring ports themselves (they are direct-addressed packets). Other packets will be data or control information for the associated base processor (they are indirect-addressed packets). Some packets will not be for the ring port or associated base processor, but will be for another ring port on the same ring.

Once a packet has been received, the ring port checks the function code (most significant 4 bits) of the packet. If it is a direct address function, it sends the functional unit code of the packet to the switch compare logic and compares it to the equipment code switches. If a match exists, the packet is retained by the ring port. If not, the packet is sent to the ring output register for placing back on the ring.

If it is an indirect address function, the path code (bits 4--7) specifies an address of a destination table entry. If that entry is enabled, then the ring packet (less the destination code) is placed in the input FIFO for processing. If the entry is disabled, the packet is sent to the ring output register for placing back on the ring. Once a retained packet is processed, the gobble bit entry will be checked. If it is not set (that is, the ring port is not to "gobble" the packet), the packet is sent to the ring output register for placing back on the ring.

The 12-bit control register receives the 12-bit operation code from the 16-bit dynamic control field of the processor instruction word via the crossbar. The bits of the operation code determine what function the ring port will perform under control of the processor.

The 16-bit A register receives data from the crossbar when enabled by the A clock. The A clock is set by the program into the clock control field of the instruction word, bit 41(RP0) or 43(RP1). The clock bits gate the data at time 0 of clock cycle one when they are set. If the clock bits are clear, the contents of the A register is not changed.

The 16-bit crossbar register receives the same data as the A register (one is the complement of the other). The status and mask register is loaded with the data from the crossbar register when the load mask instruction is used.

The 8-bit shadow select register, which only exists in RP0, is loaded from the A register (bits 8--15) or the ring input register (bits 12--19). It contains the location code of the 16-bit shadow register being read from the shadow matrix.

The destination table is a 16-word 6-bit memory. Each 6-bit word loaded into the table contains a 4-bit destination code (bits 0--3), a "gobble" bit (bit 4), and an enable bit (bit 5). The table is loaded from bits 8--13 of the ring input register.

The 24-bit input FIFO holding register (made up of two blocks, the 8-bit holding register and 16-bit FIFO data register) receives the indirectly addressed packets as they leave the input FIFO buffer. Here they are decoded and routed to either the operation table (function codes 4 or C), one of the four data memories or XMAU 0 (function codes 1, 3, 9, or C), or they are used to set a status flag register bit (function codes 2, 3, A, or B). For function codes 9, A, B, or C an indirect interrupt request is also generated.

The operation table is a 16-word 16-bit memory. Each 16-bit word loaded into the table contains a 12-bit unit operation code (bits 0--11) and a 4-bit functional unit code (bits 12--15). This 16-bit word format is identical to the dynamic control field format of the processor instruction word. If the holding register contains a data transfer packet, the 12-bit operation code portion is transmitted to either one of the four data memory units or to XMAU 0 (in ring port 0, only) via the operation table output circuits.

The 29-bit ring output register allows placing of ring packets onto the ring. The register is loaded from the ring input register, the shadow matrix (RPO only), the output FIFO buffer, or, if the output FIFO buffer is empty, it is set to all zeros (empty packet).

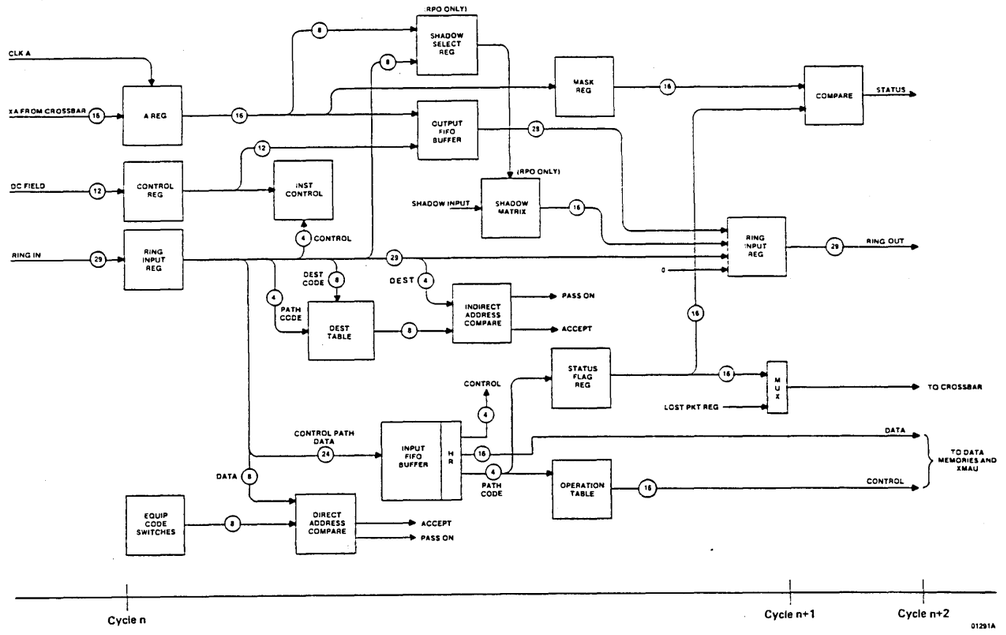


Figure IV-7-2. Ring Port Unit Block Diagram

TIMING

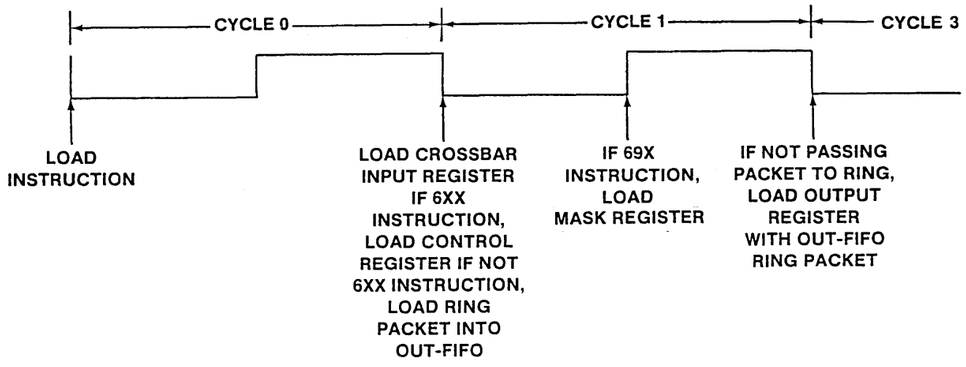

CYCLE 0
CYCLE 1
CYCLE 3
LOAD INSTRUCTION
LOAD CROSSBAR INPUT REGISTER IF 6XX INSTRUCTION, LOAD CONTROL REGISTER IF NOT 6XX INSTRUCTION, LOAD RING PACKET INTO OUT-FIFO
IF 69X INSTRUCTION, LOAD MASK REGISTER
IF NOT PASSING PACKET TO RING, LOAD OUTPUT REGISTER WITH OUT-FIFO RING PACKET

Figure IV-7-3. Ring Port Unit Processor Instructions Timing

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C2N 2.0 X BAR FAN2UT TRUE DATA
16
X BAR REGISTER RPU 4.0-01
16
8
SHA 2.0 SHAD2W SELECT REGISTER
MASK REGISTER RPU 4.0-01
16
FLAG REGISTER RPU 4.0-12
16
15
FLAG C2MPARE RPU 4.0-12
2
C2NDITI2N VECT2R REGISTER RPU 4.0-21
2
3
C2N 2.0
INTERNAL STATUS
6
STATUS REGISTER RPU 4.0-01
16 SHAD2W
1
5 SHAD2W
RPU 2.1 SHAD2W WIRED 'AND' 21
C2N 2.0
C2N 2.0 AND 20
SHAD2W WIRED
SET FLAG DEC2DER RPU 4.0-12
16
12
PART 2F SHAD2W WIRED △1 'AND' 20 RPU 4.3-00
16
SHA 2.0
16
12
16
28-BIT L2ST PACKET REGISTER RPU 4.0-13
16
X BAR DATA RPU 4.0-13
16
RPU 2.1 X BAR DATA
C2N 2.0 X BAR FAN2UT C2MP DATA
16
A REGISTER RPU 4.2-00
15
RPO 2UTPUT FIF2 RPU 4.2-03
28
SYSTEM RING
RPO ACCEPT/REJECT INDIRECT ADDRESS PACKET
C2N 2.0 DC FIELDS FAN2UT
12
C2NTR2L REGISTER RPU 4.0-01
12
12 SHAD2W
△2
SHA 2.0 2R SHA 2.1
16
1
SHAD2W L2CK2UT GATE RPU 4.0-20
15
1
RPO RING 2UTPUT REGISTER RPU 4.0-00
29
4 DMU 2.0 ADRS MUX
4 DMU 2.0 ADRS MUX
4 DMU 2.0 ADRS MUX
4 DMU 2.0 ADRS MUX 2UTPUT CABLE
8 DMU 2.0 MICR2 INSTR RGTR
8 DMU 2.0 MICR2 INSTR RGTR
8 DMU 2.0 MICR2 INSTR RGTR
8 DMU 2.0 MICR2 INSTR RGTR
RPO RING INPUT REGISTER RPU 4.0-00
28
SYSTEM RING
29
RING INPUT REGISTER FAN2UT RPU 4.0-10
28
28
6
4
12
24
C2N 2.0 BKPT RGTR MUX B
6
4
C2MPARE RPU 4.0-11
4
5
12
2PERATI2N TABLE 2UTPUT RPU 4.2-10
RPU 2.1 2PERATI2N TABLE 2UTPUT
DESTINATI2N TABLE RPU 4.0-11
+G2BBLE BIT
5
4
RPU 2.1 MEM2RY DATA
RING 2UTPUT BUFFER RPU 4.2-10
16 DMU 2.0 DATA SELECT
16 DMU 2.0 DATA SELECT
16 DMU 2.0 DATA SELECT
16 DMU 2.0 DATA SELECT
8
INPUT C2NTR2L H2LDING REGISTER RPU 4.0-00
4
4
RPO 2PERATI2N TABLE RPU 4.2-12
12
12
XMA 2.0 C2NTR2L RGTR
16
EGUIP ID SW C2MPARE RPU 4.0-11
8
INPUT FIF2 RPU 4.0-10
8
16
INPUT DATA H2LDING REGISTER RPU 4.0-00
16
16
MEM2RY DATA RPU 4.2-10
16
XMU 2.0 A/D DATA RGTR
RPO EQUIP C2DE SWITCHES
8
RPO ACCEPT/REJECT DIRECT ADDRESS PACKET

NOTE:
△1 SHAD2W RGTR AND WIRED 'AND' DUPLICATED 2N SHA 2.0.
△2 INPUT FR2M SHA 2.0. IF N2 FL2ATING P2INT UNIT. 2THERWISE INPUT FR2M FSH 2.0

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 2 DIAGRAM
RING PORT 0
CAGE IDENT
DWG NO 60461830
REV A
SHEET RPU 2.0
PAGE IV-7-5

C0N 2.0 X BAR FAN0UT (16)

X BAR REGISTER RPU 4.1-01 (16)

MASK REGISTER RPU 4.1-01 (16)

FLAG REGISTER RPU 4.1-12 (16)

FLAG C0MPARE RPU 4.1-12 (15)

C0NDITI0N VECT0R REGISTER RPU 4.1-21 (2)

(3) C0N 2.0

INTERNAL STATUS (5)

STATUS REGISTER RPU 4.1-01

(16) SHAD0W

(4) SHAD0W

(1)

C0N 2.0 AND 21 — SHAD0W WIRED (16)

(16)

(9)

(12)

PART 0F SHAD0W WIRED 'AND' 21 ⚠1 RPU 4.3-00 (16) SHA 2.0

RPU 2.0 STATUS (5)

C0N 2.0 X BAR FAN0UT (16)

A REGISTER RPU 4.2-00 (16)

SET FLAG DEC0DER RPU 4.1-12

28-BIT L0ST PACKET REGISTER RPU 4.1-13

RPU 2.0 X BAR DATA (16)

(12)

(16)

X BAR DATA SELECT0R RPU 4.1-13 (16) C0N 2.0 DATA X BAR

C0N 2.0 DC FIELDS FAN0UT (12)

C0NTR0L REGISTER RPU 4.1-01 (12)

(12)

RPI 0UTPUT FIF0 RPU 4.2-03 (28)

RPI RING 0UTPUT REGISTER RPU 4.1-00 (29) APPLICATI0N RING

APPLICATI0N RING (29)

RPI RING INPUT REGISTER RPU 4.1-00 (28)

RING INPUT REGISTER FAN0UT RPU 4.1-10

(28)

(28)

(6)

(4)

(24)

(4) (5)

DESTINATI0N TABLE RPU 4.1-11

+G0BBLE BIT

(4)

(5)

C0MPARE RPU 4.1-11

RPI ACCEPT/REJECT INDIRECT ADDRESS PACKET

(8)

INPUT C0NTR0L H0LDING REGISTER RPU 4.1-00 (4)

(4)

(16)

RPI 0PERATI0N TABLE RPU 4.2-11 (12)

0PERATI0N TABLE 0UTPUT RPU 4.2-11 (12) RPU 2.0 0PERATI0N TABLE 0UTPUT

RPI EQUIP C0DE SWITCHES (8)

EQUIP ID SW C0MPARE RPU 4.1-11

INPUT FIF0 RPU 4.1-10 (8) (16)

INPUT DATA H0LDING REGISTER RPU 4.1-00 (16)

(16)

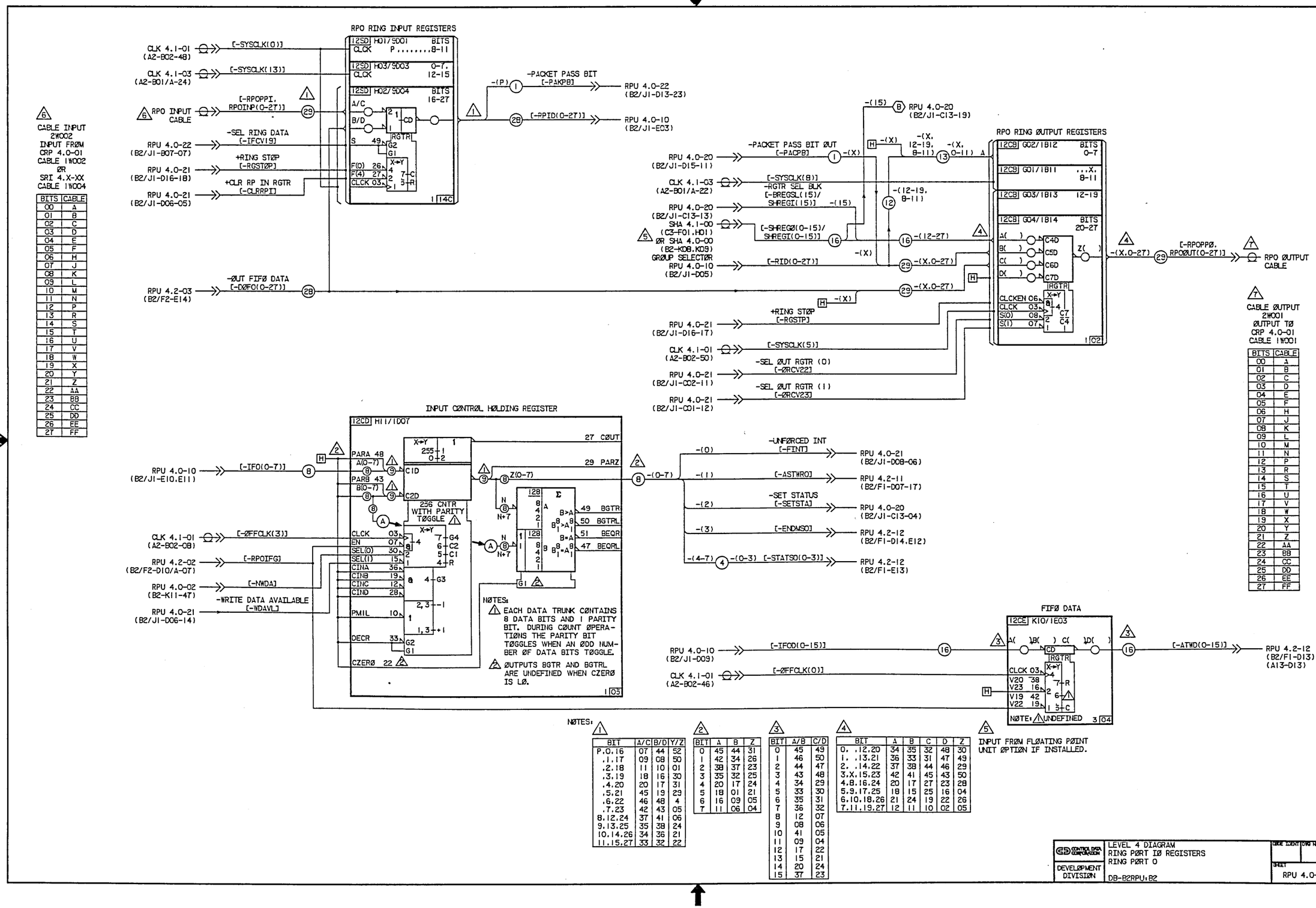
MEMORY DATA RPU 4.2-11 (16) RPU 2.0 RING 0UTPUT BUFFER

RPI ACCEPT/REJECT DIRECT ADDRESS PACKET

N0TE:

⚠1 SHAD0W RGTR AND WIRED 'AND' DUPLICATED 0N SHA 2.0.

GE CONTROL DATA CORPORATION	LEVEL 2 DIAGRAM RING PART 1	CODE IDENT/DWG NO 60461830	REV A
DEVELOPMENT DIVISION		SHEET RPU 2.1	PAGE IV-7-7



NØTES:

1

BIT	A/C	B/D	Y/Z
P.0.16	07	44	52
.1.17	09	08	50
.2.18	11	10	01
.3.19	18	16	30
.4.20	20	17	31
.5.21	45	19	29
.6.22	46	48	4
.7.23	42	43	05
8.12.24	37	41	06
9.13.25	35	38	24
10.14.26	34	36	21
11.15.27	33	32	22

2

BIT	A	B	Z
0	45	44	31
1	42	34	26
2	38	37	23
3	35	32	25
4	20	17	24
5	18	01	21
6	16	09	05
7	11	06	04

3

BIT	A/B	C/D
0	45	49
1	46	50
2	44	47
3	43	48
4	34	29
5	33	30
6	35	31
7	36	32
8	12	07
9	08	06
10	41	05
11	09	04
12	17	22
13	15	21
14	20	24
15	37	23

4

BIT	A	B	C	D	Z
0, .12,20	34	35	32	48	30
1, .13,21	36	33	31	47	49
2, .14,22	37	38	44	46	29
3,X,15,23	42	41	45	43	50
4,8,16,24	20	17	27	23	28
5,9,17,25	18	15	25	16	04
6,10,18,26	21	24	19	22	26
7,11,19,27	12	11	10	02	05

5 INPUT FRØM FLØATING PØINT UNIT ØPTIØN IF INSTALLED.

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
RING PØRT IØ REGISTERS
RING PØRT O

DB-B2RPU:B2

CAGE IDENT | DWG NØ 60461830 | REV A
SHEET RPU 4.0-00 | PAGE IV-7-9

CØNTRØL REGISTER

12DB G07/8B01

C2N 4.1-00 (C2-E01/A→E15/A-27) -RING PØRT 0 DC FIELD(0-11) [-FID(0-8)14/RPOCTL(0-11)] -(0-11)

CLK 4.1-01 (A2-B02-51) [-ØFFCLK(1)]

C2N 4.5-21 (C2/C1-E13-08) [-ITDØNE(10)]

C2N 4.5-31 (C2/C2-E05-04) [-NINTR(1)]

C2N 4.1-00 (C2-F09-22) -LØAD RING PØRT 0 CØNTRØL RGTR [-GØU(14)/GØRPO]

SHA 4.0-01 (B2-A06/B-27) -SHADØW RØW SELECT 1 [-URS1(8)]

MASTER SLAVE

A(0-3) 17.18. 36.37 — C1D C2D RGTR — D(0-3) 23.27.30.33 26.28.31.34 -(3.4.6.7)

C1 3 ENI 9 XFR 8 GØI 35 ENS 10 — X↔Y 4 2 1 5.7→C2 6→C1 — GI 1 1

E(0-3) 24.25. 29.32 -(3.4.6.7)

B(0-7) 16.15. 11.12. 44.38. 41.42 -(0-2, 5.8-11)

C2 2 ENI 46 GØ2 43

F(0-7) 22.21.6. 4.51.49. 47.45 -(0-2.5.8.11) -CØNT REG [-ØFCØ(0-11)] RPU 4.2-03 (B2/F2-D14)

G(0-7) 19.20.7. 5.1.52. 50.48 -(0-2.5.8.11) -CØNTRØL RGTR SHADØW [-WAND2Ø(0-11)] RPU 4.3-00 SHADØW WIRED 'AND' 20

0 00

[-CFØNB(3.4.7)] -(3) RPU 4.2-01 (B2/F2-D11-18)

-(4) RPU 4.2-01 (B2/F2-C08-04)

-(7) RPU 4.2-01 (B2/F2-E12/B-23)

RPU 4.0-22 (BE/J1-B07-11) +INT ENABLE [-INTEN] -(0)

RPU 4.0-21 (B2/J1-D07-12) -ANY BIT CØMPARES [-ANYCMP] -(1)

RPU 4.0-21 (B2/J1-D07-16) -ALL BITS CØMPARE [-ALCMP] -(2)

RPU 4.0-02 (B2-G05-49) [-NØFFLO] -(3) -(0-3)

-(3) -(5) -(6)

RPU 4.0-21 (B2/J1-B03-13) -RPO CLR STAT STØP [-RPOCS] -(4)

RPU 4.0-22 (B2/J1-C07-14) -STACK FULL [-SKFULL] -(7) -(4-7)

CLK 4.1-01 (A2-B02-06) [-SYSCLK(3)]

SHA 4.0-02 (B2-A06/D-08) -SHADØW RØW SELECT 3 [-URS3(9)]

C RPU 4.1-01

RPU 4.2-01 (B2/F2-E12/A-07) [-GTEMKØ]

CLK 4.1-01 (A2-B02-01) [-ØFFCLK(2)]

SHA 4.0-02 (B2-A06/A-46) -SHADØW RØW SELECT 2 [-URS2(8)]

STATUS AND MASK REGISTERS

12DB H09/8B02 A(0-3) — STATUS BITS 0-3, MASK BITS 0-7

12DB H10/8B03 — STATUS BITS 4-7, MASK BITS 8-15

MASTER SLAVE

A(0-3) 17.18. 36.37 — C1D C2D RGTR — D(0-3) 23.27.30.33 26.28.31.34

C1 3 ENI 9 XFR 8 GØI 35 ENS 10 — X↔Y 4 2 1 5.7→C2 6→C1 — GI 1 1

E(0-3) 24.25. 29.32

B(0-7) 16.15. 11.12. 44.38. 41.42 -(0-15)

C2 2 ENI 46 GØ2 43

F(0-7) 22.21.6. 4.51.49. 47.45

G(0-7) 19.20.7. 5.1.52. 50.48

0 00

-(4) -RPO CLR STAT STØP [-RPOCSS] RPU 4.0-21 (B2/J1-A04/B-04)

-(5.6) -(5) [-ØFFULO] C2N 4.3-00 CØNDITIØN VECTØR (C2-G06-49)

-(6) [-ØFFULO] RPU 4.2-01 (B2/F2-B11/A-06)

L

CLK 4.1-01 (A2-B02-06) [-SYSCLK(3)]

SHADØW RØW SELECT 3 [-URS3(9)] SHA 4.0-02 (B2-A06/D-08)

-(5) -(0-3.7) -STATUS RGTR SHADØW [-WAND21(3.1.2.0.8)] RPU 4.3-00 SHADØW WIRED 'AND' 21

-(0-15) [-MASK(0-15)] RPU 4.0-12 (B2/J1-C14)

-(0-15) -MASK RGTR SHADØW [-WAND20(0-15)] RPU 4.3-00 SHADØW WIRED 'AND' 20

RPU 4.2-01 (B2/F2-E12/A-07) [-GTEMKØ]

CLK 4.1-01 (A2-B02-01) [-ØFFCLK(2)]

SHA 4.0-02 (B2-A06/A-46) -SHADØW RØW SELECT 2 [-URS2(8)]

-(0-15)

XBAR REGISTER

12CE H08/1EC8

C2N 4.2-00 X BAR FANØUT (D2-A06→A11) -XBAR TØ RPO [-RPOXBR(0-15)/RPOXBI(0-15)]

A( ) B( ) C( ) D( ) — CD — RGTR — X↔Y 4 — 7→R 6→C 5→C

CLK 4.1-01 (A2-B02-47) [-SYSCLK(4)]

C2N 4.1-00 (C2-E11/B-47) [-CLK41/RPOCA]

H

NØTE: UNDEFINED 3 04

[-XBREGO(0-15)] -(8-15) -XBAR RGTR SEL SHA 4.0-00 (B2-G08-B(0-7))

A RPU 4.2-01 (B2/F2-E12/C-19)

RPU 4.0-21 (B2/J1-C09-11) +MC [-MMCT]

12HB A C15/7B17-A/B

CX 15 — A(0) 17 — A(1) 18 — A(2) 36 — A(3) 35 — 12|12

20 T1(0) 19 T2(0) 22 F1(0) 21 F2(0) 25 T1(1) 26 T2(1) 23 F1(1) 24 F2(1) 27 T1(2) 28 T2(2) 29 F1(2) 30 F2(2) 34 T1(3) 33 T2(3) 32 F1(3) 31 F2(3)

1 02

[-MCF(8)] RPU 4.0-02 (B2-G06.G05-15.30)

[-MCL] NU

[-MCT(0)] XMA 4.10-01 (D2/E1-B08/B-19)

[-MCF(9)] RPU 4.0-02 (B2-K12.K11-15.30)

[-MCL] NU

[-MCT(1)] XMA 4.11-01 (D2/E2-C07/B-24)

[-MCF(10)] RPU 4.1-02 (B2-G10.G11-15.30)

[-MCL] NU

[-MCT(2)/MSTCLR] C2N 4.5-01 (C2/B1-C05-22)

[-MCF(11)] RPU 4.1-02 (B2-K05.K06-15.30)

[-MCL] NU

12HB B C15/7B18-B/B

CX 41 — A(0) 43 — A(1) 44 — A(2) 10 — A(3) 09 — 12|12

46 T1(0) 45 T2(0) 48 F1(0) 47 F2(0) 51 T1(1) 52 T2(1) 49 F1(1) 50 F2(1) 01 T1(2) 02 T2(2) 03 F1(2) 04 F2(2) 08 T1(3) 07 T2(3) 06 F1(3) 05 F2(3)

1 02

L

[-MCF(0)/MCF] FPC 4.0-04 (C3-B08/E-41)

[-MCF(4)] XMA 4.0-02 (D2-B12-30)

[-MCF(1)/NMCLR] MMI 4.0-00 (C1/P-G11.G10-22)

[-MCF(5)] XMA 4.1-02 (D2-F12-30)

[-MCF(2)/EXTMCI] MRI 4.2-05 (C1/E-D04-22)

[-NMSCL1] +MC RPU 4.1-21 (B2/J2-C09-19.20.23)

[-MCF(3)/NMCI] MEL 4.0-04 (C1/D-A09-22)

[-MCF(7)/MCF] RPU 4.2-01 (B2/F2-D11-22)

NØTES: 1

BIT	A/B	C/D
0	45	49
1	46	50
2	44	47
3	43	48
4	34	29
5	33	30
6	35	31
7	36	32
8	12	07
9	08	06
10	41	05
11	09	04
12	17	22
13	15	21
14	20	24
15	37	23

CONTROL DATA CORPORATION — DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
CØNTRØL, STATUS, AND MASK
RING PØRT 0

DB-B2RPU:B2

CODE IDENT NO 60461830 REV A

SHEET RPU 4.0-01 PAGE IV-7-11

INPUT FIFØ WRITE/READ CØUNTER

12CD KI2/1D05

PARA 48 · PARB 43 · A(0-7) · B(0-7) · H · L · B · A · N · N+7

C1D · C2D · Z4 · Z3 · Z2 · Z1

DUAL 16 CNTRS WITH PARITY TØGGLE

CLCK 03 · EN 07 · SEL(0) 30 · SEL(1) 15 · PM8ØIU 52 · PMIL 10 · DECR 33 · CZERØ 22

X=Y · G3 · C2 · C1 · R · G2 · G1

Σ · 128 8 4 2 1 · A B 128>A 128 16 · B 8>A 8 1 · 128=A 128 16 · B 8=A 8 1

29 PARZ · Z(0-7) · Z(0) · Z(5) · Z(4) · Z(7) · 49 BGTR · 50 BGTRL · 51 BEQR · 47 BEQRL

NØTES:

1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. THE DATA BITS FRØM EACH TRUNK SEPARATE, 4 BITS TØ EACH CØUNTER. THE SELECTED PARITY BIT STILL REPRESENTS THE PARITY FØR ALL 8 SELECTED DATA BITS. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF THE 8 DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

5|05

-(0-7) · -(0-3) · -WRITE ADRS [-WRIFA(0-3)] → RPU 4.0-10 (B2/J1-D12)

-(4-7) · -READ ADRS [-RDIFA(0-3)] → RPU 4.0-10 (B2/J1-E12)

CLK 4.1-01 (A2-B02-49) [-SYSCLK(1)]

RPU 4.0-01 (B2-C15/A-25) [-MCF(9)]

-WRITE IN FIFØ [-WRITIF]

RPU 4.0-11 (B2/J1-D03-13) -RD IN FIFØ [-RDIF]

RPU 4.0-20 (B2/J1-E08-08)

INPUT FIFØ WØRD CØUNTER

12CD KI1/1D06

PARA 48 · PARB 43 · A(0-7) · B(0-7) · H · L · B · A · N · N+7

C1D · C2D · Z4 · Z3 · Z2 · Z1

DUAL 16 CNTRS WITH PARITY TØGGLE

CLCK 03 · EN 07 · SEL(0) 30 · SEL(1) 15 · PM8ØIU 52 · PMIL 10 · DECR 33 · CZERØ 22

X=Y · G3 · C2 · C1 · R · G2 · G1

Σ · 128 8 4 2 1 · A B 128>A 128 16 · B 8>A 8 1 · 128=A 128 16 · B 8=A 8 1

29 PARZ · Z(0-7) · Z(0) · Z(5) · Z(4) · Z(7) · 49 BGTR · 50 BGTRL · 51 BEQR · 47 BEQRL

NØTES:

1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. THE DATA BITS FRØM EACH TRUNK SEPARATE, 4 BITS TØ EACH CØUNTER. THE SELECTED PARITY BIT STILL REPRESENTS THE PARITY FØR ALL 8 SELECTED DATA BITS. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF THE 8 DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

5|05

NU · BIAS 0 FRØM PANEL A2 · [-ROINPF] · H · -(0-7) · -(0.2) · -(1.3) · -(4-7)

-(0-7) → [-NIFFLO] → RPU 4.2-01 (B2/F2-E11-19)

+WRITE DATA AVAIL [-NWDA] → RPU 4.0-21 (B2/J1-D06-19)

[-NWDA] → RPU 4.0-00 (B2-H11-15)

RPU 4.2-01 (B2/F2-E11-05) [-ENCTRO]

-RD/WRT CNT INHIBIT [-RWIF] → RPU 4.0-11 (B2/J1-E05-05)

ØUTPUT FIFØ WRITE/READ CØUNTER

12CD GO6/1D01

PARA 48 · PARB 43 · A(0-7) · B(0-7) · H · L · B · A · N · N+7

C1D · C2D · Z4 · Z3 · Z2 · Z1

DUAL 16 CNTRS WITH PARITY TØGGLE

CLCK 03 · EN 07 · SEL(0) 30 · SEL(1) 15 · PM8ØIU 52 · PMIL 10 · DECR 33 · CZERØ 22

X=Y · G3 · C2 · C1 · R · G2 · G1

Σ · 128 8 4 2 1 · A B 128>A 128 16 · B 8>A 8 1 · 128=A 128 16 · B 8=A 8 1

29 PARZ · Z(0-7) · Z(0) · Z(5) · Z(4) · Z(7) · 49 BGTR · 50 BGTRL · 51 BEQR · 47 BEQRL

NØTES:

1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. THE DATA BITS FRØM EACH TRUNK SEPARATE, 4 BITS TØ EACH CØUNTER. THE SELECTED PARITY BIT STILL REPRESENTS THE PARITY FØR ALL 8 SELECTED DATA BITS. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF THE 8 DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

5|05

-(0-7) · -(0-3) · [-WRFA0(0-3)] → RPU 4.2-03 (B2/F2-D13)

-(4-7) · [-RDFA0(0-3)] → RPU 4.2-03 (B2/F2-E13)

CLK 4.1-03 (A2-B01/B-51) [-ØFFCLK(5)]

RPU 4.0-01 (B2-C15/A-20) [-MCF(8)]

RPU 4.2-01 (B2/F2-D11-08) [-GATØFO] -EN RD CNTR

RPU 4.0-21 (B2/J1-D07) [-READØF]

ØUTPUT FIFØ WØRD CØUNTER

12CD GO5/1D02

PARA 48 · PARB 43 · A(0-7) · B(0-7) · H · L · B · A · N · N+7

C1D · C2D · Z4 · Z3 · Z2 · Z1

DUAL 16 CNTRS WITH PARITY TØGGLE

CLCK 03 · EN 07 · SEL(0) 30 · SEL(1) 15 · PM8ØIU 52 · PMIL 10 · DECR 33 · CZERØ 22

X=Y · G3 · C2 · C1 · R · G2 · G1

Σ · 128 8 4 2 1 · A B 128>A 128 16 · B 8>A 8 1 · 128=A 128 16 · B 8=A 8 1

29 PARZ · Z(0-7) · Z(0) · Z(5) · Z(4) · Z(7) · 49 BGTR · 50 BGTRL · 51 BEQR · 47 BEQRL

NØTES:

1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. THE DATA BITS FRØM EACH TRUNK SEPARATE, 4 BITS TØ EACH CØUNTER. THE SELECTED PARITY BIT STILL REPRESENTS THE PARITY FØR ALL 8 SELECTED DATA BITS. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF THE 8 DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

5|05

-(0-7) · -(0-3) · [-NØFFLO] → RPU 4.0-01 (B2-H10-18,36) (B2-H09-37)

-(4-7) · +ØUTPUT READY [-NØUTRY] → RPU 4.0-21 (B2/J1-D06-18)

NU · BIAS 0 FRØM PANEL A2 · [-ROØUTF] · H · -(0-7) · -(0-1) · -(2-3) · -(4-7)

NØTE:

BIT	A	B	Z
0	45	44	31
1	42	34	26
2	38	37	23
3	35	32	25
4	20	17	24
5	18	01	21
6	16	09	05
7	11	06	04

CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
FIFØ WRITE/READ AND WØRD CØUNTERS
RING PØRT 0

DB-B2RPU:B2

CODE IDENT · DWG NO 60461830 · REV A

SHEET RPU 4.0-02 · PAGE IV-7-13

RPU 4.0-00 (B2-H02) [-RPID(0-27)] 28

NOTES:

1

BIT	AUX	LSI
0	10-01	B2-J11-01
1	08-01	B2-J09-01
2	12-17	B2-J13-17
3	12-16	B2-J13-16
4	10-03	B2-J11-03
5	10-04	B2-J11-04
6	09-21	B2-J10-21
7	09-03	B2-J10-03

2

BIT	AUX	LSI
0	07-21	B2-J08-21
1	09-20	B2-J10-20
2	09-17	B2-J10-17
3	09-04	B2-J10-04
4	08-03	B2-J09-03
5	09-26	B2-J10-26
6	11-19	B2-J12-19
7	09-01	B2-J10-01
8	08-26	B2-J09-26
9	08-25	B2-J09-25
10	08-24	B2-J09-24
11	11-20	B2-J12-20
12	07-19	B2-J08-19
13	06-09	B2-J07-09
14	07-10	B2-J08-10
15	07-17	B2-J08-17

3

BIT	AUX	LSI
0	02-15	B2-J03-15
1	02-16	B2-J03-16
2	02-10	B2-J03-10
3	02-01	B2-J03-01
4	07-06	B2-J08-06
5	02-26	B2-J03-26
6	02-25	B2-J03-25
7	01-04	B2-J02-04
8	01-10	B2-J02-10
9	01-09	B2-J02-09
10	01-08	B2-J02-08
11	01-07	B2-J02-07
12	03-01	B2-J04-01
13	03-04	B2-J04-04
14	05-26	B2-J06-26
15	13-18	B2-J04-08
16	04-07	B2-J05-07
17	04-06	B2-J05-06
18	04-01	B2-J05-01
19	04-04	B2-J05-04
20	06-03	B2-J07-03
21	03-06	B2-J04-06
22	03-17	B2-J04-17
23	03-09	B2-J04-09
24	04-17	B2-J05-16
25	06-06	B2-J07-06
26	04-19	B2-J05-19
27	06-01	B2-J07-01

4

BIT IN	A	BIT OUT	T1	T2	F1	F2
0,12,16,20,24	24	0	1	2	3	4
1,13,17,21,25	23	1	8	7	6	5
2,14,18,22,26	20	2	11	12	13	14
3,15,19,23,27	19	3	18	17	16	15

5

BIT	AUX	LSI
0	10-24	B2-J11-24
1	10-21	B2-J11-21
2	10-25	B2-J11-25
3	10-20	B2-J11-20

6

BIT	AUX	LSI
0	02-09	B2-J03-09
1	07-07	B2-J08-07
2	02-17	B2-J03-17
3	08-10	B2-J09-10
4	08-16	B2-J09-16
5	08-15	B2-J09-15
6	10-06	B2-J11-06
7	09-19	B2-J10-19
8	07-04	B2-J08-04
9	01-24	B2-J02-24
10	01-20	B2-J02-20
11	01-17	B2-J02-17
12	07-01	B2-J08-01
13	07-08	B2-J08-08
14	07-09	B2-J08-09
15	07-15	B2-J08-15
16	11-09	B2-J12-09
17	11-15	B2-J12-15
18	11-07	B2-J12-07
19	11-24	B2-J12-24
20	03-15	B2-J04-15
21	03-25	B2-J04-25
22	03-26	B2-J04-26
23	03-19	B2-J04-19
24	04-21	B2-J05-21
25	04-26	B2-J05-26
26	04-24	B2-J05-24
27	05-25	B2-J06-25

7

BIT	AUX	LSI
0	07-03	B2-J08-03
1	01-19	B2-J02-19
2	01-26	B2-J02-26
3	01-16	B2-J02-16
4	03-20	B2-J04-20
5	03-24	B2-J04-24
6	02-26	B2-J03-26
7	03-21	B2-J04-21
8	06-10	B2-J07-10
9	04-20	B2-J05-20
10	06-16	B2-J07-16
11	05-03	B2-J06-03

8

BIT	AUX	LSI
0	10-26	B2-J11-26
1	13-21	B2-J14-21
2	13-06	B2-J14-06
3	13-24	B2-J14-24

-(0) -INTR BIT (S) RPU 4.0-11 (B2/J1-A04/A-18)

RPU 4.0-02 (B2-K12) 8 -WRITE ADRS [-WRIFA(0-3)]

RPU 4.0-02 (B2-K12) 5 -READ ADRS [-RDIFA(0-3)]

RING INPUT RGTR FANØUT

12112 E03/A13 BITS 0-3

12112 E02/A14 BITS 4-7

12112 E01/A15 BITS 8-11

[-RPID(1-3)] (T) RPU 4.0-11 (B2/J1-D03)

[-RPID(4-7)] (U) RPU 4.0-11 (B2/J1-D01)

-(9-10) (V) RPU 4.0-22 (B2/J1-E01-01)

12112 D12/A01 BITS 0-3

12112 E12/A02 BITS 0-3

TP86,87, 74,73

TP91,78, 75,114

[+RIPD(0-3)] RPU 4.0-21 (B2/J1-C03/B)

RPU 4.0-20 (B2/J1-E08-12) -IN FIFØ WE2

RPU 4.0-20 (B2/J1-E08-16) -IN FIFØ WE1

[-RID(4-7)] RPU 4.0-11 (B2/J1-D01,D02)

[-RID(5-7)] RPU 4.0-22 (B2/J1-A01)

RING INPUT RGTR FANØUT

12112 C04/C01 BITS 12-15 FI

12112 C05/C02 BITS 16-19

12112 D04/C03 BITS 20-23

12112 D05/C04 BITS 24-27

INPUT FIFØ

12145 E11/B03 BITS 0-3

12145 E10/B04 4-7

12145 E09/B05 12-15

12145 D11/B06 16-19

12145 D10/B07 20-23

12145 D09/B08 BITS 24-27

1A15 1A00

2A15 2A00

MEM

[-IFI0(0-7)] RPU 4.0-00 (B2-H11)

[-IFC0(0-15)] RPU 4.0-00 (B2-K10)

+(12,13) [-NRPID(12-13)] RPU 4.0-11 (B2/J1-D02-13,14)

[-RADD(0-11)] C2N 4.0-00 (C2-A13,F05)

-RING RGTR SEL

[-RID(12-19)] SHA 4.0-00 (B2-G08/A)

[-RID(0-27)] RPU 4.0-00 (B2-G04)

[+RPID(0-19)] RPU 4.0-13 (B2/J1-B08)

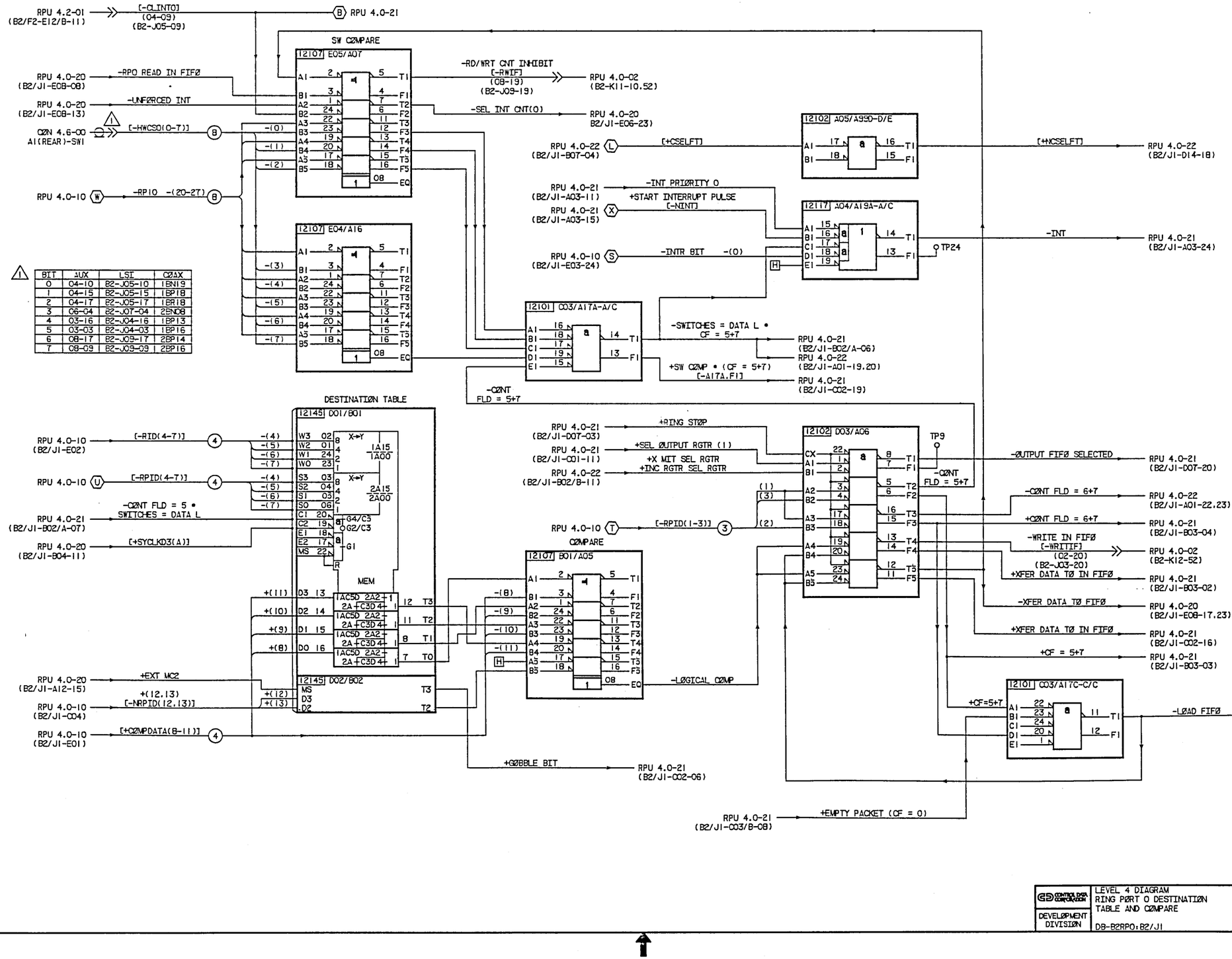
[+C2MPDATA(8-11)] RPU 4.0-11 (B2/J1-D01,B01)

[+RPID(11-19)] RPU 4.0-22 (B2/J1-A06)

[-NRID(20-27)] RPU 4.0-13 (B2/J1-B08,C08)

RPU 4.0-11 (B2/J1-E05) (W) -(20-27)

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM INPUT RING PØRT 0 DATA AND INPUT FIFØ REGISTERS	CAGE IDENT / DRG NO	60461830 / REV A
DEVELOPMENT DIVISION	DB-B2RP0:B2/J1	SHEET RPU 4.0-10	PAGE IV-7-15



CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM RING PORT 0 DESTINATION TABLE AND COMPARE	CODE IDENT DWG NO: 60461830	REV: A
DEVELOPMENT DIVISION	DB-B2RP0:B2/J1	SHEET: RPU 4.0-11	PAGE: IV-7-17

RPU 4.0-01
(B2-H09,H10)

[-MASK(0-15)]

BIT	AUX	LSI
0	12-10	B2-J13-10
1	13-10	B2-J14-10
2	11-25	B2-J12-25
3	11-16	B2-J12-16
4	13-01	B2-J14-01
5	12-24	B2-J13-24
6	12-03	B2-J13-03
7	13-15	B2-J14-15
8	11-01	B2-J12-01
9	12-08	B2-J13-08
10	11-10	B2-J12-10
11	11-06	B2-J12-06
12	11-26	B2-J12-26
13	13-20	B2-J14-20
14	13-26	B2-J14-26
15	13-04	B2-J14-04

SET FLAG DECØDER

12170 B13/A21

+STAT RGTR (0)
-STAT RGTR (0-3)

RPU 4.0-20
(B2/J1-A12)

-STRØBE STAT RGTR (SET)

RPU 4.0-20
(B2/J1-C13-16)

X↔Y CØDER

+(15) [+SETST(15)]

12170 A13/A20

+(7) [+SET ST(7)]

+(0)

16 -(0-15)

-(15) [-MASK(15)] A RPU 4.0-20 (B2/J1-C13-01,23)

FLAG RGTR

12131 A16/A22 BITS 0-2
12131 A17/A23 3-5
12131 B16/A24 6-8
12131 B17/A25 9-11
12131 C16/A26 12-14
12131 C17/A27 BITS 15,X,Y

RPU 4.0-21
(B2/J1-C09-08)

[+WC5]

-(19)

RPU 4.0-21
(B2/J2-D16)

-CLR STAT RGTR (0-5) *

RPU 4.0-21
(B2/J1-C09-07)

[+WC4]

RPU 4.0-21
(B2/J1-A03-08)

+ENABLE RGTR SEL (X)

RPU 4.0-22
(B2/J1-A05/C-13)

+CLR LØCKØUT (X)

FLAG CØMPARE

12118 C14/A32 — TP88 — (F)
12118 B14/A31 — TP90 — (E)
12118 A14/A30 — TP89 — (D)
12118 C15/A35 — TP99 — (C)
12118 B15/A34 — TP98 — (B)
12118 A15/A33 — TP97 — (A)

-TEST (A-F) RPU 4.0-20 (B2/J1-C12/A,B)

-STATUS BITS (0-15) RPU 4.0-20 (B2/J1-B12)

+STATUS BIT 15 RPU 4.0-20 (B2/J1-C13-02)

-RGTR SEL LØCKØUT RPU 4.0-22 (B2/J1-A02-01)

+RGTR SEL LØCKØUT [-NPRRS] (13-8) SHA 4.0-00 (B2-G08-15)

+STATUS BITS (0-15) RPU 4.0-13 (B2/J1-B10)

+(Y) [-NRSLØ] RPU 4.0-20 (B2/J1-C13-20)

CONTROL DATA CORPORATION
DEVELØPMENT DIVISION

LEVEL 4 DIAGRAM
RING PØRT 0 FLAG AND CØMPARE REGISTERS

DB-B2RP0:B2/J1

CODE IDENT 60461830 REV A
SHEET RPU 4.0-12 PAGE IV-7-19

RPU 4.0-22 (B2/J1-D14-13) +LØST PACKET +FF D1

RPU 4.0-20 (Y) -X BAR IN SEL (0)

RPU 4.0-20 (Z) -X BAR IN SEL (1)

RPU 4.0-10 (B2/J1-C05) [+RPID(0-19)] 20

RPU 4.0-20 (B2/J1-B05) [-SYCLKD1 (B,D,E,G,H)] 5

RPU 4.0-10 (B2/J1-D04,D05) [-NRID (20-27)] 8

RPU 4.0-22 (B2/J1-D13-16,13) +LØST PACKET FF(A-C) 3

RPU 4.0-12 (B2/J1-A16) +STATUS BITS (0-15)

RPU 4.0-20 (B2/J1-D15-16) -SEL TØ X BAR 2(1)

RPU 4.0-20 (B2/J1-D15-13) -SEL TØ X BAR 2(0)

LØST PACKET RGTR

12151 A09/D01

12151 B08/D04

12151 C08/D05

12151 B09/D02

12151 A08/D03

RGTR

X BAR DATA

12171 A10/D06

12171 A11/D07

12171 B10/D08

12171 B11/D09

12171 C10/D10

12171 C11/D11

MUX

[-STSR(0-15)] 16 RPU 4.1-13 (B2/J2-B10)

BIT	AUX	LSI
0	09-10	B2-J10-10
1	09-09	B2-J10-09
2	11-04	B2-J12-04
3	08-06	B2-J09-06
4	08-07	B2-J09-07
5	09-25	B2-J10-25
6	09-16	B2-J10-16
7	09-06	B2-J10-06
8	13-16	B2-J14-16
9	08-04	B2-J09-04
10	09-07	B2-J10-07
11	09-24	B2-J10-24
12	11-08	B2-J12-08
13	08-08	B2-J09-08
14	13-25	B2-J14-25
15	09-15	B2-J10-15

7 -(9-15) -(0-8) 9

CONTROL DATA CORPORATION — DEVELOPMENT DIVISION

LEVEL 4 DIAGRAM
RING PORT 0 DATA TO X BAR
LOST PACKET RGTR

DB-B2RP0:B2/J1

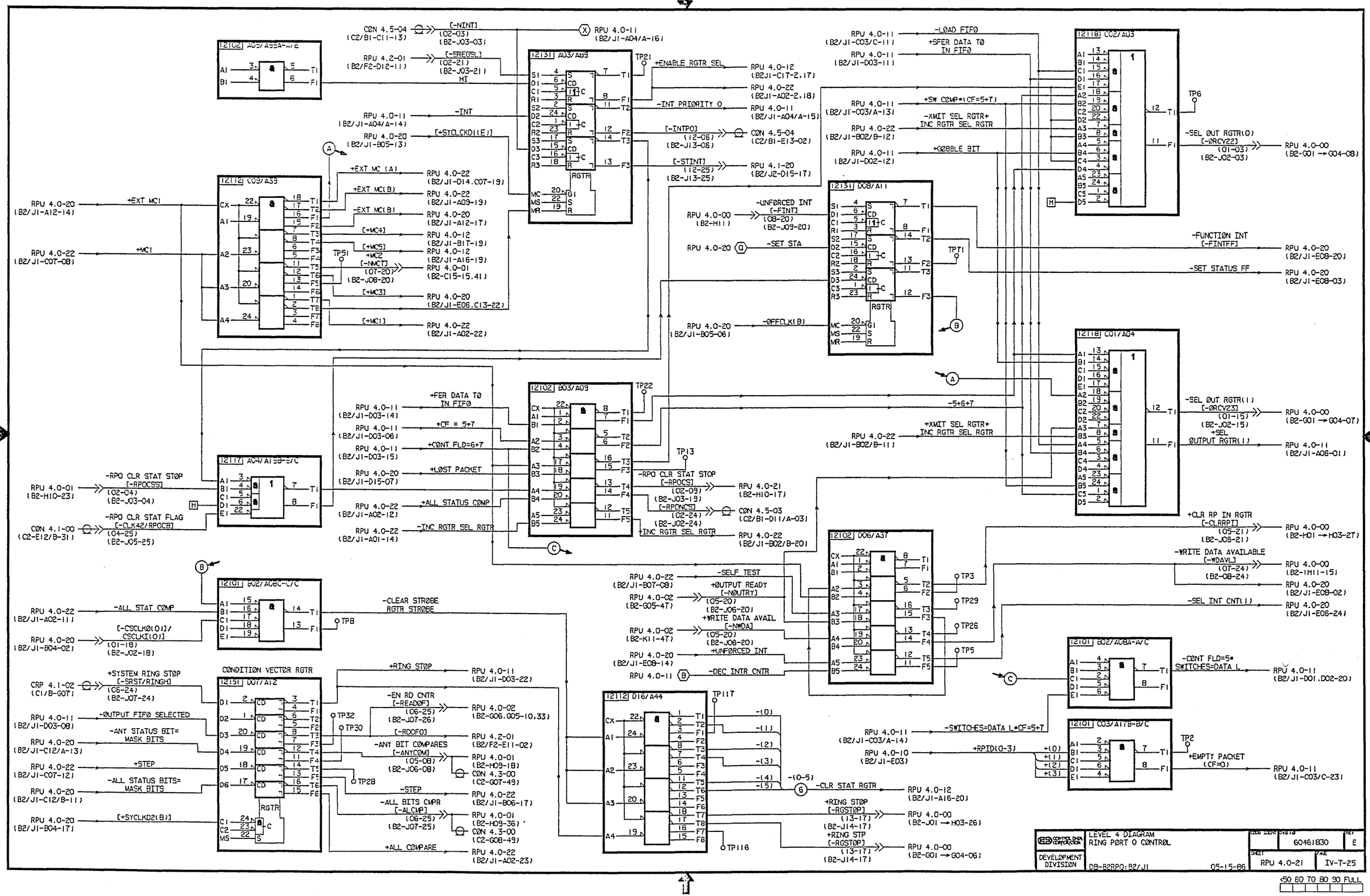
CODE IDENT | DWG NO 60461830 | REV A

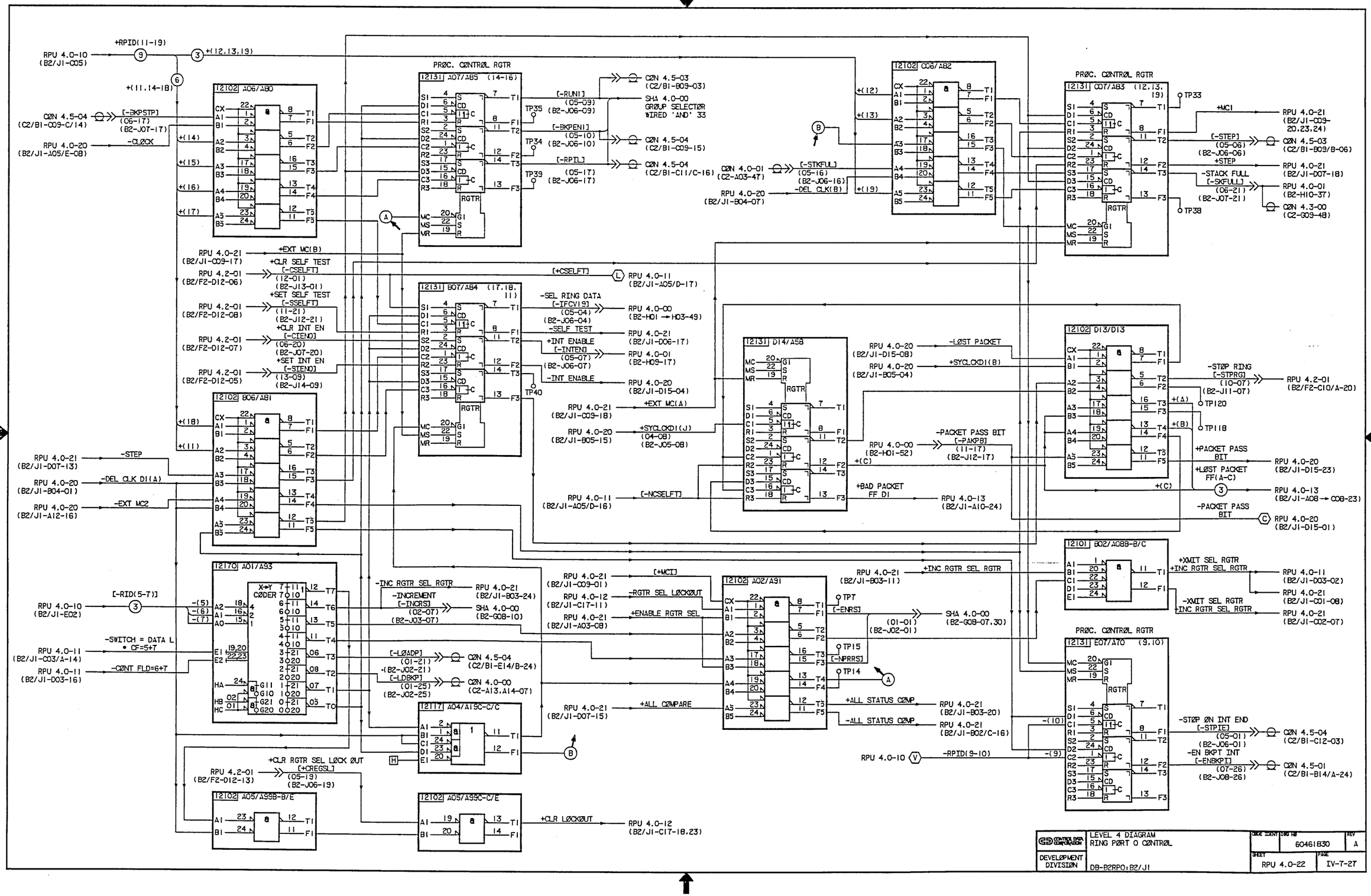
SHEET RPU 4.0-13 | PAGE IV-7-21

CLK 4.1-04 (A2-G14/B-03) [-ØFFCLK(46)] (06-15) (B2-J07-15)
CLK 4.1-03 (A2-H01/A-20) [-ØFFCLK(28)] (03-10) (B2-J04-10)
12112 B04/A10
-DEL CLK DI(A) [-CSCLKØ(0)/ CSCLKI(0)] (03-18) (B2-J04-18)
-DEL CLK(B)
[-DØF2] (03-27) (B2-J04-07)
[+SYCLKD3(A)]
[+SYCLKD2(B)]
TP25
RPU 4.0-22 (B2/JI-B06-18,20)
RPU 4.0-21 (B2/JI-B02/C-17)
C2N 4.5-04 (C2/BI-B13-1,3)
RPU 4.0-22 (B2/JI-C06-20)
RPU 4.1-11 (B2/J2-D01,D02-19)
RPU 4.0-21 (B2/JI-D07-24)
RPU 4.0-12 (B2/JI-A16) [-STATUS(0-15)] 16
12164 B12/A40
-(0) … -(15)
MUX X↔Y
11 TI
RPU 4.2-12 (B2/FI-E13) [-STATA0(0-3)/ STATA(0-3)] 4
BIT | MUX | LSI
0 | 10-19 | B2-J11-19
1 | 10-17 | B2-J11-17
2 | 10-16 | B2-J11-16
3 | 12-04 | B2-J13-04
12102 D15/A95
RPU 4.0-22 (B2/JI-D14-06) -PACKET PASS BIT C
BIAS 0 FRØM THIS PANEL (B2-3-BL01) 1 [-ØFCAFP(0)] (12-19) (B2-J13-19)
RPU 4.0-22 (B2/JI-B07-12) -INT ENABLE
RPU 4.2-11 (B2/FI-D07-13) [-STASEL(0)] (12-15) (B2-J13-15)
RPU 4.2-11 (B2/FI-D07-12) [-STASEL(1)] (12-07) (B2-J13-07)
RPU 4.0-22 (B2/JI-D13-11) +PACKET PASS BIT
1 NU [-ZFCAFP]
-LØST PACKET
+LØST PACKET
+RPO INTR [-INTP2/INTP(3)] (12-20) (B2-J13-20)
-SEL TØ X BAR 2(1)
-SEL TØ X BAR 2(0)
-PACKET PASS BIT ØUT [-PACPB] (12-26) (B2-J13-26)
TP94
TP96
TP95
TP93
RPU 4.0-22 (B2/JI-D13-01)
RPU 4.0-21 (B2/JI-B03-18)
C2N 4.5-04 (C2/BI-E13-24)
RPU 4.0-13 (B2/JI-B10-20)
RPU 4.0-13 (B2/JI-B10-19)
RPU 4.0-00 (B2-G01)
Y RPU 4.0-13 (B2/JI-A10-20)
Z RPU 4.0-13 (B2/JI-A10-19)
12151 A12/A41
RGTR
-(0) … -(3)
+(0)
-STAT RGTR +(0),-(0-3)
5 RPU 4.0-12 (B2/JI-B13,B14)
TP81 TP79 TP80
CRP 4.1-03 (C1/B-G12→G14) +EXTMC [-NMSCLR] (10-15) (B2-J11-15)
+EXT MC1
[-EXTMC] (10-10) (B2-J11-10)
-EXT MC2
+EXT MC2
RPU 4.0-21 (B2/JI-C09-22)
RPU 4.1-21 (B2/J2-C09-24)
RPU 4.0-22 (B2/JI-B06-19)
RPU 4.0-11 (B2/JI-B02-22)
RPU 4.0-21 (B2/JI-C09-15) -EXT MC(B)
3
12112 B05/A96
2 TP27
CLK 4.1-03 (A2-B01/A-31) [-SYSCLK(15)] (04-08) (B2-J05-08)
[-SYCLKDI(B)]
[-ØFFCLK(B)]
[+SYCLKDI(E)]
[-SYCLOCKDI(B,C,E,G,H)]
[+SYCLKDI(J)]
-(B) -(C) -(E) -(G) -(H)
RPU 4.0-22 (B2/JI-D13-02)
RPU 4.0-21 (B2/JI-D08-20)
RPU 4.0-21 (B2/JI-A03-20)
RPU 4.0-13 (B2/JI-B08-24)
RPU 4.0-22 (B2/JI-D14-05)
12102 A05/A93E-E/E
-CLØCK
RPU 4.0-22 (B2/JI-A06-02)
12136 E06/A97
H
TC
16CNTR/ SR-4
-SEL INT CNT(1)
-SEL INT CNT(0)
[+MC3]
RPU 4.0-21 (B2/JI-D06-12)
RPU 4.0-11 (B2/JI-E05-07)
RPU 4.0-21 (B2/JI-C09-12)
12101 C12/A28C-C/C
TP76
FUNTIØN | MØDE | SO | SI
NØTHING | HØLD | 0 | 0
STØRE INTR | CNT DØWN | 1 | 0
DELETE INTR | CNT UP | 1 | 1
B
RPU 4.0-12 (B2/JI-C17-08) A
RPU 4.0-12 (B2/JI-C17-08) B +STATUS BIT 15
RPU 4.0-00 (B2-H11-01) -SET STATUS [-SETSTA]
RPU 4.0-00 RPØ ØUTPUT REGISTER (B2-J10-08) B [-SHREGI(15)] (09-08)
RPU 4.0-12 (B2/JI-C17-13) [-NRSLØ] G RPU 4.0-21
SHADØW LØCKØUT GATE
12102 C13/A29
TP82 TP85 TP84
+RPØ STATUS SET STØP [-RPOSSS] (10-09) (B2-J11-09)
RPU 4.2-01 (B2/F2-C08-19)
-STRØBE STAT RGTR(SET)
RPU 4.0-12 (B2/JI-B13-19,20)
-RGTR SEL BLK [-BREGSL(15)/ SHREGI(15)] (07-16) (B2-J08-16)
RPU 4.0-00 (B2-G04-12)
12101 C12/A28A-A/C
TP92
-ANY STATUS BIT = MASK BITS
RPU 4.0-21 (B2/JI-D07-19)
RPU 4.0-12 (B2/JI-A15) [-TEST(A-F)]
12101 C12/A28B-B/C
TP77
-ALL STATUS BITS = MASK BITS
RPU 4.0-21 (B2/JI-D07-17)
RPU 4.2-02 (B2/F2-E10/A-07) [-RPOGIF] (06-07) (B2-J07-07)
12102 E08/A38
-WRITE DATA AVAILABLE
-SET STATUS FF
-X FER DATA TØ FIFØ
-FUNCTIØN INT [-FINTFF]
RPU 4.0-21 (B2/JI-D06-14)
RPU 4.0-21 (B2/JI-D08-14)
RPU 4.0-11 (B2/JI-D03-12)
RPU 4.0-21 (B2/JI-D08-07)
-RPO READ IN FIFØ
-RD IN FIFØ [-RDIF] (08-21) (B2-J09-21)
-IN FIFØ WE1
-UNFØRCED INT
+UNFØRCED INT
-IN FIFØ WE2
TP37 TP42 TP72 TP41
RPU 4.0-11 (B2/JI-E05-03)
RPU 4.0-02 (B2-K11,K12-10,33)
RPU 4.0-10 (B2/JI-D09-20)
RPU 4.0-11 (B2/JI-E05-01)
RPU 4.0-21 (B2/JI-D06-23)
RPU 4.0-10 (B2/JI-E09-20)

NØTES:
1. ØFCAFP BIAS ZERØ. ZFCAFP BIAS ØNE TØ DISABLE BAD PACKET DETECT. BAD PACKET DETECT IS DØNE EXCLUSIVELY IN THE CRP.
2. ALL LINES FRØM B05 (EXCEPT ØUTPUT F7) MUST STAY WITHIN A 2 INCH RANGE.
3. MAKE B05. F3 SHØRT

CONTROL DATA CORPORATION — DEVELØPMENT DIVISIØN
LEVEL 4 DIAGRAM
STATUS
RING PØRT 0
DB-B2RP0:B2/J1
CAGE IDENT | DRG NO | REV
60461830 | A
SHEET | PAGE
RPU 4.0-20 | IV-7-23


12102 A03/A05-A/C
12131 A03/A09
12118 C02/A03
12112 C03/A39
12131 D08/A11
12118 C07/A04
12102 B03/A09
12117 A04/A15-B/C
12101 B02/A08-C/C
12102 D06/A31
12101 B02/A08A-A/C
12101 C03/A17B-B/C
12151 D07/A12
12112 D16/A44
CONDITION VECTOR RGTR
RGTR
RPU 4.0-20 (B2/J1-A12-14)
+EXT MC!
RPU 4.0-22 (B2/J1-C07-08)
+MC!
C2N 4.5-04 (C2/B1-C11-13)
[-NINT] (02-03) (B2-J03-03)
RPU 4.0-11 (B2/J1-A04/A-16)
RPU 4.2-01 (B2/F2-D12-11)
[-SREGSL] (02-21) (B2-J03-21) HI
-INT
RPU 4.0-20 (B2/J1-B05-13)
[+SYCLCKD1(E)]
+ENABLE RGTR SEL
RPU 4.0-12 (B2J1-C17-2,17)
RPU 4.0-22 (B2J1-A02-2,18)
-INT PRIORITY 0
RPU 4.0-11 (B2/J1-A04/A-15)
[-INTPO] (12-08) (B2-J13-08)
C2N 4.5-04 (C2/B1-E13-02)
[-STINT] (12-25) (B2-J13-25)
RPU 4.1-20 (B2/J2-D15-17)
+EXT MC (A)
RPU 4.0-22 (B2/J1-D14.C07-19)
+EXT MC(B)
RPU 4.0-22 (B2/J1-A09-19)
-EXT MC(B)
RPU 4.0-20 (B2/J1-A12-17)
[+MC4]
RPU 4.0-12 (B2/J1-B1T-19)
[+MC5]
+MC2
RPU 4.0-12 (B2/J1-A16-19)
[-NMCT] (07-20) (B2-J08-20)
RPU 4.0-01 (B2-C15-15.41)
[+MC3]
RPU 4.0-20 (B2/J1-E06.C13-22)
[+MC1]
RPU 4.0-22 (B2/J1-A02-22)
TP51
TP21
TP22
TP13
TP6
TP1
TP3
TP29
TP26
TP5
TP2
TP8
TP32
TP30
TP28
TP117
TP118
RPU 4.0-11 (B2/J1-C03/C-11)
-LØAD FIFØ
+SFER DATA TØ IN FIFØ
RPU 4.0-11 (B2/J1-D03-11)
RPU 4.0-11 (B2/J1-C03/A-13)
+SW C2MP*(CF=5+7)
-XMIT SEL RGTR+ INC RGTR SEL RGTR
RPU 4.0-22 (B2/J1-B02/B-12)
RPU 4.0-11 (B2/J1-D02-12)
+GØBBLE BIT
-SEL ØUT RGTR(0) [-ØRCV22] (01-03) (B2-J02-03)
RPU 4.0-00 (B2-G01 → G04-08)
-FUNCTIØN INT [-FINTFF]
RPU 4.0-20 (B2/J1-EC8-20)
-SET STATUS FF
RPU 4.0-20 (B2/J1-EC8-03)
RPU 4.0-00 (B2-H11) -UNFØRCED INT [-FINT] (08-20) (B2-J09-20)
RPU 4.0-20 -SET STA
RPU 4.0-20 (B2/J1-B05-06) -ØFFCLK(B)
-SEL ØUT RGTR(1) [-ØRCV23] (01-15) (B2-J02-15)
RPU 4.0-00 (B2-G01 → G04-07)
+SEL ØUTPUT RGTR(1)
RPU 4.0-11 (B2/J1-A06-01)
-5+6+7
RPU 4.0-22 (B2/J1-B02/B-11)
+XMIT SEL RGTR+ INC RGTR SEL RGTR
+CLR RP IN RGTR [-CLRRP] (05-21) (B2-J06-21)
RPU 4.0-00 (B2-H01 → H03-27)
-WRITE DATA AVAILABLE [-WDAVL] (07-24) (B2-08-24)
RPU 4.0-00 (B2-1H11-15)
RPU 4.0-20 (B2/J1-EC8-02)
-SEL INT CNT(1)
RPU 4.0-20 (B2/J1-E06-24)
RPU 4.0-01 (B2-H10-23) -RPO CLR STAT STØP [-RPOCSS] (02-04) (B2-J03-04)
C2N 4.1-00 (C2-E12/B-31) -RPO CLR STAT FLAG [-CLK42/RPOCB] (04-25) (B2-J05-25)
RPU 4.0-11 (B2/J1-D03-14) +FER DATA TØ IN FIFØ
RPU 4.0-11 (B2/J1-D03-06) +CF = 5+7
RPU 4.0-11 (B2/J1-D03-15) +CØNT FLD=6+7
RPU 4.0-20 (B2/J1-D15-07) +LØST PACKET
RPU 4.0-22 (B2/J1-A02-12) +ALL STATUS CØMP
RPU 4.0-22 (B2/J1-A01-14) -INC RGTR SEL RGTR
-RPO CLR STAT STOP [-RPOCS] (02-09) (B2-J03-19)
[-RPONCS] (02-24) (B2-J02-24)
+INC RGTR SEL RGTR
RPU 4.0-21 (B2-H10-17)
C2N 4.5-03 (C2/B1-D11/A-03)
RPU 4.0-22 (B2/J1-B02/B-20)
RPU 4.0-22 (B2/J1-B07-08) -SELF TEST
RPU 4.0-02 (B2-G05-47) +ØUTPUT READY [-NØUTRY] (05-20) (B2-J06-20)
RPU 4.0-02 (B2-K11-47) +WRITE DATA AVAIL [-NWDA] (05-20) (B2-J06-20)
RPU 4.0-20 (B2/J1-EC8-14) +UNFØRCED INT
RPU 4.0-11 -DEC INTR CNTR
-CLEAR STRØBE RGTR STRØBE
RPU 4.0-22 (B2/J1-A02-11) -ALL STAT CØMP
RPU 4.0-20 (B2/J1-B04-02) [-CSCLKØ(01)/CSCLKI(01)] (01-18) (B2-J02-18)
CRP 4.1-02 (C1/B-G07) +SYSTEM RING STØP [-SRST/RINGH] (06-24) (B2-J07-24)
RPU 4.0-11 (B2/J1-D03-08) -ØUTPUT FIFØ SELECTED
RPU 4.0-20 (B2/J1-C12/A-13) -ANY STATUS BIT= MASK BITS
RPU 4.0-22 (B2/J1-C07-12) +STEP
RPU 4.0-20 (B2/J1-C12/B-11) -ALL STATUS BITS= MASK BITS
RPU 4.0-20 (B2/J1-B04-17) [+SYCLKD2(B)]
+RING STØP RPU 4.0-11 (B2/J1-D03-22)
-EN RD CNTR [-READØF] (06-25) (B2-J07-26) RPU 4.0-02 (B2-G06.G05-10,33)
[-RDOFO] RPU 4.2-01 (B2/F2-E11-02)
-ANY BIT CØMPARES [-ANYCØM] (05-08) (B2-J06-08) RPU 4.0-01 (B2-H09-18) C2N 4.3-00 (C2-G07-49)
-STEP RPU 4.0-22 (B2/J1-B06-17)
-ALL BITS CMPR [-ALCMP] (06-25) (B2-J07-25) RPU 4.0-01 (B2-H09-36) C2N 4.3-00 (C2-G08-49)
+ALL CØMPARE RPU 4.0-22 (B2/J1-A02-23)
-(0) -(1) -(2) -(3) -(4) -(5) -(0-5) -CLR STAT RGTR RPU 4.0-12 (B2/J1-A16-20)
+RING STØP [-RGSTØP] (13-17) (B2-J14-17) RPU 4.0-00 (B2-J01 → H03-26)
+RING STP [-RGSTØP] (13-17) (B2-J14-17) RPU 4.0-00 (B2-G01 → G04-06)
RPU 4.0-11 (B2/J1-C03/A-14) -SWITCHES=DATA L•CF=5+7
RPU 4.0-10 (B2/J1-E03) +RPID(0-3) +(0) +(1) +(2) +(3)
-CØNT FLD=5• SWITCHES=DATA L RPU 4.0-11 (B2/J1-D01.D02-20)
+EMPTY PACKET (CF=0) RPU 4.0-11 (B2/J1-C03/C-23)
LEVEL 4 DIAGRAM
RING PØRT 0 CØNTRØL
DEVELOPMENT DIVISION
DB-B2RPO:B2/J1
05-15-86
60461830
E
RPU 4.0-21
IV-T-25
50 60 70 80 90 FULL


+RPID(11-19)
RPU 4.0-10 (B2/J1-C05)
+(12,13,19)
+(11,14-18)
C2N 4.5-04 (C2/B1-C09-C/14)
[-BKPSTP] (06-17) (B2-J07-17)
-CLOCK
RPU 4.0-20 (B2/J1-A05/E-08)
12102 A06/A80
PROC. CONTROL RGTR
12131 A07/A85 (14-16)
[-RUN1] (05-09) (B2-J06-09)
[-BKPEN1] (05-10) (B2-J06-10)
[-RPIL] (05-17) (B2-J06-17)
TP35
TP34
TP39
C2N 4.5-03 (C2/B1-B09-03)
SHA 4.0-00 GROUP SELECTOR WIRED 'AND' 33
C2N 4.5-04 (C2/B1-C09-15)
C2N 4.5-04 (C2/B1-C11/C-16)
12102 CC6/A82
+(12)
+(13)
+(19)
C2N 4.0-01 (C2-A03-47)
[-STKFULL] (05-16) (B2-J06-16)
-DEL CLK(B)
RPU 4.0-20 (B2/J1-B04-07)
PROC. CONTROL RGTR
12131 CC7/A83 (12,13,19)
TP33
TP38
+MC1
RPU 4.0-21 (B2/J1-C09-20,23,24)
[-STEP] (05-06) (B2-J06-06)
C2N 4.5-03 (C2/B1-B09/B-06)
+STEP
RPU 4.0-21 (B2/J1-D07-18)
-STACK FULL
[-SKFULL] (06-21) (B2-J07-21)
RPU 4.0-01 (B2-H10-37)
C2N 4.3-00 (C2-G09-48)
RPU 4.0-21 (B2/J1-C09-17)
+EXT MC(B)
+CLR SELF TEST
RPU 4.2-01 (B2/F2-D12-06)
[-CSELFT] (12-01) (B2-J13-01)
+SET SELF TEST
RPU 4.2-01 (B2/F2-D12-08)
[-SSELFT] (11-21) (B2-J12-21)
+CLR INT EN
RPU 4.2-01 (B2/F2-D12-07)
[-CIENO] (06-20) (B2-J07-20)
+SET INT EN
RPU 4.2-01 (B2/F2-D12-05)
[-SIENO] (13-09) (B2-J14-09)
[+CSELFT]
RPU 4.0-11 (B2/J1-A05/D-17)
12131 B07/A84 (17,18,11)
-SEL RING DATA
[-IFCV19] (05-04) (B2-J06-04)
RPU 4.0-00 (B2-H01 → H03-49)
-SELF TEST
RPU 4.0-21 (B2/J1-D06-17)
+INT ENABLE
[-INTEN] (05-07) (B2-J06-07)
RPU 4.0-01 (B2-H09-17)
-INT ENABLE
RPU 4.0-20 (B2/J1-D15-04)
TP40
RPU 4.0-21 (B2/J1-C09-18)
+EXT MC(A)
RPU 4.0-20 (B2/J1-B05-15)
+SYCLOCK1(J) (04-08) (B2-J05-08)
RPU 4.0-11 (B2/J1-A05/D-16)
[-NCSELFT]
12131 D14/A58
RPU 4.0-20 (B2/J1-D15-08)
RPU 4.0-20 (B2/J1-B05-04)
-LOST PACKET
+SYCLOCK1(B)
RPU 4.0-00 (B2-H01-52)
+(C)
-PACKET PASS BIT
[-PAKPB] (11-17) (B2-J12-17)
+BAD PACKET FF D1
RPU 4.0-13 (B2/J1-A10-24)
12102 D13/D13
-STOP RING
[-STPRG] (10-07) (B2-J11-07)
RPU 4.2-01 (B2/F2-C10/A-20)
TP120
TP118
+(A)
+(B)
+PACKET PASS BIT
RPU 4.0-20 (B2/J1-D15-23)
+LOST PACKET FF(A-C)
RPU 4.0-13 (B2/J1-A08 → C08-23)
-PACKET PASS BIT
RPU 4.0-20 (B2/J1-D15-01)
RPU 4.0-21 (B2/J1-D07-13)
-STEP
RPU 4.0-20 (B2/J1-B04-01)
-DEL CLK DI(A)
RPU 4.0-20 (B2/J1-A12-16)
-EXT MC2
12102 B06/A81
+(18)
+(11)
12170 A01/A93
[-RID(5-7)]
RPU 4.0-10 (B2/J1-E02)
-(5)
-(6)
-(7)
-SWITCH = DATA L • CF=5+7
RPU 4.0-11 (B2/J1-C03/A-14)
-CONT FLD=6+7
RPU 4.0-11 (B2/J1-D03-16)
X→Y CODER
-INC RGTR SEL RGTR
-INCREMENT
[-INCRS] (02-07) (B2-J03-07)
RPU 4.0-21 (B2/J1-B03-24)
SHA 4.0-00 (B2-G08-10)
[-LOADP] (01-21) (B2-J02-21)
C2N 4.5-04 (C2/B1-E14/B-24)
[-LDBKP] (01-25) (B2-J02-25)
C2N 4.0-00 (C2-A13,A14-07)
RPU 4.0-21 (B2/J1-D07-15)
+ALL COMPARE
12117 A04/A19C-C/C
+CLR RGTR SEL LOCK OUT
RPU 4.2-01 (B2/F2-D12-13)
[+CREGSL] (05-19) (B2-J06-19)
12102 A05/A99B-B/E
12102 A05/A99C-C/E
+CLR LOCKOUT
RPU 4.0-12 (B2/J1-C17-18,23)
RPU 4.0-21 (B2/J1-C09-01)
[+MC1]
RPU 4.0-12 (B2/J1-C17-11)
-RGTR SEL LOCKOUT
RPU 4.0-21 (B2/J1-A03-08)
+ENABLE RGTR SEL
12102 A02/A91
RPU 4.0-21 (B2/J1-B03-11)
+INC RGTR SEL RGTR
TP15
TP14
[-ENRS]
(01-01) (B2-J02-01)
SHA 4.0-00 (B2-G08-07,30)
[-NPRRS]
+ALL STATUS COMP
RPU 4.0-21 (B2/J1-B03-20)
-ALL STATUS COMP
RPU 4.0-21 (B2/J1-B02/C-16)
RPU 4.0-10 (V)
-RPID(9-10)
12101 B02/A08B-B/C
+XMIT SEL RGTR
+INC RGTR SEL RGTR
RPU 4.0-11 (B2/J1-D03-02)
RPU 4.0-21 (B2/J1-C01-08)
-XMIT SEL RGTR
+INC RGTR SEL RGTR
RPU 4.0-21 (B2/J1-C02-07)
PROC. CONTROL RGTR
12131 E07/A70 (9,10)
-STOP ON INT END
[-STPIE] (05-01) (B2-J06-01)
C2N 4.5-04 (C2/B1-C12-03)
-EN BKPT INT
[-ENBKPI] (07-26) (B2-J08-26)
C2N 4.5-01 (C2/B1-B14/A-24)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
RING PORT 0 CONTROL
DB-B2RP0:B2/J1
CODE IDENT
DWG NO
60461830
REV
A
SHEET
RPU 4.0-22
PAGE
IV-7-27

CABLE INPUT
2W004

BITS	CABLE
00	A
01	B
02	C
03	D
04	E
05	F
06	H
07	J
08	K
09	L
10	M
11	N
12	P
13	R
14	S
15	T
16	U
17	V
18	W
19	X
20	Y
21	Z
22	AA
23	BB
24	CC
25	DD
26	EE
27	FF
28	HH

RPI RING INPUT REGISTERS

CLK 4.1-03 (A2-B01-32) [-SYSCLK(11)] [-RPIPPI.]
RPI INPUT CABLE [-RPIINP(0-27)] -(0-27)
RPU 4.2-03 (B2/F2-E04) [-DØFI(0-27)]
-SEL RING DATA [-ICV15]
RPU 4.1-22 (B2/J2-C07-07) +RING STØP [-RSTØPI]
RPU 4.1-22 (B2/J2-D16-18) CLR RPIN RGTR [-CLRRPI]
RPU 4.1-22 (B2/J2-E07-08)
CLK 4.1-03 (A2-B01/A-23) [-SYSCLK(9)]

12SD H15/5011 BITS P,.....8-11
12SD H13/5013 0-7, 12-15
12SD H14/5014 BITS 16-27
CLOCK
A/C
B/D
S 49
F(0) 26
F(4) 27
CLCK 03
CD
RGTR
G2
G1
X↔Y
1 I14C

[-IDRI(0-27)] RPU 4.1-10 (B2/J2-E03)
-PACKET PASS BIT [-PAKPBI] RPU 4.1-20 (B2/J2-E15/C.D15-19)

-PACKET PASS BIT ØUT [-PACPBI]
RPU 4.1-20 (B2/J2-D15-11) -(X)
CLK 4.1-01 (A2-B02-05) [-SYSCLK(7)]
-(12-19, 8-11)
RPU 4.1-10 (B2/J2-E01) [-RIDI(0-27)] -(X)
-(X.12-19,8-11) -(X.0-11)
-(X.0-27)
-(X)

RPI RING ØUTPUT REGISTERS

12CB G14/1B32 BITS 0-7
12CB G15/1B31 ..,X, 8-11
12CB G13/1B33 12-19
12CB G12/1B34 BITS 20-27
A( ) B( ) C( ) D( )
C4D C5D C6D C7D
Z( )
RGTR
CLCKEN 06
CLCK 03
S(0) 08
S(1) 07
1 I02

-(X.0-27) [-RPIPPØ, RPIØUT(0-27)] RPI ØUTPUT CABLE

+RING STØP [-RSTPI] RPU 4.1-22 (B2/J2-D16-17)
CLK 4.1-03 (A2-B01/A-30) [-SYSCLK(14)] -SEL ØUT RGTR (0) [-ØCV22]
RPU 4.1-21 (B2/J2-C02-11) -SEL ØUT RGTR (1) [-ØCV23]
RPU 4.1-21 (B2/J2-D02-12)

CABLE ØUTPUT
2W003

BITS	CABLE
00	A
01	B
02	C
03	D
04	E
05	F
06	H
07	J
08	K
09	L
10	M
11	N
12	P
13	R
14	S
15	T
16	U
17	V
18	W
19	X
20	Y
21	Z
22	AA
23	BB
24	CC
25	DD
26	EE
27	FF
28	HH

INPUT CØNTRØL HØLDING RGTR

RPU 4.1-10 (B2/J2-E10.E11) [-IFOI(0-7)]
CLK 4.1-03 (A2-B01/B-01) [-ØFFCLK(6)]
RPU 4.2-02 (B2/F2-D10/B-11) [-RPIIFG]
-WRITE DATA AVAILABLE [-WDAVL1]
RPU 4.1-21 (B2/J2-B03-11)
RPU 4.1-02 (B2-K06-51) [-NWDA1]

12CD H05/1D17
PARA 48 A(0-7)
PARB 43 B(0-7)
CLCK 03
EN 07
SEL(0) 30
SEL(1) 15
CINA 36
CINB 19
CINC 12
CIND 28
PMIL 10
DECR 33
CZERØ 22
C1D C2D
256 CNTR WITH PARITY TØGGLE
X↔Y
Σ
27 CØUT
29 PARI
Z(0-7)
49 BGTR
50 BGTRL
51 BEQR
47 BEQRL
G1 G2 G3 G4

NØTES:
1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

1 I05

-UNFØRCED INT [-FINTI]
-(0) RPU 4.1-21 (B2/J2-D08-06)
-(1) [-ASTWRI] RPU 4.2-11 (B2/F1-D07-03.01)
-(2) [-SETSTI] RPU 4.1-20 (B2/J2-C13-04)
-(3) [-ENDMSI] RPU 4.2-11 (B2/F1-E07)
-(4-7) -(0-3) [-STATUSI(0-3)] RPU 4.2-11 (B2/F1-E06)

FIFØ DATA

RPU 4.1-10 (B2/J2-D09) [-IFDI(0-15)]
CLK 4.1-05 (A2-C01/B-01) [-ØFFCLK(10)]

12CE K07/1E13
A( ) B( ) C( ) D( )
CD
RGTR
X↔Y
CLCK 03
V20 38
V23 16
V19 42
V22 19
NØTE: UNDEFINED -3 I04

[-ASTDI(0-15)] RPU 4.2-11 (B2/F1-A07)

NØTES:

1

BIT	A/C	B/D	Y/Z
P,0,16	07	44	52
,1,17	09	08	50
,2,18	11	10	01
,3,19	18	16	30
,4,20	20	17	31
,5,21	45	19	29
,6,22	46	48	4
,7,23	42	43	05
8,12,24	37	41	06
9,13,25	35	38	24
10,14,26	34	36	21
11,15,27	33	32	22

2

BIT	A	B	Z
0	45	44	31
1	42	34	26
2	38	37	23
3	35	32	25
4	20	17	24
5	18	01	21
6	16	09	05
7	11	06	04

3

BIT	A/B	C/D
0	45	49
1	46	50
2	44	47
3	43	48
4	34	29
5	33	30
6	35	31
7	36	32
8	12	07
9	08	06
10	41	05
11	09	04
12	17	22
13	15	21
14	20	24
15	37	23

4

BIT	A	B	C	D	Z
0, ,12,20	34	35	32	48	30
1, ,13,21	36	33	31	47	49
2, ,14,22	37	38	44	46	29
3,X,15,23	42	41	45	43	50
4,8,16,24	20	17	27	23	28
5,9,17,25	18	15	25	16	04
6,10,18,26	21	24	19	22	26
7,11,19,27	12	11	10	02	05

5 INPUT FRØM FLØATING PØINT UNIT ØPTIØN IF INSTALLED.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM RING PØRT I RING PØRT I/Ø REGISTERS	CODE IDENTIFICATION NO 60461830	REV A
DEVELØPMENT DIVISIØN	DB-B2RPU:B2	SHEET RPU 4.1-00	PAGE IV-T-29

CONTROL REGISTER

12DB G09/8811

-RING PORT 1 DC FIELD (0-11) [-FID(0-8)15/ RPICTL(0-11)]

CON 4.1-00 (C2-E01/A→E15/A-51)

CLK 4.1-03 (A2-B01/B-08)

CON 4.5-21 (C2/C1-E13-07)

CON 4.5-31 (C2/C2-E05-06)

[-ØFFCLK(7)]

[-ITDØNE(11)]

[-NINTR(2)]

-(3,4, 6,7)

-(0-11)

-(0-2, 5.8-11)

MASTER SLAVE

A(0-3) 17,18, 36,37

B(0-7) 16,15, 11,12, 44,38, 41,42

C1 3

EN1 9

XFR 8

GØ1 35

ENS 10

C2 2

EN2 46

GØ2 43

23,27,30,33

26,29,31,34

D(0-3) C(0-3)

E(0-3) 24,25, 29,32

F(0-7) 22,21,6, 4,51,49, 47,45

G(0-7) 19,20,7, 5,1,52, 50,48

-(3,4,6,7)

-(3,4,6,7)

-(0-2,5,8,11)

-(0-2,5,8,11)

[-CFINB(3,4,7)]

-(3)

-(4)

-(7)

RPU 4.2-01 (B2/F2-E07/A-06)

RPU 4.2-01 (B2/F2-C08-02)

RPU 4.2-01 (B2/F2-E07/C-18)

[-ØFCI(0-11)]

RPU 4.2-03 (B2/F2-D04)

-LOAD RING PORT 1 CONTROL RGTR [-GØU(15)/GØRPI]

CON 4.1-00 (C2-F09-19)

-SHADOW ROW SELECT 1 [-URS1(9)]

SHA 4.0-01 (B2-A06/B-34)

-CONTROL RGTR SHADOW [-*AND21(0-11)]

RPU 4.3-00 SHADOW WIRED 'AND' 21

+INT ENABLE [-INTEN1]

-ANY BIT COMPARES [-ANYCM1]

-ALL BITS COMPARE [-ALCMP1]

RPU 4.1-22 (B2/J2-C07-11)

RPU 4.1-21 (B2/J2-D07-12)

RPU 4.1-21 (B2/J2-D07-16)

-(0)

-(1)

-(2)

RPU 4.1-02 (B2-G11-49)

[-NØFFL1]

-(3)

-(0-3)

-SHADOW ROW SELECT 3 [-URS3(9)]

RPU 4.0-01 (G)

CLK 4.1-05 (A2-C01/B-46)

[-ØFFCLK(8)]

-(3)

-(1)

-(2)

-(0)

-(3)

-CLR STAT STØP [-RP1CS]

RPU 4.1-21 (B2/J2-B03-13)

CLK 4.1-03 (A2-B01/A-21)

[-SYSCLK(12)]

-(0-3) -(4-7)

STATUS AND MASK REGISTERS

12DB H06/8812

A(0-3)

GO1

C2

STATUS BITS 0-3

MASK BITS 0-7

12DB H07/8813

STATUS BITS 4-7

MASK BITS 8-15

-RP1 CLR STAT STØP [-RP1CSS]

RPU 4.1-21 (B2/J2-A04/B-04)

-(4)

-(5,6)

-(5) [-ØFFUL1]

-(6) [-ØFFUL1]

CON 4.3-00 (C2-H06-21)

RPU 4.2-01 (B2/F2-B11/B-24)

-STATUS RGTR SHADOW [-WAND21(7,5,6,4)]

-(0-3)

RPU 4.3-00 SHADOW WIRED 'AND' 21

-(0-15)

[-MSK1(0-15)]

RPU 4.1-12 (B2/J2-A16)

-MASK RGTR SHADOW [-WAND21(0-15)]

-(0-15)

RPU 4.3-00 SHADOW WIRED 'AND' 21

RPU 4.2-01 (B2/F2-E07/B-11)

[-GTEMK1]

CLK 4.1-05 (A2-C01/B-51)

[-ØFFCLK(9)]

-SHADOW ROW SELECT 2 [-URS2(9)]

SHA 4.0-02 (B2-A06/B-51)

-(0-15)

XBAR REGISTER

12CE H04/1E18

-X BAR TO RP1 [-RP1XBR(0-15)/RP1XBI(0-15)]

CON 4.2-00 X BAR FANOUT (D2-F09/A05)

CLK 4.1-03 (A2-B01/B-06)

[-SYSCLK(19)]

CON 4.1-00 (C2-E12/B-32)

[-CLK43/RP1CA]

[-XBREGI(0-15)]

NOTE: ⚠ UNDEFINED

B RPU 4.2-01 (B2/F2-E07-05)

NOTE: ⚠

BIT	A/B	C/D
0	45	49
1	46	50
2	44	47
3	43	48
4	34	29
5	33	30
6	35	31
7	36	32
8	12	07
9	08	06
10	41	05
11	09	04
12	17	22
13	15	21
14	20	24
15	37	23

CONTROL DATA CORPORATION

LEVEL 4 DIAGRAM
RING PORT 1 CONTROL, STATUS, AND MASK

DEVELOPMENT DIVISION

DB-B2RPU:B2

CODE IDENT | DWG NO: 60461830 | REV: A

SHEET: RPU 4.1-01 | PAGE: IV-7-31

INPUT FIFØ WRITE/READ CØUNTER

12CD K05/1D15

PARA 48 C1D
PARB 43 C2D
A(0-7) A(0) A(3) Z4 Z3 C1D
B(0-7) B(0) B(3) A(4) A(7) Z2 Z1 B(4) B(7) C2D
DUAL 16 CNTRS WITH PARITY TØGGLE
X=Y
CLCK 03
EN 07
SEL(0) 30
SEL(1) 15
PMBØIU 32
PMIL 10
DECR 33
CZERØ 22
29 PARZ
Z(0-7)
Z(0) Z(3) Z(4) Z(7)
N N+7
Σ A B 128 16 A>B, A=B
49 BGTR
50 BGTRL
51 BEQR
47 BEQRL
G3 G2 G1
7 6 5 4 C2 C1 R Z4 Z3 Z2 Z1

NØTES:
1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. THE DATA BITS FRØM EACH TRUNK SEPARATE, 4 BITS TØ EACH CØUNTER. THE SELECTED PARITY BIT STILL REPRESENTS THE PARITY FØR ALL 8 SELECTED DATA BITS. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF THE 8 DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

5/05

-(0-7) -(0-3) -WRITE ADRS CNT [-WIFA1(0-3)] → RPU 4.1-10 (B2/J2-D12)
-(4-7) -READ ADRS CNT [-RIFA1(0-3)] → RPU 4.1-10 (B2/J2-E12)

CLK 4.1-03 (A2-B01/A-29) [-SYSCLK(10)]
RPU 4.0-01 (B2-C15/A-34) [-MCF(11)]
RPU 4.1-11 (B2/J2-D03-13) [-WRIF1]
RPU 4.1-20 (B2/J2-E08-08) [-RDIF1]

ØUTPUT FIFØ WRITE/READ CØUNTER

12CD G10/1D11

PARA 48 C1D
PARB 43 C2D
A(0-7) A(0) A(3) Z4 Z3 C1D
B(0-7) B(0) B(3) A(4) A(7) Z2 Z1 B(4) B(7) C2D
DUAL 16 CNTRS WITH PARITY TØGGLE
X=Y
CLCK 03
EN 07
SEL(0) 30
SEL(1) 15
PMBØIU 52
PMIL 10
DECR 33
CZERØ 22
29 PARZ
Z(0-7)
Z(0) Z(3) Z(4) Z(7)
N N+7
Σ A B 128 16 A>B, A=B
49 BGTR
50 BGTRL
51 BEQR
47 BEQRL
G3 G2 G1
7 6 5 4 C2 C1 R Z4 Z3 Z2 Z1

NØTES:
1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. THE DATA BITS FRØM EACH TRUNK SEPARATE, 4 BITS TØ EACH CØUNTER. THE SELECTED PARITY BIT STILL REPRESENTS THE PARITY FØR ALL 8 SELECTED DATA BITS. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF THE 8 DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

5/05

-(0-7) -(0-3) [-WRFA1(0-3)] → RPU 4.2-03 (B2/F2-D05)
-(4-7) [-RDFA1(0-3)] → RPU 4.2-03 (B2/F2-E05)

CLK 4.1-03 (A2-B01/B-46) [-ØFFCLK(4)]
RPU 4.0-01 (B2-C15/A-27) [-MCF(10)]
RPU 4.2-01 (B2/J2-D11-05) [-GATØF1]
RPU 4.1-21 (B2/J2-D07-08) [-REDØF1]

INPUT FIFØ WØRD CØUNTER

12CD K06/1D16

PARA 48 C1D
PARB 43 C2D
A(0-7) A(0) A(3) Z4 Z3 C1D
B(0-7) B(0) B(3) A(4) A(7) Z2 Z1 B(4) B(7) C2D
DUAL 16 CNTRS WITH PARITY TØGGLE
X=Y
CLCK 03
EN 07
SEL(0) 30
SEL(1) 15
PMBØIU 52
PMIL 10
DECR 33
CZERØ 22
29 PARZ
Z(0-7)
Z(0) Z(3) Z(4) Z(7)
N N+7
Σ A B 128 16 A>B, A=B
49 BGTR
50 BGTRL
51 BEQR
47 BEQRL
G3 G2 G1
7 6 5 4 C2 C1 R Z4 Z3 Z2 Z1

NØTES:
1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. THE DATA BITS FRØM EACH TRUNK SEPARATE, 4 BITS TØ EACH CØUNTER. THE SELECTED PARITY BIT STILL REPRESENTS THE PARITY FØR ALL 8 SELECTED DATA BITS. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF THE 8 DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

5/05

NU → -(0.2)
BIAS 0 FRØM PANEL A2 [-RIINPF] → -(1.3)
-(4-7)
-(0-7)

RPU 4.1-11 (B2/J2-E05-05) [-RWIF1]

NU → -(0-1.3)
BIAS 0 FRØM PANEL A2 [-RIØUTF] → -(2)
-(4-7)
-(0-7)

[-NIFFL1] → RPU 4.2-01 (B2/F2-B10-01.02)
+WRITE DATA AVAIL [-NWDA1] → RPU 4.1-21 (B2/J2-B03-23)
[-NWDA1] → RPU 4.1-00 (B2-H05-30)

RPU 4.2-01 (B2/F2-E11-07) [-ENCTR1]

ØUTPUT FIFØ WØRD CØUNTER

12CD G11/1D12

PARA 48 C1D
PARB 43 C2D
A(0-7) A(0) A(3) Z4 Z3 C1D
B(0-7) B(0) B(3) A(4) A(7) Z2 Z1 B(4) B(7) C2D
DUAL 16 CNTRS WITH PARITY TØGGLE
X=Y
CLCK 03
EN 07
SEL(0) 30
SEL(1) 15
PMBØIU 52
PMIL 10
DECR 33
CZERØ 22
29 PARZ
Z(0-7)
Z(0) Z(3) Z(4) Z(7)
N N+7
Σ A B 128 16 A>B, A=B
49 BGTR
50 BGTRL
51 BEQR
47 BEQRL
G3 G2 G1
7 6 5 4 C2 C1 R Z4 Z3 Z2 Z1

NØTES:
1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. THE DATA BITS FRØM EACH TRUNK SEPARATE, 4 BITS TØ EACH CØUNTER. THE SELECTED PARITY BIT STILL REPRESENTS THE PARITY FØR ALL 8 SELECTED DATA BITS. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF THE 8 DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

5/05

[-NØFFL1] → RPU 4.1-01 (B2-H06-37)
[-NØUTR1] → RPU 4.1-21 (B2/J2-D02-07)

NØTE: 1

BIT	A	B	Z
0	45	44	31
1	42	34	26
2	38	37	23
3	35	32	25
4	20	17	24
5	18	01	21
6	16	09	05
7	11	06	04

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
RING PØRT 1 FIFØ WRITE/READ AND WØRD CØUNTERS
DB-B2RPU:B2

CODE IDENT NO 60461830
REV A
SHEET RPU 4.1-02
PAGE IV-T-33

5 BIT	AUX	LSI
0	10-25	B2-J05-51
1	10-20	B2-J05-46
2	10-26	B2-J05-52
3	10-19	B2-J05-45

6 BIT	AUX	LSI
0	10-24	B2-J05-50
1	10-21	B2-J05-47
2	09-01	B2-J06-27
3	09-03	B2-J06-29

7 BITS	Δ	T1	T2	F1	F2
0,12,16,20,24	24	1	2	3	4
1,13,17,21,25	23	8	7	6	5
2,14,18,22,26	20	11	12	13	14
3,15,19,23,27	19	18	17	16	15

1 BIT	AUX	LSI
0	02-03	B2-J13-29
1	02-15	B2-J13-41
2	02-06	B2-J13-32
3	02-17	B2-J13-43
4	01-03	B2-J14-29
5	02-25	B2-J13-51
6	01-10	B2-J14-36
7	01-15	B2-J14-41
8	01-17	B2-J14-43
9	01-16	B2-J14-42
10	01-20	B2-J14-46
11	01-21	B2-J14-47
12	03-15	B2-J12-41
13	04-25	B2-J11-51
14	03-21	B2-J12-47
15	03-24	B2-J12-50
16	05-24	B2-J10-50
17	05-21	B2-J10-47
18	05-19	B2-J10-45
19	05-20	B2-J10-46
20	04-03	B2-J11-29
21	04-01	B2-J11-27
22	04-15	B2-J11-41
23	03-09	B2-J12-35
24	03-07	B2-J12-33
25	02-08	B2-J13-34
26	03-08	B2-J12-34
27	03-20	B2-J12-46

3 BIT	AUX	LSI
0	09-19	B2-J06-45
1	09-17	B2-J06-43
2	09-21	B2-J06-47
3	09-20	B2-J06-46
4	07-03	B2-J08-29
5	07-04	B2-J11-30
6	07-06	B2-J11-32
7	07-01	B2-J11-27

4 BIT	AUX	LSI
12	06-10	B2-J09-36
13	06-04	B2-J09-30
14	06-16	B2-J09-42
15	06-15	B2-J09-41
16	09-16	B2-J06-42
17	09-15	B2-J06-41
18	09-10	B2-J06-36
19	09-08	B2-J06-34
20	06-20	B2-J09-46
21	06-19	B2-J09-45
22	06-21	B2-J09-47
23	06-24	B2-J09-50
24	06-06	B2-J09-32
25	07-26	B2-J08-52
26	06-03	B2-J09-29
27	06-01	B2-J09-27

2 BIT	AUX	LSI
0	02-07	B2-J13-33
1	01-04	B2-J14-30
2	01-08	B2-J14-34
3	02-24	B2-J13-50
4	07-19	B2-J08-45
5	07-25	B2-J08-51
6	07-21	B2-J08-47
7	07-24	B2-J08-50
8	01-19	B2-J14-45
9	01-25	B2-J14-51
10	01-26	B2-J14-52
11	01-24	B2-J14-50
12	02-10	B2-J13-36
13	03-25	B2-J12-51
14	03-26	B2-J12-52
15	02-09	B2-J13-35
16	05-26	B2-J10-52
17	04-20	B2-J11-46
18	04-19	B2-J11-45
19	05-25	B2-J10-51
20	04-09	B2-J11-35
21	04-16	B2-J11-42
22	04-21	B2-J11-47
23	04-08	B2-J11-34
24	03-17	B2-J12-43
25	02-20	B2-J13-46
26	02-19	B2-J13-45
27	03-19	B2-J12-45

RPU 4.1-00 (B2-H14) [-IDR1(0-27)] 28

RING INPUT RGTR FANØUT

12|12 E03/A13 BITS 0-3 — CX 22, A1 24, A2 23, A3 20, A4 19, G1 8

12|12 E02/A14 BITS 4-7 — CX 22, A1 24, A2 23, A3 20, A4 19, G1 8

12|12 E01/A15 BITS 8-11 — CX 22, A1 24, A2 23, A3 20, A4 19, G1 8

-INTR BIT → K RPU 4.1-21 (B2/J2-A04/A-24)

RPU 4.1-02 (B2-K05) -WRITE ADRS CNT [-WIFA1(0-3)]

RPU 4.1-02 (B2-K05) -READ ADRS CNT [-RIFA1(0-3)]

12|12 D12/A01 BITS 0-3 — TP86,87, T4,73

12|12 E12/A02 BITS 0-3 — TP91,78, T5,114

-RID(0-7) [-A13,FX] → RPU 4.1-21 (B2/J2-C03)

RPU 4.1-20 (B2/J2-E08-12) -INP FIFØ WE2

RPU 4.1-20 (B2/J2-E08-16) -INP FIFØ WE1

INPUT FIFØ

12|45 E11/B03 BITS 0-3 — 12|45 E10/B04 4-7 — 12|45 E09/B05 12-15 — 12|45 D11/B06 16-19 — 12|45 D10/B07 20-23 — 12|45 D09/B08 BITS 24-27

W3 02, W2 01, W1 24, W0 23, S3 03, S2 04, S1 05, S0 06, C1 20, C2 19, E1 18, E2 17, MS 22, R

1A15 1A00 2A15 2A00 G4/C5 G2/C3 G1

DI(0-3) D — MEM — DØ(0-3) T — 1AC5D 2A2+1 2A+C3D4+1 — 16,15,14,13 — 7,8,11,12

-(12-27) 16 [-IFDI(0-15)] → 4 RPU 4.1-00 (B2-K07)

[-IFØI(0-7)] → 3 RPU 4.1-00 (B2-H05)

-W ADRS → RPU 4.1-11 (B2/J2-C01)

-INPUT DATA RGTR → RPU 4.1-22 (B2/J2-A01)

-RPI INPUT RGTR → RPU 4.1-22 (B2/J2-C07-16)

[+COMPDATA] → RPU 4.1-11 (B2/J2-C01)

RING INPUT RGTR FANØUT

12|12 C04/C01 BITS 12-15 — 12|12 C05/C02 BITS 16-19

12|12 D05/C03 BITS 20-23 — 12|12 D04/C04 BITS 24-27

-(12-27) 16 → RPU 4.1-22 (B2/J2-C07-05.01) -(17,18) 2

+(12,13) 2 [-NRPID(12,13)] → RPU 4.1-11 (B2/J2-D01-13,14)

[-RID1(0-27)] 28 → 2 RPU 4.1-00 (B2-G12)

-LØST PACKET DATA -(0-19) 20 → RPU 4.1-13 (B2/J2-B08)

[-NRID(20-27)] → RPU 4.1-13 (B2/J2-B08,C08)

-(4-7) 4 → I RPU 4.1-11 (B2/J2-C01)

-(8-27) 20 → J RPU 4.1-11 (B2/J2-E04,E05)

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM INPUT DATA AND INPUT FIFØ REGISTERS RING PØRT 1	CODE IDENT NO	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-B2RP1:B2/J2	SHEET RPU 4.1-10	SIZE IV-7-35

RPU 4.2-01
(B2/F2-E07/C-14)
[-CLINT1]
(4-7)
(B2-J11-33)

RPU 4.1-20
(B2/J2-D15-02)
RPU 4.1-21
(B2/J2-D06-04)

SW COMPARE
12107 E05/A07

RPU 4.1-20
(B2/J2-E08-08)
-READ IN FIFØ
[-A38A.T1]

RPU 4.1-20
(B2/J2-E08-13)
-F INT GATED*
[-A38D.T1]

CØN 4.6-00
A1(REAR)-SW6
[-HWCS1(0-7)]

-(20)
-(0)
-(21)
-(1)
-(22)
-(2)

[-RWIF1]
(4-17)
(B2-J11-43)
RPU 4.1-02
(B2-K06-10/52)

-SEL INT CNTR(0)
[-A07B.T1]
RPU 4.1-20
(B2/J2-E06-23)

BIT	AUX	LSI	CØAX
0	04-04	B2-J11-30	3-BS01
1	04-06	B2-J11-32	3-BS02
2	04-10	B2-J11-36	3-BS03
3	03-10	B2-J12-36	3-BS06
4	03-04	B2-J12-30	3-BS05
5	03-03	B2-J12-29	3-BR05
6	03-06	B2-J12-32	3-BR04
7	03-16	B2-J12-42	3-BS07

12107 E04/A16

-(23)
-(3)
-(24)
-(4)
-(25)
-(5)
-(26)
-(6)
-(27)
-(7)

RPU 4.1-10
(B2/J2-D04)
-(20-27)

12101 C03/A17A-A/C

-SWITCHES = DATA L CØNT FLD = 5+7
[-A17A.T1]
RPU 4.1-21
(B2/J2-B02/A-05)
RPU 4.1-22
(B2/J2-A01-19,20)
RPU 4.1-21
(B2/J2-C02-19)

+SW = DATA L CØNT FLD = 5+7

DESTINATIØN TABLE
12145 C01/B01

RPU 4.1-10
(B2/J2-E02)
-W ADRS
-(4)
-(5)
-(6)
-(7)

RPU 4.1-10
(B2/J2-E02)
-R ADRS
-(4)
-(5)
-(6)
-(7)

-(CØNT FLD=5)*(SWITCH=DATA)
[-A08A.T1]

RPU 4.1-21
(B2/J2-B02/A-07)

RPU 4.1-20
(B2/J2-B04-11)
+SYSCLK DEL
[-A1D.T5]

MEM

-(11)
-(10)
-(9)
-(8)

RPU 4.1-21
(B2/J2-C09-04)
+WC
[-A39.F2]

RPU 4.1-10
(B2/J2-C04,C05)
[-NRPID(12,13)]
-(12)
-(13)

RPU 4.1-10
(B2/J2-E01)
[+CØMPDATA]
+(8-11)

12145 D01/B02

-DEST TBL ENABLE

+GØBBLE BIT
[-B02.T3]
RPU 4.1-21
(B2/J2-C02-24)

CØMPARE
12107 B01/A05

+(8)
+(9)
+(10)
+(11)

-LØGICAL CØMP
[-A05.EQ]

RPU 4.1-21
(B2/J2-D07-03)
+RING STØP
[-A12.T1]

RPU 4.1-21
(B2/J2-D02-11)
-A04.F1

RPU 4.1-10
(B2/J2-E03)
[-IDR1(1-3)]

12102 D03/A06

TP25
-CØNT FLD = 5+7

-ØUT FIFØ SELECTED
[-A06.T1]
RPU 4.1-21
(B2/J2-D07-20)

-CØNT FLD = 6+7
[-A06.T3]
RPU 4.1-22
(B2/J2-A01-22,23)

+CØNT FLD = 6+7
RPU 4.1-21
(B2/J2-B02/A,B03-04)

[-WRIF1]
(1-1)
(B2-J14-27)
RPU 4.1-02
(B2-K05-52)

+DATA TØ IN FIFØ
[-A06.F4]
RPU 4.1-21
(B2/J2-B03-01)

-XFER DATA TØ FIFØ
[-A06.T5]
RPU 4.1-20
(B2/J2-E08-17,23)

+DATA XFER
RPU 4.1-21
(B2/J2-C02-16)

+CF = 5+7
[-A06.F2]
RPU 4.1-21
(B2/J2-B03-03)

-CF = 5+7

12101 C03/A17C-C/C

[-A17C.T1]
RPU 4.1-21
(B2/J2-C02-15)

RPU 4.1-21
(B2/J2-C03/B-12)
+EMPTY PACKET
[-CF=0]

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM RING PØRT I DESTINATIØN TABLE AND CØMPARE	CODE IDENT	DWG NØ 60461830 REV A
DEVELOPMENT DIVISIØN	DB-B2RP1:B2/J2	SHEET RPU 4.1-11	PAGE IV-7-37

BIT	AUX	LSI
0	11-25	B2-J04-51
1	12-24	B2-J03-50
2	11-06	B2-J04-32
3	12-17	B2-J03-43
4	13-04	B2-J02-30
5	12-07	B2-J03-33
6	12-25	B2-J03=51
7	11-24	B2-J04-50
8	12-26	B2-J03-52
9	13-10	B2-J02-36
10	13-01	B2-J02-27
11	11-07	B2-J04-33
12	13-15	B2-J02-41
13	13-03	B2-J02-29
14	13-07	B2-J02-33
15	13-08	B2-J02-34

RPU 4.1-01 (B2-H06/H07) [-MSKI(0-15)]

SET FLAG DECØDER

12170 B13/A21

RPU 4.1-20 (B2/J2-A12) [+STATREG(0)] [-STATREG(0-3)]

RPU 4.1-20 (B2/J2-C13-16) -SET STATUS STRØBE

12170 A13/A20

+(0)

-(0-15)

-(15) RPU 4.1-20 (B2/J2-C13-1.23)

FLAG RGTR

12131 A16/A22 BITS 0-2

12131 A17/A23 3-5

12131 B16/A24 6-8

12131 B17/A25 9-11

12131 C16/A26 12-14

12131 C17/A27 BITS 15.X.Y

RPU 4.1-21 (B2/J2-C09-07) +MC [-A39.T4]

RPU 4.1-22 (B2/J2-D16) -CLR STAT RGTR (A22-A27)

RPU 4.1-21 (B2/J2-C09-08) [-A39.T3]

NU (X)

NU (Y)

FLAG CØMPARE

12118 C14/A32 — TP91 — (C)

12118 B14/A31 — TP90 — (B)

12118 A14/A30 — TP89 — (A)

FLAG CØMPARE

12118 C15/A35 — TP93 — (D)

12118 B15/A34 — TP96 — (E)

12118 A15/A33 — TP94 — (F)

+STATUS (15) RPU 4.1-20 B2/J2-C13-02)

-STATUS BITS (0-15) RPU 4.1-20 (B2/J2-B12)

+STATUS (0-15) RPU 4.1-13 (B2/J2-B10)

-TEST (A-F) RPU 4.1-20 (B2/J2-C12/A.B)

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM STATUS AND COMPARE REGISTERS RING PØRT 1	CAGE IDENT / DWG NO	REV
		60461830	A
DEVELOPMENT DIVISIØN	DB-B2RP1:B2/J2	SHEET RPU 4.1-12	PAGE IV-T-39

RPU 4.1-21 (B2/J2-D14-13) +LØST PACKET BIT FF

RPU 4.1-22 (B2/J2-E15/A-11) -STAT SEL 0

RPU 4.1-22 (B2/J2-E15/B-07) -STAT SEL 1

RPU 4.1-10 (B2/J2-C05) -LØST PACKET DATA (20)

RPU 4.1-10 (B2/J2-B05) [-CLØCKS (D1-D5)] (5)

RPU 4.1-21 (B2/J2-D14-12) +LØST PACKET FF

RPU 4.1-10 (B2/J2-D04,D05) [-NRID(20-27)] (8)

RPU 4.1-22 (B2/J2-D13-13,16) -CLØCK ENABLE (3)

(D13-16)

(D13-16)

LØST PACKET RGTR 12151 BØ8/DØ4 — RGTR

LØST PACKET RGTR 12151 AØ9/DØ1 — RGTR

12151 CC8/DØ5 — RGTR

12151 BØ9/DØ2 — RGTR

12151 AØ8/DØ3 — RGTR

XBAR DATA SELECT 12171 A10/DØ6 — MUX

XBAR DATA SELECT 12171 B11/DØ9 — MUX

12171 A11/DØ7 — MUX

12171 B10/DØ8 — MUX

12171 C10/DI0 — MUX

12171 C11/DI1 — MUX

-X BAR 15 IN (0-15) [-STR1(0-15)/ XBRIO-15(15)] (16) → C2N 4.2-01 DATA X BAR (C2-G01 → K15-17,48)

BIT	AUX	LSI
0	07-15	B2-J08-41
1	07-09	B2-J08-35
2	07-20	B2-J08-46
3	08-10	B2-J07-36
4	08-09	B2-J07-35
5	08-15	B2-J07-41
6	07-08	B2-J08-34
7	07-10	B2-J08-36
8	08-24	B2-J07-50
9	08-08	B2-J07-34
10	08-07	B2-J07-33
11	08-03	B2-J07-29
12	08-26	B2-J07-52
13	07-07	B2-J08-33
14	08-20	B2-J07-46
15	08-04	B2-J07-30

BIT	AUX	LSI
0	08-25	B2-J07-51
1	10-06	B2-J05-30
2	11-20	B2-J04-46
3	08-01	B2-J07-27
4	09-24	B2-J06-50
5	08-17	B2-J07-43
6	08-21	B2-J07-47
7	09-06	B2-J06-32
8	10-07	B2-J05-33
9	09-25	B2-J06-51
10	10-01	B2-J05-27
11	09-26	B2-J06-52
12	08-19	B2-J07-45
13	08-16	B2-J07-42
14	09-07	B2-J06-33
15	09-04	B2-J06-30

RPU 4.1-12 (B2/J2-A16) +STATUS (0-15)

RPU 4.0-13 (B2/J1-B11) [-STSR(0-15)]

RPU 4.1-22 (B2/J2-E15/A-12) +STAT SEL 0

RPU 4.1-22 (B2/J2-E15/B-08) +STAT SEL 1

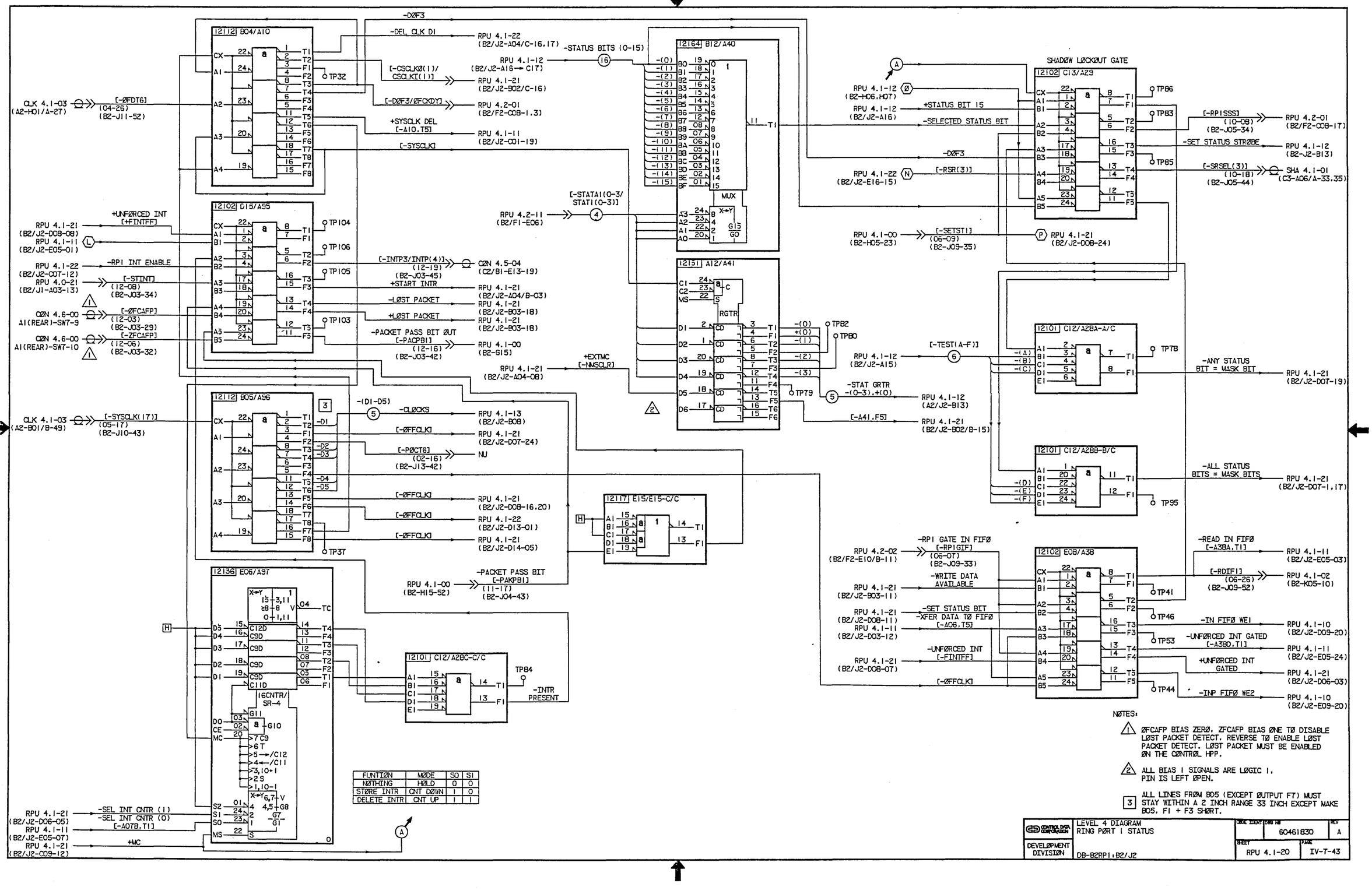
(7) -(9-15) -(0-8) (9)

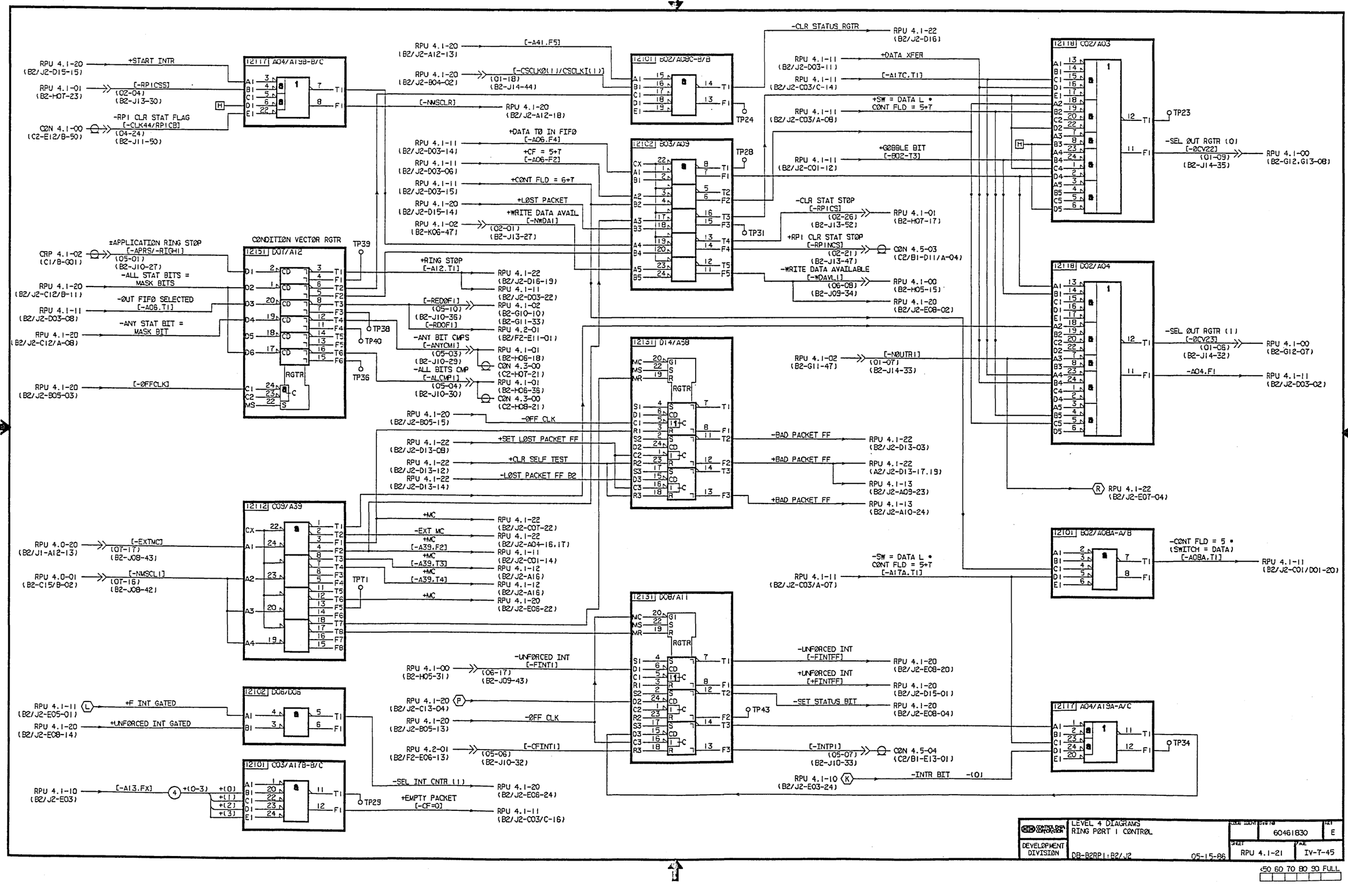
RPU 4.1-22 (M) (B2/J2-E16-18,16) [-RSR(1,2)] (2)

[-SRSEL(1)] (8-6) (B2-J07-32) → NU

[-SRSEL(2)] (9-9) (B2-J06-35) → SHA 4.1-01 (C3-A06/A-20,22)

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	LEVEL 4 DIAGRAM DATA TØ X BAR RING PØRT 1 DB-B2RP1:B2/J2	CODE IDENT	DWG NO 60461830 REV A
		SHEET RPU 4.1-13	PAGE IV-7-41


12112 B04/A10
12112 B05/A56
12102 D15/A55
12164 B12/A40
12131 A12/A41
12102 C13/A29
SHADØW LØCKØUT GATE
12101 C12/A28A-A/C
12101 C12/A28B-B/C
12102 E08/A38
12136 E06/A37
12101 C12/A28C-C/C
12117 E15/E15-C/C
MUX
RGTR
16CNTR/SR-4
CLK 4.1-03 (A2-H01/A-27)
[-ØFDT6] (04-26) (B2-J11-52)
-DØF3
-DEL CLK DI
RPU 4.1-22 (B2/J2-A04/C-16,17)
-STATUS BITS (0-15)
RPU 4.1-12 (B2/J2-A16→C17)
[-CSCLKØ(1)/CSCLK1(1)]
RPU 4.1-21 (B2/J2-B02/C-16)
[-DØF3/ØFCKDY]
RPU 4.2-01 (B2/F2-C08-1,3)
+SYSCLK DEL [-A10,T5]
RPU 4.1-11 (B2/J2-C01-19)
[-SYSCLK]
TP32
[-STATA1(0-3/STAT1(0-3)]
RPU 4.2-11 (B2/F1-E06)
+UNFØRCED INT [+FINTFF]
RPU 4.1-21 (B2/J2-D08-08)
RPU 4.1-11 (B2/J2-E05-01)
-RPI INT ENABLE
RPU 4.1-22 (B2/J2-C07-12)
RPU 4.0-21 (B2/J1-A03-13)
[-STINT] (12-08) (B2-J03-34)
C2N 4.6-00 A1(REAR)-SW7-9
[-ØFCAFP] (12-03) (B2-J03-29)
C2N 4.6-00 A1(REAR)-SW7-10
[-ZFCAFP] (12-06) (B2-J03-32)
TP104
TP106
TP105
TP103
[-INTP3/INTP(4)] (12-19) (B2-J03-45)
C2N 4.5-04 (C2/B1-E13-19)
+START INTR
RPU 4.1-21 (B2/J2-A04/B-03)
-LØST PACKET
RPU 4.1-21 (B2/J2-B03-18)
+LØST PACKET
RPU 4.1-21 (B2/J2-B03-18)
-PACKET PASS BIT ØUT [-PAQPBI] (12-16) (B2-J03-42)
RPU 4.1-00 (B2-G15)
RPU 4.1-21 (B2/J2-A04-08)
+EXTMC [-NMSCLR]
-(0)
+(0)
-(1)
-(2)
-(3)
TPB2
TPB0
TPB9
-STAT GRTR -(0-3),+(0)
RPU 4.1-12 (A2/J2-B13)
[-A41,F5]
RPU 4.1-21 (B2/J2-B02/B-15)
[-TEST(A-F)]
RPU 4.1-12 (B2/J2-A15)
TP78
-ANY STATUS BIT = MASK BIT
RPU 4.1-21 (B2/J2-D07-19)
TP86
TP83
TP85
RPU 4.1-12 (B2-H06,H07)
+STATUS BIT 15
-SELECTED STATUS BIT
-DØF3
RPU 4.1-22 (B2/J2-E16-15)
[-RSR(3)]
RPU 4.1-00 (B2-H05-23)
[-SETST1] (06-09) (B2-J09-35)
RPU 4.1-21 (B2/J2-D08-24)
[-RP1SSS] (10-08) (B2-J05-34)
RPU 4.2-01 (B2/F2-C08-17)
-SET STATUS STRØBE
RPU 4.1-12 (B2-J2-B13)
[-SRSEL(3)] (10-18) (B2-J05-44)
SHA 4.1-01 (C3-A06/A-33,35)
-ALL STATUS BITS = MASK BITS
RPU 4.1-21 (B2/J2-D07-1,17)
TP95
CLK 4.1-03 (A2-B01/B-49)
[-SYSCLK(17)] (05-17) (B2-J10-43)
-(D1-D5)
-CLØCK5
RPU 4.1-13 (B2/J2-B08)
[-ØFFCLK]
RPU 4.1-21 (B2/J2-D07-24)
[-PØCT6] (02-16) (B2-J13-42)
NU
-D1
-D2
-D3
-D4
-D5
TP37
[-ØFFCLK]
RPU 4.1-21 (B2/J2-D08-16,20)
[-ØFFCLK]
RPU 4.1-22 (B2/J2-D13-01)
[-ØFFCLK]
RPU 4.1-21 (B2/J2-D14-05)
-PACKET PASS BIT [-PAKPBI] (11-17) (B2-J04-43)
RPU 4.1-00 (B2-H15-52)
-RPI GATE IN FIFØ [-RPIGIF] (06-07) (B2-J09-33)
RPU 4.2-02 (B2/F2-E10/B-11)
-WRITE DATA AVAILABLE
RPU 4.1-21 (B2/J2-B03-11)
-SET STATUS BIT
-XFER DATA TØ FIFØ [-A06,T5]
RPU 4.1-21 (B2/J2-D08-11)
RPU 4.1-11 (B2/J2-D03-12)
-UNFØRCED INT [-FINTFF]
RPU 4.1-21 (B2/J2-D08-07)
[-ØFFCLK]
-READ IN FIFØ [-A38A,T1]
[-RDIF1] (06-26) (B2-J09-52)
RPU 4.1-11 (B2/J2-E05-03)
RPU 4.1-02 (B2-K05-10)
TP41
TP46
TP53
TP44
-IN FIFØ WE1
RPU 4.1-10 (B2/J2-D09-20)
-UNFØRCED INT GATED [-A38D,T1]
RPU 4.1-11 (B2/J2-E05-24)
+UNFØRCED INT GATED
RPU 4.1-21 (B2/J2-D06-03)
-INP FIFØ WE2
RPU 4.1-10 (B2/J2-E09-20)
TP84
-INTR PRESENT
-SEL INT CNTR (1)
-SEL INT CNTR (0) [-A07B,T1]
RPU 4.1-21 (B2/J2-D06-05)
RPU 4.1-11 (B2/J2-E05-07)
RPU 4.1-21 (B2/J2-C09-12)
+MC
FUNTIØN | MØDE | SO | SI
NØTHING | HØLD | 0 | 0
STØRE INTR | CNT DØWN | 1 | 0
DELETE INTR | CNT UP | 1 | 1
NØTES:
1 ØFCAFP BIAS ZERØ, ZFCAFP BIAS ØNE TØ DISABLE LØST PACKET DETECT. REVERSE TØ ENABLE LØST PACKET DETECT. LØST PACKET MUST BE ENABLED ØN THE CØNTRØL HPP.
2 ALL BIAS 1 SIGNALS ARE LØGIC 1, PIN IS LEFT ØPEN.
3 ALL LINES FRØM B05 (EXCEPT ØUTPUT F7) MUST STAY WITHIN A 2 INCH RANGE 33 INCH EXCEPT MAKE B05, F1 + F3 SHØRT.
CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 4 DIAGRAM
RING PØRT 1 STATUS
DB-B2RP1:B2/J2
CODE IDENT
DWG NO 60461830
REV A
SHEET RPU 4.1-20
PAGE IV-7-43


RPU 4.1-20 (B2/J2-D15-15) +START INTR
RPU 4.1-01 (B2-H07-23) [-RP1CSS] (02-04) (B2-J13-30)
C2N 4.1-00 (C2-E12/B-50) -RP1 CLR STAT FLAG [-CLK44/RP1CB] (04-24) (B2-J11-50)
12117 A04/A19B-B/C
RPU 4.1-20 (B2/J2-A12-13) [-A41.F5]
RPU 4.1-20 (B2/J2-B04-02) [-CSCLK0(1)/CSCLKI(1)] (01-18) (B2-J14-44)
[-NMSCLR] RPU 4.1-20 (B2/J2-A12-18)
12101 B02/A08C-B/B
TP24
-CLR STATUS RGTR RPU 4.1-22 (B2/J2-D16)
RPU 4.1-11 (B2/J2-D03-11) +DATA XFER
RPU 4.1-11 (B2/J2-C03/C-14) [-A17C.T1]
RPU 4.1-11 (B2/J2-C03/A-08) +SW = DATA L • C0NT FLD = 5+7
12118 C02/A03
TP23
-SEL 0UT RGTR (0) [-0CV22] (01-09) (B2-J14-35) RPU 4.1-00 (B2-G12,G13-08)
+DATA T0 IN FIF0 [-A06.F4]
RPU 4.1-11 (B2/J2-D03-14) +CF = 5+T [-A06-F2]
RPU 4.1-11 (B2/J2-D03-06) +C0NT FLD = 6+T
RPU 4.1-11 (B2/J2-D03-15) +L0ST PACKET
RPU 4.1-20 (B2/J2-D15-14) +WRITE DATA AVAIL [-NWDAI] (01-01) (B2-J13-27)
RPU 4.1-02 (B2-K06-47)
12102 B03/A09
TP28
TP31
+G0BBLE BIT [-B02-T3]
RPU 4.1-11 (B2/J2-C01-12)
-CLR STAT ST0P [-RP1CS] (02-26) (B2-J13-52) RPU 4.1-01 (B2-H07-17)
+RPI CLR STAT ST0P [-RP1NCS] (02-21) (B2-J13-47) C2N 4.5-03 (C2/B1-D11/A-04)
-WRITE DATA AVAILABLE [-WDAVL1] (06-08) (B2-J09-34) RPU 4.1-00 (B2-H05-15)
RPU 4.1-20 (B2/J2-E08-02)
±APPLICATI0N RING ST0P [-APRS/-RIGHI] (05-01) (B2-J10-27)
CRP 4.1-02 (C1/B-G01)
-ALL STAT BITS = MASK BITS
RPU 4.1-20 (B2/J2-C12/B-11)
-0UT FIF0 SELECTED [-A06.T1]
RPU 4.1-11 (B2/J2-D03-08)
-ANY STAT BIT = MASK BIT
RPU 4.1-20 (B2/J2-C12/A-08)
C0NDITI0N VECT0R RGTR
12151 D07/A12
TP39
TP38
TP40
TP36
+RING ST0P [-A12.T1]
RPU 4.1-22 (B2/J2-D16-19)
RPU 4.1-11 (B2/J2-D03-22)
[-RED0F1] (05-10) (B2-J10-36) [-RD0F1] RPU 4.1-02 (B2-G10-10) (B2-G11-33)
RPU 4.2-01 (B2/F2-E11-01)
-ANY BIT CMPS [-ANYCM1] (05-03) (B2-J10-29) RPU 4.1-01 (B2-H06-18) C2N 4.3-00 (C2-H07-21)
-ALL BITS CMP [-ALCMP1] (05-04) (B2-J10-30) RPU 4.1-01 (B2-H06-38) C2N 4.3-00 (C2-H08-21)
RPU 4.1-20 (B2/J2-B05-03) [-0FFCLK]
RPU 4.1-20 (B2/J2-B05-15) -0FF CLK
12131 D14/A58
RPU 4.1-02 (B2-G11-47) [-N0UTR1] (01-07) (B2-J14-33)
12118 D02/A04
-SEL 0UT RGTR (1) [-0CV23] (01-06) (B2-J14-32) RPU 4.1-00 (B2-G12-07)
-A04.F1 RPU 4.1-11 (B2/J2-D03-02)
RPU 4.1-22 (B2/J2-D13-08) +SET L0ST PACKET FF
RPU 4.1-22 (B2/J2-D13-12) +CLR SELF TEST
RPU 4.1-22 (B2/J2-D13-14) -L0ST PACKET FF B2
-BAD PACKET FF RPU 4.1-22 (B2/J2-D13-03)
+BAD PACKET FF RPU 4.1-22 (A2/J2-D13-17,19)
RPU 4.1-13 (B2/J2-A09-23)
+BAD PACKET FF RPU 4.1-13 (B2/J2-A10-24)
R RPU 4.1-22 (B2/J2-E07-04)
12112 C09/A39
RPU 4.0-20 (B2/J1-A12-13) [-EXTMC] (07-17) (B2-J08-43)
RPU 4.0-01 (B2-C15/B-02) [-NMSCL1] (07-16) (B2-J08-42)
TPT1
+MC RPU 4.1-22 (B2/J2-C07-22)
-EXT MC +MC [-A39.F2] RPU 4.1-22 (B2/J2-A04-16,17)
+MC [-A39.T3] RPU 4.1-11 (B2/J2-C01-14)
+MC [-A39.T4] RPU 4.1-12 (B2/J2-A16)
+MC RPU 4.1-12 (B2/J2-A16)
RPU 4.1-20 (B2/J2-E06-22)
12101 B02/A08A-A/B
-C0NT FLD = 5 • (SWITCH = DATA) [-A08A.T1] RPU 4.1-11 (B2/J2-C01/D01-20)
-SW = DATA L • C0NT FLD = 5+T [-A17A.T1]
RPU 4.1-11 (B2/J2-C03/A-07)
-UNF0RCED INT [-FINTI1] RPU 4.1-00 (B2-H05-31) (06-17) (B2-J09-43)
12131 D08/A11
-UNF0RCED INT [-FINTFF] RPU 4.1-20 (B2/J2-E08-20)
+UNF0RCED INT [+FINTFF] RPU 4.1-20 (B2/J2-D15-01)
-SET STATUS BIT RPU 4.1-20 (B2/J2-E08-04)
TP43
RPU 4.1-20 (P) (B2/J2-C13-04)
RPU 4.1-20 (B2/J2-B05-13) -0FF CLK
RPU 4.2-01 (B2/F2-E06-13) [-CFINT1] (05-06) (B2-J10-32)
[-INTP1] (05-07) (B2-J10-33) C2N 4.5-04 (C2/B1-E13-01)
RPU 4.1-10 (K) (B2/J2-E03-24) -INTR BIT -(0)
12117 A04/A19A-A/C
TP34
RPU 4.1-11 (L) (B2/J2-E05-01) +F INT GATED
RPU 4.1-20 (B2/J2-E08-14) +UNF0RCED INT GATED
12102 D06/D06
12101 C03/A17B-B/C
RPU 4.1-10 (B2/J2-E03) [-A13.FX] 4 +(0-3) +(0) +(1) +(2) +(3)
-SEL INT CNTR (1) RPU 4.1-20 (B2/J2-E06-24)
TP29
+EMPTY PACKET [-CF=0] RPU 4.1-11 (B2/J2-C03/C-16)
CONTROL DATA CORPORATION
LEVEL 4 DIAGRAMS
RING P0RT 1 C0NTR0L
60461830 E
DEVELOPMENT DIVISION
DB-B2RP1:B2/J2 05-15-86
SHEET RPU 4.1-21
PAGE IV-7-45
<50 60 70 80 90 FULL

RPU 4.2-11 (B2/F1-D07-11) [-NSTAS(1)] (12-09) (B2-J03-35)

SHA 4.0-00 (B2-G08-21) [-RSR(5)] (12-20) (B2-J03-46)

Q2N 4.5-04 (C2/B1-C12-23) [-CKB46/ROR1] (12-10) (B2-J03-36)

12112 E14/D15

TP119

TP108

TP107

[-CBRS0(0)] (11-16) (B2-J04-42) SHA 4.0-00 (B2-K01 → K04-08)

[-CBRS0(1)] (11-15) (B2-J04-41) SHA 4.0-00 (B2-H12,K13,K15-08) H

[-CBRS1(0)] (11-19) (B2-J04-45) SHA 4.0-00 (B2-K01 → K04-07)

[-CBRS0(1)] (11-21) (B2-J04-47) SHA 4.0-00 (B2-H12,K13 → K15-07)

[-CLK(46)]

RPU 4.2-11 (B2/F1-D07-14) [-NSTAS(0)] (12-15) (B2-J03-41)

[-SRSEL(5)] (11-18) (B2-J04-44) SHA 4.1-00 (C3-K05/B-22)

12117 E15/D16A-A/C

12117 E15/D16B-B/C

-STAT SEL 0 RPU 4.1-13 (B2/J2-A10-20)

+STAT SEL 0 RPU 4.1-13 (B2/J2-C11-20)

-STAT SEL 1 RPU 4.1-13 (B2/J2-A10-19)

+STAT SEL 1 RPU 4.1-13 (B2/J2-C11-19)

SHA 4.0-00 (B2-G08-26,23,25) [-RSR(1-3)]

-(3) [-RSR(3)] N RPU 4.1-20 (B2/J2-C13-19)

[-RSR(1-2)] M RPU 4.1-13 (B2/J2-C11)

BIT	AUX	LSI
1	13-16	B2-J02-42
2	13-17	B2-J02-43
3	13-19	B2-J02-45

12170 E16/D17

-RØW DECØDER

-(1) -(2) -(3)

-(7) [-GRØUP(7)] SHA 4.0-03 (B2-A07-41)

-(6) [-GRØUP(6)] SHA 4.0-03 (B2-A07-15)

-(5) [-GRØUP(5)] SHA 4.0-02 (B2-A09-41)

-(4) [-GRØUP(4)] SHA 4.0-02 (B2-A09-15)

-(3) [-GRØUP(3)] SHA 4.0-02 (B2-D11-41)

-(2) [-GRØUP(2)] SHA 4.0-02 (B2-C09-15)

-(1) [-GRØUP(1)] SHA 4.0-01 (B2-C07-41)

-(0) [-GRØUP(0)] SHA 4.0-01 (B2-C07-15)

BIT	AUX	LSI
7	13-20	B2-J02-46
6	12-21	B2-J03-47
5	13-24	B2-J02-50
4	13-25	B2-J02-52
3	13-25	B2-J02-51
2	12-04	B2-J03-30
1	12-01	B2-J03-27
0	13-21	B2-J02-47

12112 D16/A44

RPU 4.1-21 (B2/J2-B02/B-14) -CLR STATUS RGTR

RPU 4.1-21 (B2/J2-D07-03) +RING STØP [-A12,T1]

TP118

TP109

-CLR STAT RGTR RPU 4.1-12 (B2/J2-A16)

+RING STØP [-RSTØP1] (13-06) RPU 4.1-00 (B2-J02-32)

+RING STØP [-RSTP1] (13-09) RPU 4.1-00 (B2-G12-06)

12170 A01/A93

RPU 4.1-10 (B2/J2-E02) -INPUT DATA RGTR (5-7)

RPU 4.1-11 (B2/J2-C03/A-07) -SW=DATA L • C2NT FLD=5+7 [-A17A,T1]

RPU 4.1-11 (B2/J2-D03-16) -C2NT FLD = 6+7 [-A06-T3]

RPU 4.1-20 (B2/J2-B05-14) [-ØFFCLK]

RPU 4.1-20 (B2/J2-D15-13) -LØST PACKET

RPU 4.1-21 (B2/J2-D14-11) -LØST PACKET FF

RPU 4.1-21 (B2/J2-D14-12) +LØST PACKET FF

12102 D13/

-SET LØST PACKET FF RPU 4.1-21 (B2/J2-D14-1,16)

[-STPRG1] (10-04) (B2-J05-30) RPU 4.2-01 (B2/F2-C06/A-20)

-CLØCK ENABLE RPU 4.1-13 (B2/J2-C08)

TP87

-LØST PACKET FF B2 RPU 4.1-21 (B2/J2-D114-15)

+CLR SELF TEST RPU 4.1-21 (B2/J2-D14-23,18)

RPU 4.2-01 (B2/F2-E06-06) +CLR SELF TEST [-CSLFT1] (11-26) (B2-J04-52) -(17,18)

RPU 4.1-10 (B2/J2-C05)

RPU 4.2-01 (B2/F2-E08-08) +SET SELF TEST [-SSLFT1] (C5-09) (B2-J10-35)

RPU 4.2-01 (B2/F2-E06-07) +CLR INT EN [-CIENI] (C5-08) (B2-J10-34)

RPU 4.2-01 (B2/F2-E06-05) +SET INT EN [-SIENI] (C6-25) (B2-J09-51)

RPU 4.1-10 (B2/J2-E01-17) -RP1 INPUT RGTR

RPU 4.1-10 (B2/J2-C09-03) +MC

12131 C07/A84

RGTR

-(17) -(18)

-SEL RING DATA [-ICV19] (05-15) (B2-J10-41) RPU 4.1-00 (B2-D14-49)

+INT ENABLE [-INTENI] (05-16) (B2-J10-42) RPU 4.1-00 (B2-H06-17)

-RP1 INT ENABLE RPU 4.1-20 (B2/J2-D15-04)

TP42

12117 E07/E07

RPU 4.1-21 (B2/J2-D02-07) R

RPU 4.1-21 (B2/J2-C09-02) -EXT MC

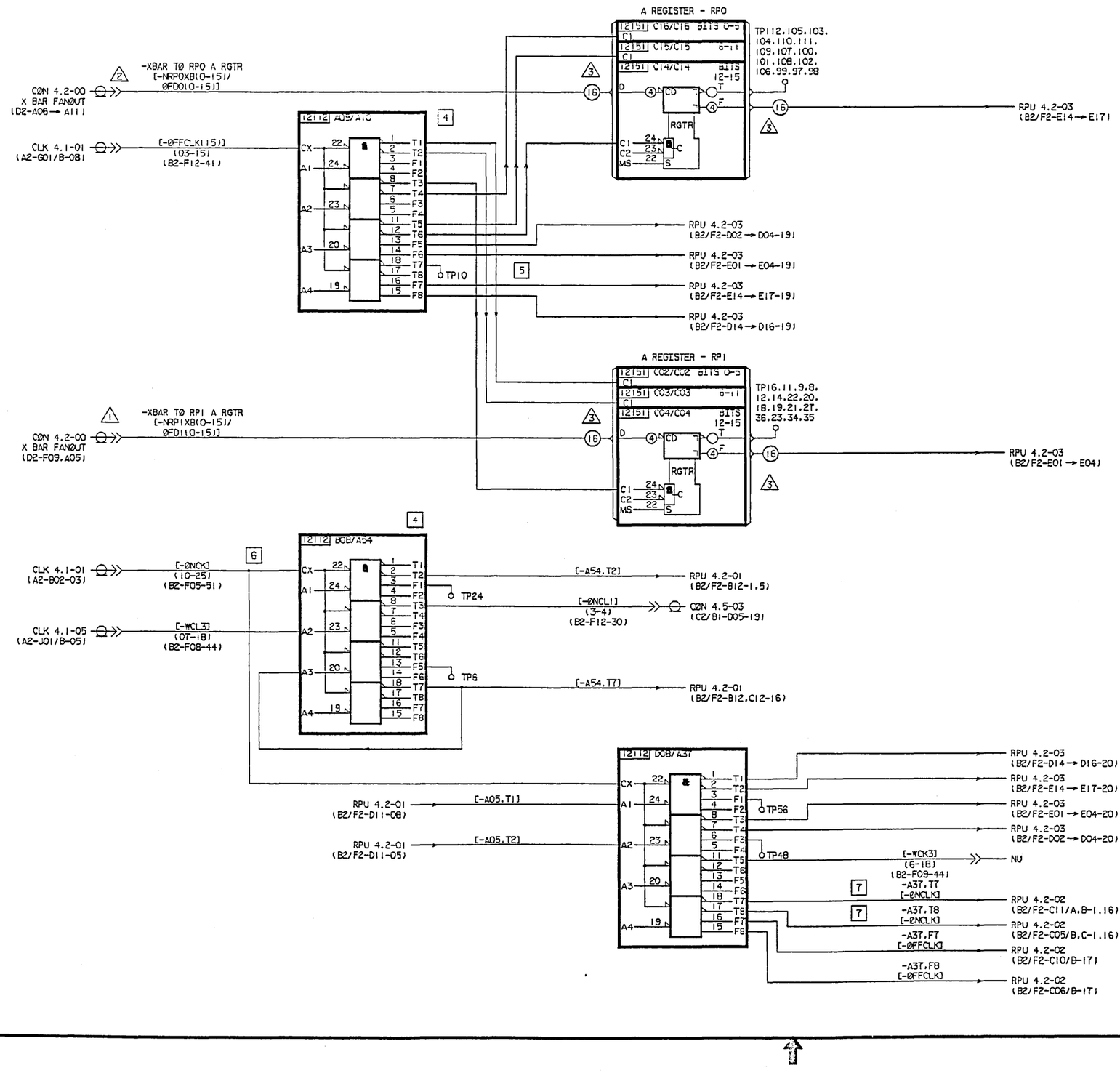
+CLR RPIN RGTR [-CLRRPI] (10-09) (B2-J05-35) RPU 4.1-00 (B2-H14-27)

12117 A04/A1SC-C/C

RPU 4.1-20 (B2/J2-B04-01) -DEL CLK D1

H

TP35



NØTES:

1

BIT	AUX	LSI	BIT	AUX	LSI
0	1-1	B2-F14-27	8	2-3	B2-F13-29
1	1-3	B2-F14-29	9	2-4	B2-F13-30
2	3-26	B2-F12-52	10	2-1	B2-F13-27
3	2-21	B2-F13-47	11	2-8	B2-F13-34
4	2-25	B2-F13-51	12	3-6	B2-F12-32
5	1-4	B2-F14-30	13	3-3	B2-F12-29
6	2-7	B2-F13-33	14	3-1	B2-F12-27
7	2-6	B2-F13-32	15	4-26	B2-F11-52

2

BIT	AUX	LSI	BIT	AUX	LSI
0	13-5	B2-F02-31	8	12-7	B2-F03-33
1	13-10	B2-F02-36	9	12-6	B2-F03-32
2	13-8	B2-F02-32	10	12-8	B2-F03-34
3	13-7	B2-F02-33	11	12-9	B2-F03-35
4	13-9	B2-F02-35	12	11-8	B2-F04-34
5	13-16	B2-F02-42	13	11-7	B2-F04-33
6	12-15	B2-F03-41	14	11-6	B2-F04-32
7	12-10	B2-F03-36	15	11-3	B2-F04-29

3

12151			
BIT	D	T	F
0.6.12	2	3	4
1.7.13	1	6	5
2.8.14	20	8	7
3.9.15	19	12	11
4.10.	18	14	13
5.11.	17	16	15

4 ALL ØUTPUT LINES SHØULD RANGE BETWEEN 5-7 INCHES EXCEPT B08, FT TØ A10. THIS LINE SHØULD BE AS SHØRT AS PØSSIBLE.

5 SIGNALS A10. F5-F8 FØILS SHØULD BE 16 INCHES ± 1 INCH AT 1:1.

6 FØIL FRØM P10-25 TØ B08-22 SHØULD BE 6.5 INCHES ± 1 INCH. FØIL FRØM B08-22 TØ D08-22 SHØULD BE 3.5 INCHES ± 1 INCH.

7 THESE FØILS SHØULD BE 13.5 INCHES ± 1 INCH.

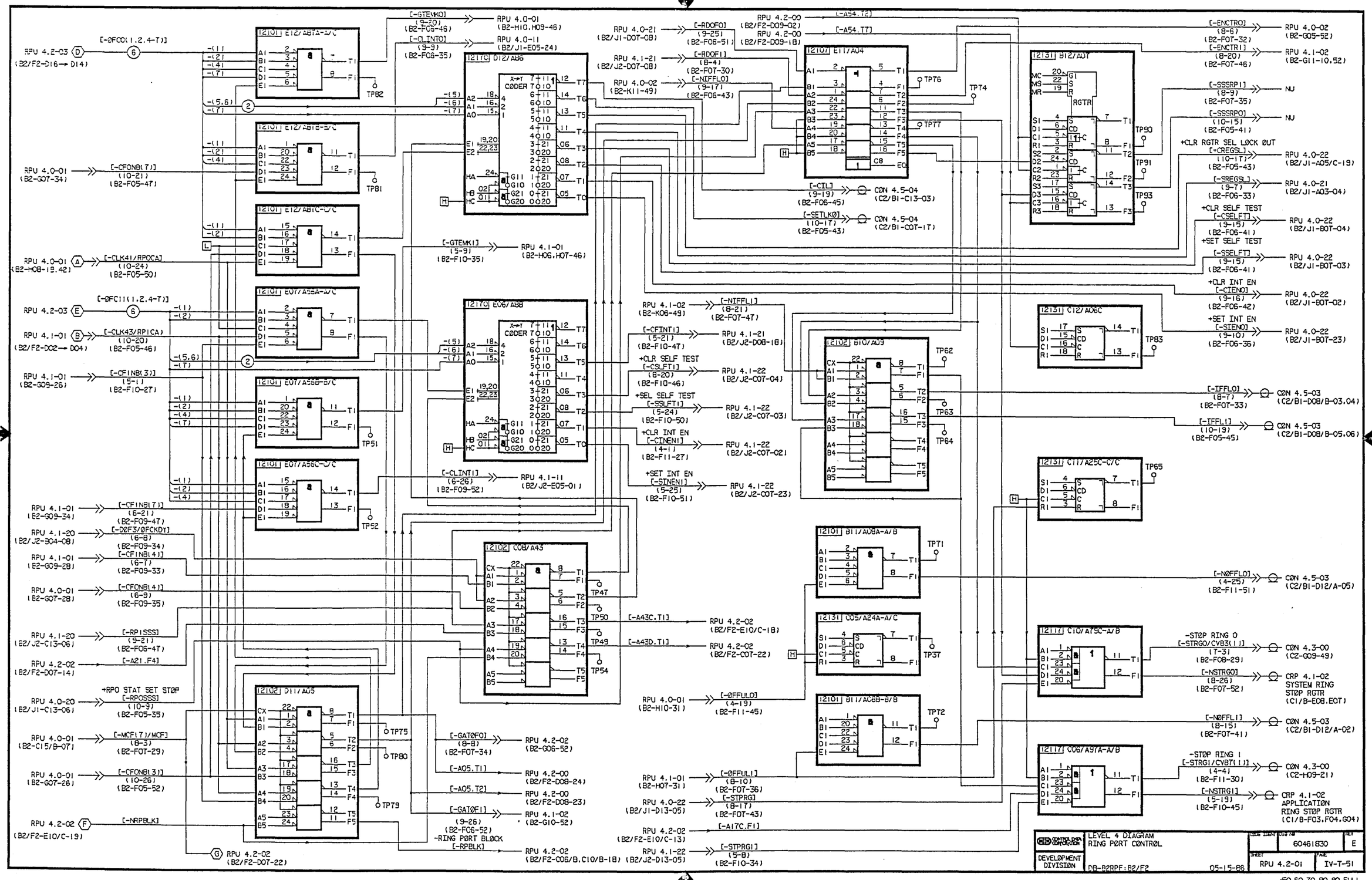
CONTROL DATA CORPORATION
DEVELOPMENT DIVISIØN

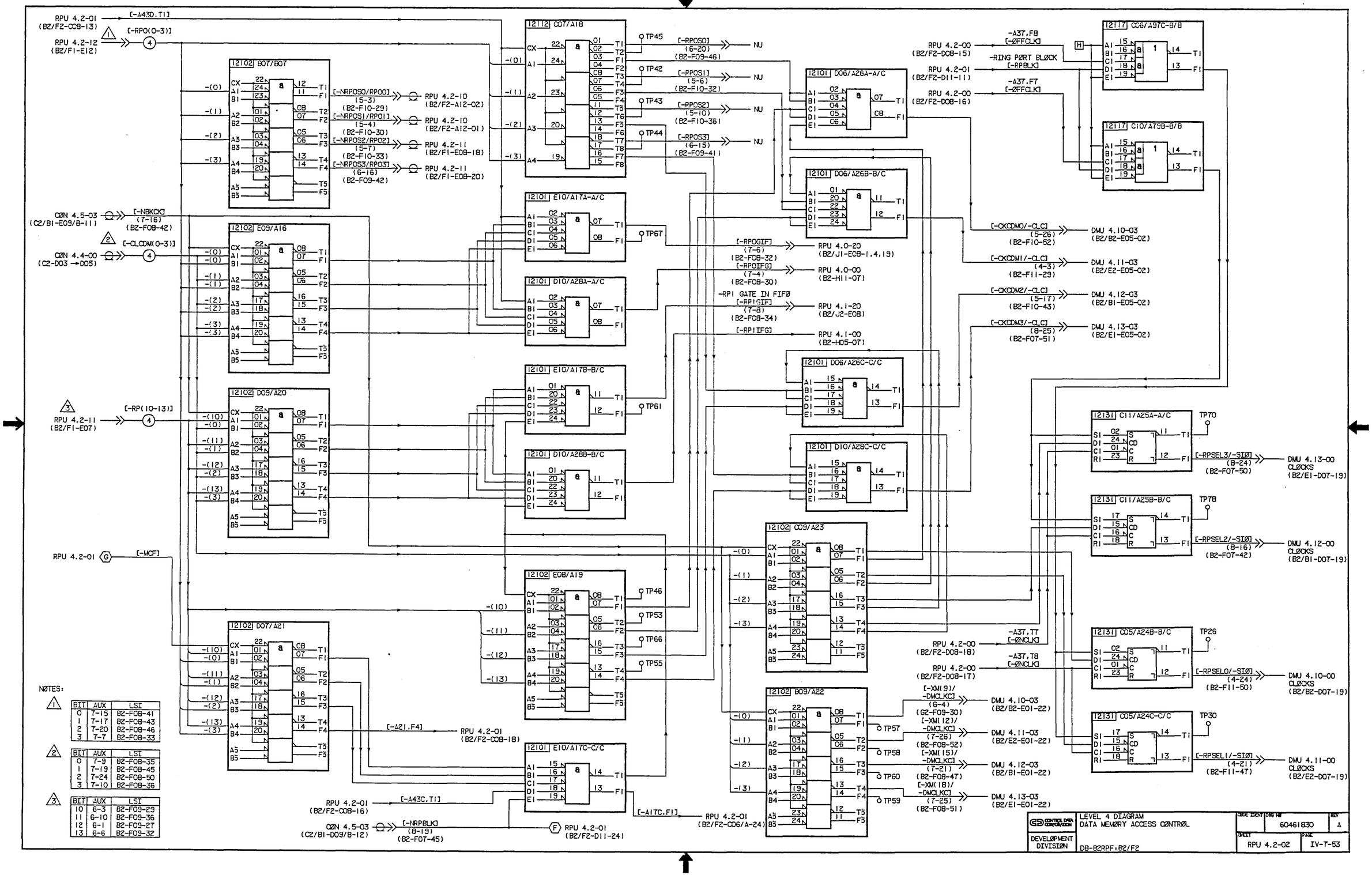
LEVEL 4 DIAGRAM
A REGISTER

DB-B2RPF:B2/F2 05-15-86

CODE IDENT NO. PART NO. 60461830 REV E
SHEET RPU 4.2-00 PAGE IV-7-49

<50 60 70 80 90 FULL>


[-0FC0(1,2,4-T)]
RPU 4.2-03 (B2/F2-D16→D14)
[-0FC1(1,2,4-T)]
RPU 4.2-03 (B2/F2-D16→D14)
RPU 4.0-01 (B2-G07-34)
[-CFONB(7)] (10-21) (B2-F05-47)
RPU 4.0-01 (B2-H08-19,42)
[-CLK41/RPOCA] (10-24) (B2-F05-50)
RPU 4.1-01 (B2/F2-D02→D04)
[-CLK43/RPICA] (10-20) (B2-F05-46)
RPU 4.1-01 (B2-G09-26)
[-CFINB(3)] (5-1) (B2-F10-27)
RPU 4.1-01 (B2-G09-34)
[-CFINB(7)] (6-21) (B2-F09-47)
RPU 4.1-20 (B2/J2-B04-08)
[-D0F3/0FCKDY] (6-8) (B2-F09-34)
RPU 4.1-01 (B2-G09-28)
[-CFINB(4)] (6-7) (B2-F09-33)
RPU 4.0-01 (B2-G07-28)
[-CFONB(4)] (6-9) (B2-F09-35)
RPU 4.1-20 (B2/J2-C13-06)
[-RPISSS] (9-21) (B2-F06-47)
RPU 4.2-02 (B2/F2-D07-14)
[-A21.F4]
+RPO STAT SET STØP
RPU 4.0-20 (B2/J1-C13-06)
[-RPOSSS] (10-9) (B2-F05-35)
RPU 4.0-01 (B2-C15/B-07)
[-MCF(7)/MCF] (8-3) (B2-F07-29)
RPU 4.0-01 (B2-G07-26)
[-CFONB(3)] (10-26) (B2-F05-52)
RPU 4.2-02 (B2/F2-E10/C-19)
[-NAPBLK]
RPU 4.2-02 (B2/F2-D07-22)
[-GTEMK0] (9-20) (B2-F06-46)
RPU 4.0-01 (B2-H10,H09-46)
[-CLINT0] (9-9) (B2-F06-35)
RPU 4.0-11 (B2/J1-E05-24)
[-GTEMK1] (5-9) (B2-F10-35)
RPU 4.1-01 (B2-H06,H07-46)
[-CLINT1] (6-26) (B2-F09-52)
RPU 4.1-11 (B2/J2-E05-01)
RPU 4.0-21 (B2/J1-D07-08)
[-RDOF0] (9-25) (B2-F06-51)
RPU 4.1-21 (B2/J2-D07-08)
[-RDOF1] (8-4) (B2-F07-30)
RPU 4.0-02 (B2-K11-49)
[-NIFFL0] (9-17) (B2-F06-43)
RPU 4.2-00 (B2/F2-D09-02)
[-A54.T2]
RPU 4.2-00 (B2/F2-D09-18)
[-A54.T7]
[-CIL] (9-19) (B2-F06-45)
C0N 4.5-04 (C2/B1-C13-03)
[-SETLK0] (10-17) (B2-F05-43)
C0N 4.5-04 (C2/B1-C07-17)
RPU 4.1-02 (B2-K06-49)
[-NIFFL1] (8-21) (B2-F07-47)
[-CFINT1] (5-21) (B2-F10-47)
RPU 4.1-21 (B2/J2-D08-18)
+CLR SELF TEST
[-CSLFT1] (8-20) (B2-F10-46)
RPU 4.1-22 (B2/J2-C07-04)
+SEL SELF TEST
[-SSLFT1] (5-24) (B2-F10-50)
RPU 4.1-22 (B2/J2-C07-03)
+CLR INT EN
[-CINEN1] (4-11) (B2-F11-27)
RPU 4.1-22 (B2/J2-C07-02)
+SET INT EN
[-SINEN1] (5-25) (B2-F10-51)
RPU 4.1-22 (B2/J2-C07-23)
[-A43C.T1]
RPU 4.2-02 (B2/F2-E10/C-18)
[-A43D.T1]
RPU 4.2-02 (B2/F2-C07-22)
RPU 4.0-01 (B2-H10-31)
[-0FFUL0] (4-19) (B2-F11-45)
[-GAT0F0] (8-8) (B2-F07-34)
RPU 4.2-02 (B2-G06-52)
[-A05.T1]
RPU 4.2-00 (B2/F2-D08-24)
[-A05.T2]
RPU 4.2-00 (B2/F2-D08-23)
[-GAT0F1] (9-26) (B2-F06-52)
RPU 4.1-02 (B2-G10-52)
-RING PØRT BLØCK
[-RPBLK]
RPU 4.2-02 (B2/F2-C06/B,C10/B-18)
RPU 4.1-01 (B2-H07-31)
[-0FFUL1] (8-10) (B2-F07-36)
RPU 4.0-22 (B2/J1-D13-05)
[-STPRG] (8-17) (B2-F07-43)
RPU 4.2-02 (B2/F2-E10/C-13)
[-A17C.F1]
RPU 4.1-22 (B2/J2-D13-05)
[-STPRG1] (5-8) (B2-F10-34)
[-ENCTR0] (8-6) (B2-F07-32)
RPU 4.0-02 (B2-G05-52)
[-ENCTR1] (8-20) (B2-F07-46)
RPU 4.1-02 (B2-G11-10,52)
[-SSSRP1] (8-9) (B2-F07-35)
NU
[-SSSRP0] (10-15) (B2-F05-41)
NU
+CLR RGTR SEL LØCK ØUT
[-CREGSL] (10-17) (B2-F05-43)
RPU 4.0-22 (B2/J1-A05/C-19)
[-SREGSL] (9-7) (B2-F06-33)
RPU 4.0-21 (B2/J1-A03-04)
+CLR SELF TEST
[-CSELFT] (9-15) (B2-F06-41)
RPU 4.0-22 (B2/J1-B07-04)
+SET SELF TEST
[-SSELFT] (9-15) (B2-F06-41)
RPU 4.0-22 (B2/J1-B07-03)
+CLR INT EN
[-CIEN0] (9-16) (B2-F06-42)
RPU 4.0-22 (B2/J1-B07-02)
+SET INT EN
[-SIEN0] (9-10) (B2-F06-36)
RPU 4.0-22 (B2/J1-B07-23)
[-IFFL0] (8-7) (B2-F07-33)
C0N 4.5-03 (C2/B1-D08/B-03,04)
[-IFFL1] (10-19) (B2-F05-45)
C0N 4.5-03 (C2/B1-D08/B-05,06)
[-NØFFL0] (4-25) (B2-F11-51)
C0N 4.5-03 (C2/B1-D12/A-05)
[-NØFFL1] (8-15) (B2-F07-41)
C0N 4.5-03 (C2/B1-D12/A-02)
-STØP RING 0
[-STRG0/CVB3(1)] (7-3) (B2-F08-29)
C0N 4.3-00 (C2-G09-49)
[-NSTRG0] (8-26) (B2-F07-52)
CRP 4.1-02 SYSTEM RING STØP RGTR (C1/B-E08.E07)
-STØP RING 1
[-STRG1/CVB7(1)] (4-4) (B2-F11-30)
C0N 4.3-00 (C2-H09-21)
[-NSTRG1] (5-19) (B2-F10-45)
CRP 4.1-02 APPLICATION RING STØP RGTR (C1/B-F03,F04,G04)
TP82
TP81
TP51
TP52
TP80
TP79
TP4T
TP50
TP49
TP54
TP75
TP76
TP74
TP77
TP90
TP91
TP93
TP83
TP62
TP63
TP64
TP65
TP71
TP37
TP72
LEVEL 4 DIAGRAM
RING PØRT CØNTRØL
DEVELØPMENT DIVISIØN
DB-B2RPF:B2/F2
05-15-86
60461830
E
RPU 4.2-01
IV-T-51
<50 60 70 80 90 FULL



NØTES:

1

BIT	AUX	LSI
0	T-15	B2-F08-41
1	T-17	B2-F08-43
2	T-20	B2-F08-46
3	T-7	B2-F08-33

2

BIT	AUX	LSI
0	T-9	B2-F08-35
1	T-19	B2-F08-45
2	T-24	B2-F08-50
3	T-10	B2-F08-36

3

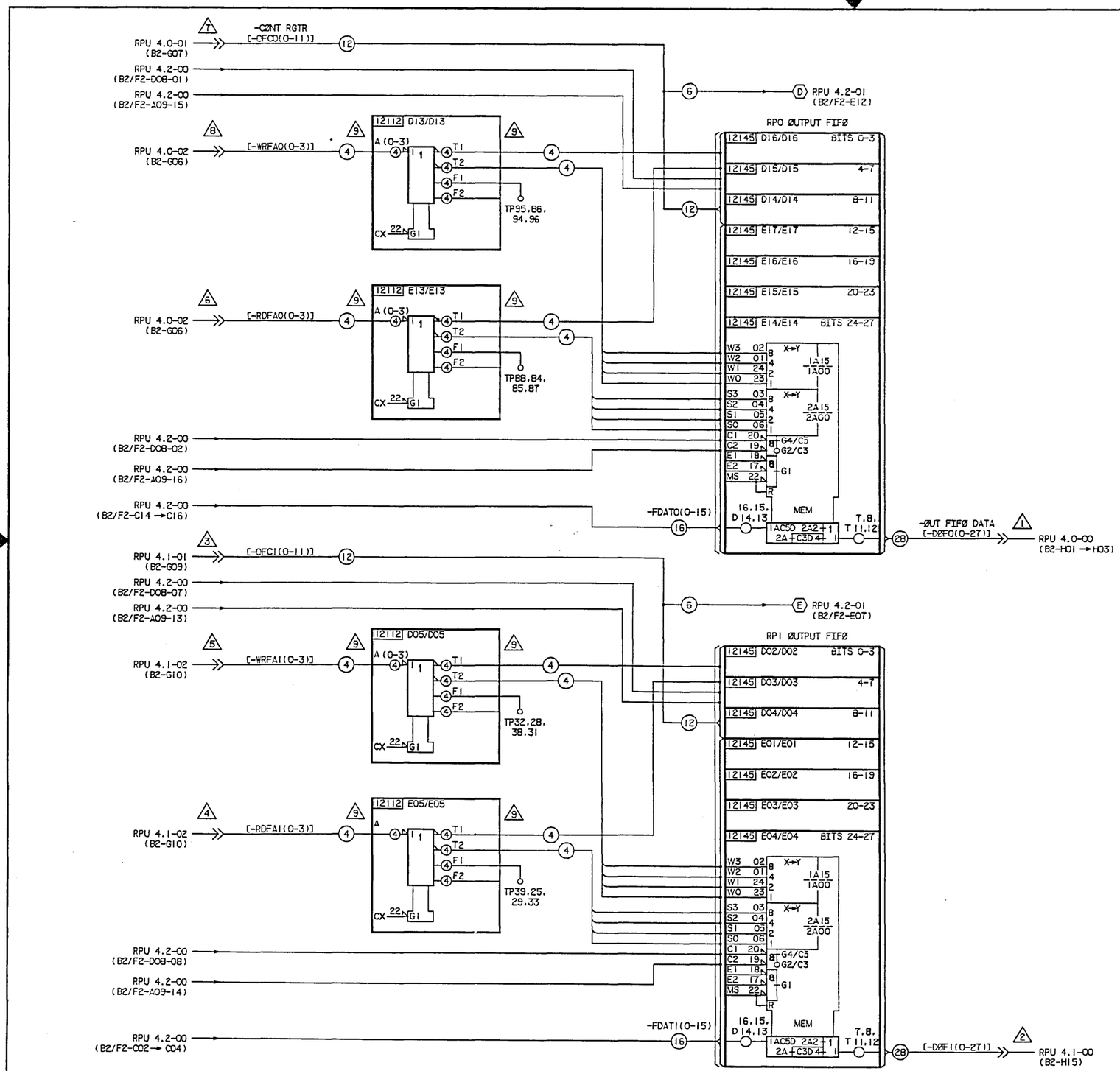
BIT	AUX	LSI
10	G-3	B2-F09-29
11	G-10	B2-F09-36
12	G-1	B2-F09-27
13	G-6	B2-F09-32

CONTROL DATA CORPORATION — DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
DATA MEMØRY ACCESS CØNTRØL
DB-B2RPF:B2/F2

CODE IDENT | DWG NØ | REV
60461830 | A

SHEET: RPU 4.2-02 | SIZE: IV-7-53



NØTES:

1

BIT	AUX	LSI
0	12-3	B2-F03-29
1	13-19	B2-F02-45
2	12-1	B2-F03-27
3	12-4	B2-F03-30
4	12-21	B2-F03-47
5	12-19	B2-F03-45
6	11-1	B2-F04-27
7	11-4	B2-F04-30
8	11-25	B2-F04-51
9	11-17	B2-F04-43
10	11-26	B2-F04-52
11	10-4	B2-F05-30
12	13-6	B2-F02-32
13	13-4	B2-F02-30
14	13-3	B2-F02-29
15	13-1	B2-F02-27
16	13-24	B2-F02-50
17	13-20	B2-F02-46
18	13-26	B2-F02-52
19	13-25	B2-F02-51
20	12-25	B2-F03-51
21	12-26	B2-F03-52
22	12-24	B2-F03-50
23	12-20	B2-F03-46
24	11-24	B2-F04-50
25	11-20	B2-F04-46
26	11-21	B2-F04-47
27	11-19	B2-F04-45

2

BIT	AUX	LSI
0	1-10	B2-F14-36
1	1-7	B2-F14-33
2	1-19	B2-F14-45
3	1-20	B2-F14-46
4	2-19	B2-F13-45
5	2-10	B2-F13-36
6	2-24	B2-F13-50
7	2-9	B2-F13-35
8	3-26	B2-F12-52
9	3-24	B2-F12-50
10	3-25	B2-F12-51
11	3-16	B2-F12-42
12	2-26	B2-F13-52
13	1-25	B2-F14-51
14	1-24	B2-F14-50
15	1-21	B2-F14-47
16	1-17	B2-F14-43
17	1-16	B2-F14-42
18	1-15	B2-F14-41
19	1-9	B2-F14-35
20	2-20	B2-F14-46
21	2-16	B2-F13-42
22	2-17	B2-F13-43
23	2-15	B2-F13-41
24	3-20	B2-F12-46
25	3-17	B2-F12-43
26	3-19	B2-F12-45
27	3-21	B2-F12-47

3

BIT	AUX	LSI	BIT	AUX	LSI
0	1-6	B2-F14-32	6	5-16	B2-F10-42
1	6-24	B2-F09-50	7	6-17	B2-F09-43
2	6-25	B2-F09-51	8	3-7	B2-F12-33
3	1-8	B2-F14-34	9	3-8	B2-F12-34
4	6-19	B2-F09-45	10	3-9	B2-F12-35
5	5-15	B2-F10-41	11	3-10	B2-F12-36

4

BIT	AUX	LSI
0	4-10	B2-F11-36
1	4-8	B2-F11-34
2	4-9	B2-F11-35
3	4-16	B2-F11-42

5

BIT	AUX	LIS
0	4-15	B2-F11-41
1	4-7	B2-F11-33
2	4-17	B2-F11-43
3	4-6	B2-F11-32

6

BIT	AUX	LSI
0	10-10	B2-F05-36
1	10-7	B2-F05-33
2	10-1	B2-F05-27
3	10-3	B2-F05-29

7

BIT	AUX	LSI	BIT	AUX	LSI
0	13-17	B2-F02-43	6	12-17	B2-F03-43
1	9-4	B2-F06-30	7	9-6	B2-F06-32
2	9-3	B2-F06-29	8	11-9	B2-F04-35
3	13-21	B2-F02-47	9	11-10	B2-F04-36
4	9-1	B2-F06-27	10	11-15	B2-F04-41
5	12-16	B2-F03-42	11	11-16	B2-F04-42

8

BIT	AUX	LSI
0	10-9	B2-F05-35
1	10-6	B2-F05-32
2	10-16	B2-F05-42
3	10-8	B2-F05-34

9

BIT	A	T1	T2	F1	F2
0	24	1	2	3	4
1	23	8	7	6	5
2	20	11	12	13	14
3	19	18	17	16	15

CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
ØUTPUT FIFØ

DB-B2RPF:B2/F2

CODE IDENT
DWG NO 60461830
REV A
SHEET RPU 4.2-03
PAGE IV-7-55

3

BUS	[-DM0C(0-11)]		[-DM1C(0-11)]		[-DM2C(0-11)]		[-DM3C(0-11)]		[-XMC]	
BIT	AUX	LSI	AUX	LSI	AUX	LSI	AUX	LSI	AUX	LSI
0	13-06	B2-F14-06	13-24	B2-F14-24	1-07	B2-F02-07	1-17	B2-F02-17	12-17	B2-F13-17
1	13-03	B2-F14-03	13-25	B2-F14-25	1-10	B2-F02-10	1-24	B2-F02-24	12-15	B2-F13-15
2	13-04	B2-F14-04	13-20	B2-F14-20	1-25	B2-F02-25	1-26	B2-F02-26	12-16	B2-F13-16
3	13-08	B2-F14-08	13-21	B2-F14-21	1-21	B2-F02-21	1-19	B2-F02-19	12-10	B2-F13-10
4	13-10	B2-F14-10	12-01	B2-F13-01	1-03	B2-F02-03	1-09	B2-F02-09	12-20	B2-F13-20
5	13-09	B2-F14-09	12-03	B2-F13-03	2-25	B2-F03-25	1-16	B2-F02-16	11-06	B2-F12-06
6	13-01	B2-F14-01	13-26	B2-F14-26	1-06	B2-F02-06	1-15	B2-F02-15	11-03	B2-F12-03
7	13-07	B2-F14-07	12-04	B2-F13-04	1-01	B2-F02-01	1-20	B2-F02-20	12-19	B2-F13-19
8	13-17	B2-F14-17	12-08	B2-F13-08	2-17	B2-F03-17	1-04	B2-F02-04	12-24	B2-F13-24
9	13-19	B2-F14-19	12-09	B2-F13-09	2-20	B2-F03-20	2-26	B2-F03-26	11-07	B2-F12-07
10	13-15	B2-F14-15	12-06	B2-F13-06	2-24	B2-F03-24	2-21	B2-F03-21	11-08	B2-F12-08
11	13-16	B2-F14-16	12-07	B2-F13-07	2-19	B2-F03-19	1-08	B2-F02-08	12-21	B2-F13-21

4

BUS	[-DM0D(0-15)/-RD]		[-DM1D(0-15)/-RD]		[-DM2D(0-15)/-RD]		[-DM3D(0-15)/-RD]		[-XMD(0-15)]	
BIT	AUX	LSI	AUX	LSI	AUX	LSI	AUX	LSI	AUX	LSI
0	8-25	B2-F09-25	7-15	B2-F08-15	5-24	B2-F06-24	3-15	B2-F04-15	10-20	B2-F11-20
1	8-03	B2-F09-03	7-04	B2-F08-04	6-06	B2-F07-06	3-06	B2-F04-06	10-19	B2-F11-19
2	8-26	B2-F09-26	7-24	B2-F08-24	6-04	B2-F07-04	3-09	B2-F04-09	10-09	B2-F11-09
3	7-26	B2-F08-26	7-25	B2-F08-25	5-19	B2-F06-19	3-17	B2-F04-17	10-10	B2-F11-10
4	8-19	B2-F09-19	7-21	B2-F08-21	5-06	B2-F06-06	3-08	B2-F04-08	9-08	B2-F10-08
5	8-24	B2-F09-24	7-07	B2-F08-07	6-03	B2-F07-03	4-19	B2-F05-19	9-16	B2-F10-16
6	8-17	B2-F09-17	7-01	B2-F08-01	6-08	B2-F07-08	3-16	B2-F04-16	10-26	B2-F11-26
7	8-21	B2-F09-21	6-16	B2-F07-16	5-16	B2-F06-16	3-04	B2-F04-04	10-25	B2-F11-25
8	8-15	B2-F09-15	7-19	B2-F08-19	6-26	B2-F07-26	4-20	B2-F05-20	10-24	B2-F11-24
9	8-07	B2-F09-07	7-06	B2-F08-06	6-10	B2-F07-10	4-24	B2-F05-24	10-21	B2-F11-21
10	8-10	B2-F09-10	7-16	B2-F08-16	6-17	B2-F07-17	5-25	B2-F06-25	9-26	B2-F10-26
11	8-20	B2-F09-20	7-17	B2-F08-17	6-25	B2-F07-25	4-26	B2-F05-26	9-21	B2-F10-21
12	8-16	B2-F09-16	7-10	B2-F08-10	6-21	B2-F07-21	4-04	B2-F05-04	9-25	B2-F10-25
13	8-08	B2-F09-08	7-03	B2-F08-03	6-07	B2-F07-07	5-26	B2-F06-26	8-04	B2-F09-04
14	8-06	B2-F09-06	7-08	B2-F08-08	6-01	B2-F07-01	5-21	B2-F06-21	9-24	B2-F10-24
15	8-09	B2-F09-09	7-09	B2-F08-09	6-19	B2-F07-19	4-16	B2-F05-16	9-20	B2-F10-20

5

12155				
BIT	IN		ØUT	
	A	B	T	F
0.4.8.12	2	1	8	7
1.5.9.13	4	3	5	6
2.6.10.14	16	15	13	14
3.7.11.15	8	7	12	11

6

ALL ØUTPUTS MUST STAY WITHIN A RANGE ØF 5 INCHES - T INCHES.
EXCEPT E10, F1, THIS LINE SHØULD BE AS SHØRT AS PØSSIBLE.

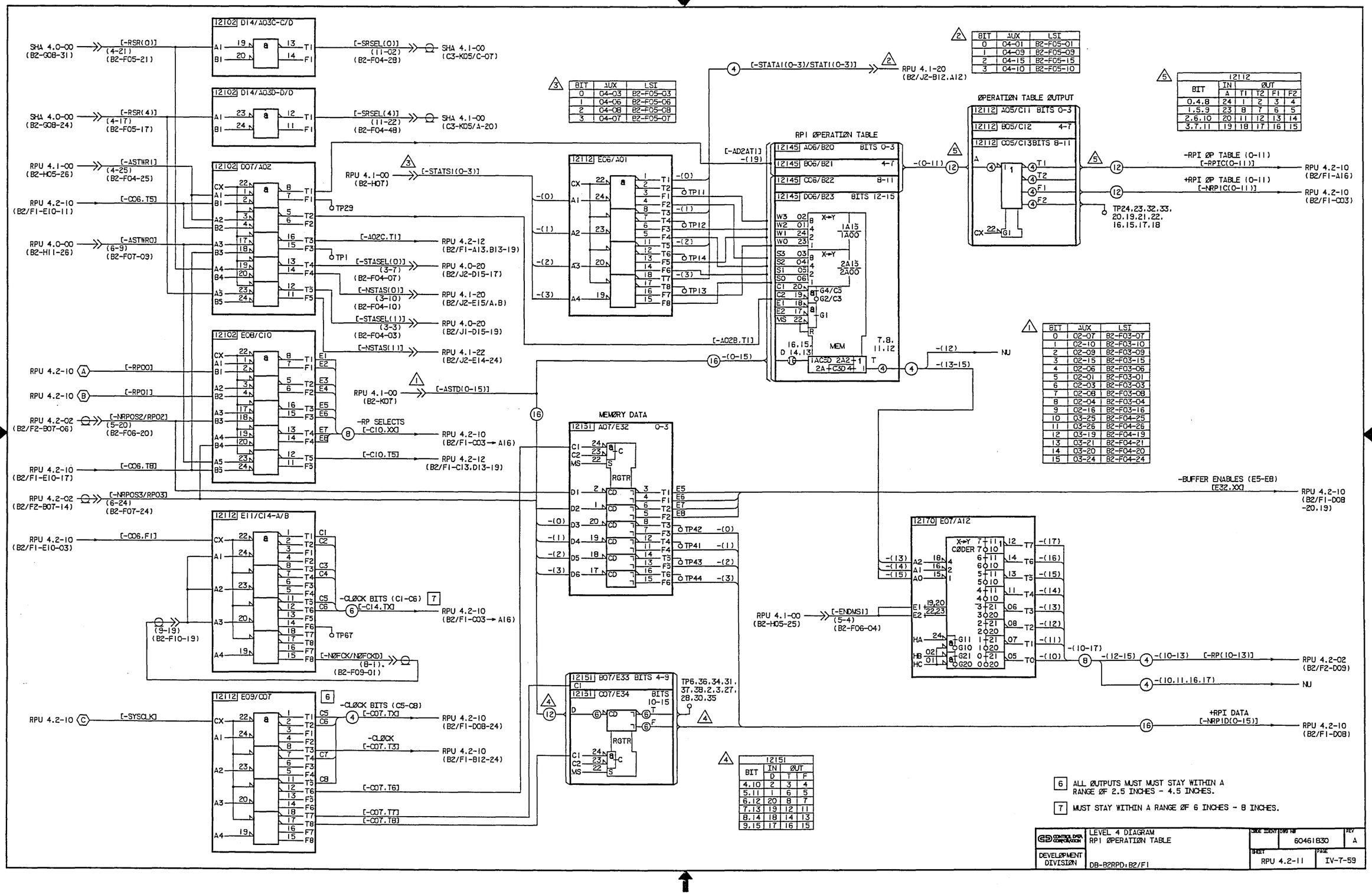
1

12112				
BIT	IN	ØUT		
	Δ	T1	T2	F1	F2
0.4.8	24	1	2	3	4
1.5.9	23	8	7	6	5
2.6.10	20	11	12	13	14
3.7.11	19	18	17	16	15

2

12151			
BIT	IN	ØUT	
	D	T	F
4.10	2	3	4
5.11	1	6	5
6.12	20	8	7
7.13	19	12	11
8.14	18	14	13
9.15	17	16	15

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM RPØ ØPERATIØN TABLE ØUTPUT RING ØUTPUT BUFFER MEMØRY DATA D8-B2RPD;B2/F1	CODE IDENT 60461830	REV A
DEVELØPMENT DIVISIØN		SHEET RPU 4.2-10	PAGE IV-7-57



BIT	AUX	LSI
0	04-01	B2-F05-01
1	04-09	B2-F05-09
2	04-15	B2-F05-15
3	04-10	B2-F05-10

BIT	AUX	LSI
0	04-03	B2-F05-03
1	04-06	B2-F05-06
2	04-08	B2-F05-08
3	04-07	B2-F05-07

BIT	IN	ØUT		
	A	T1	T2	F1	F2
0,4,8	24	1	2	3	4
1,5,9	23	8	7	6	5
2,6,10	20	11	12	13	14
3,7,11	19	18	17	16	15

12112

BIT	AUX	LSI
0	02-07	B2-F03-07
1	02-10	B2-F03-10
2	02-09	B2-F03-09
3	02-15	B2-F03-15
4	02-06	B2-F03-06
5	02-01	B2-F03-01
6	02-03	B2-F03-03
7	02-08	B2-F03-08
8	02-04	B2-F03-04
9	02-16	B2-F03-16
10	03-25	B2-F04-25
11	03-26	B2-F04-26
12	03-19	B2-F04-19
13	03-21	B2-F04-21
14	03-20	B2-F04-20
15	03-24	B2-F04-24

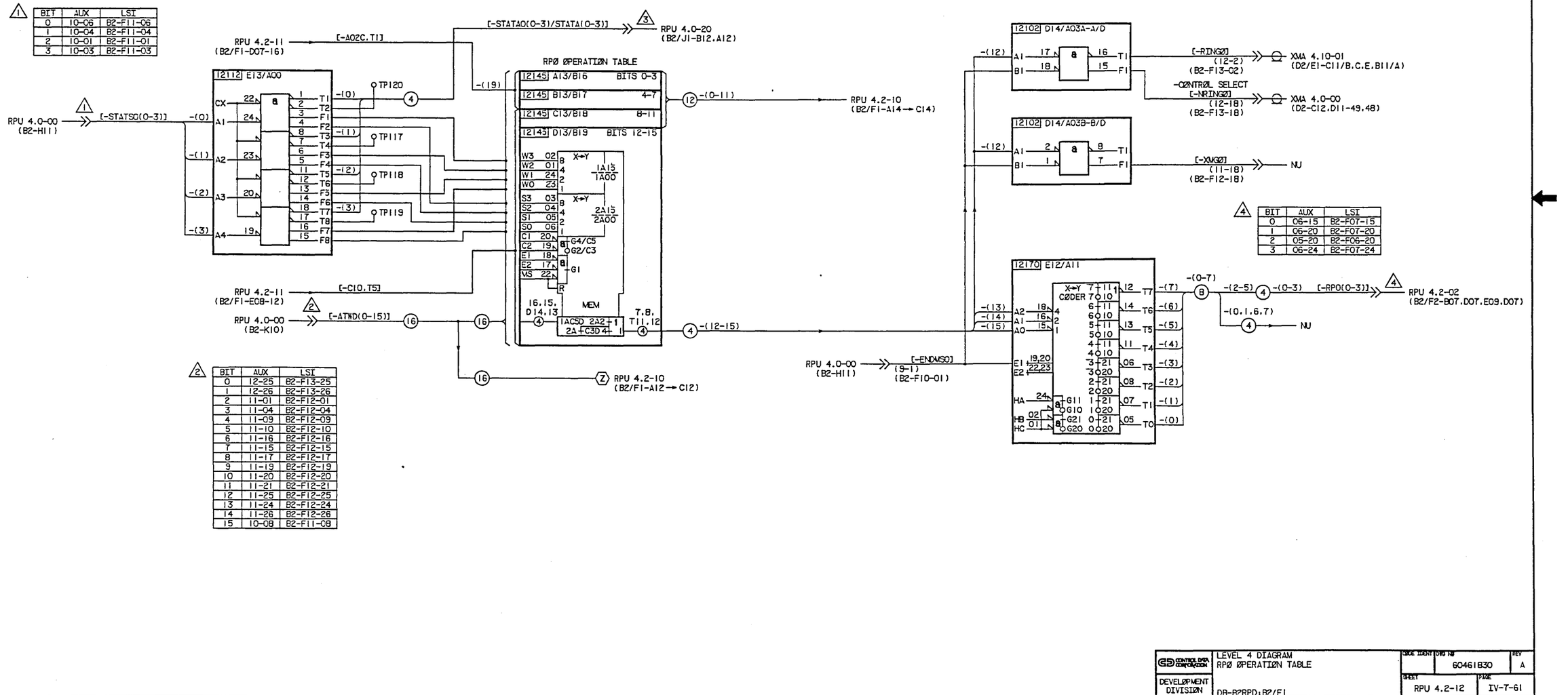
12151

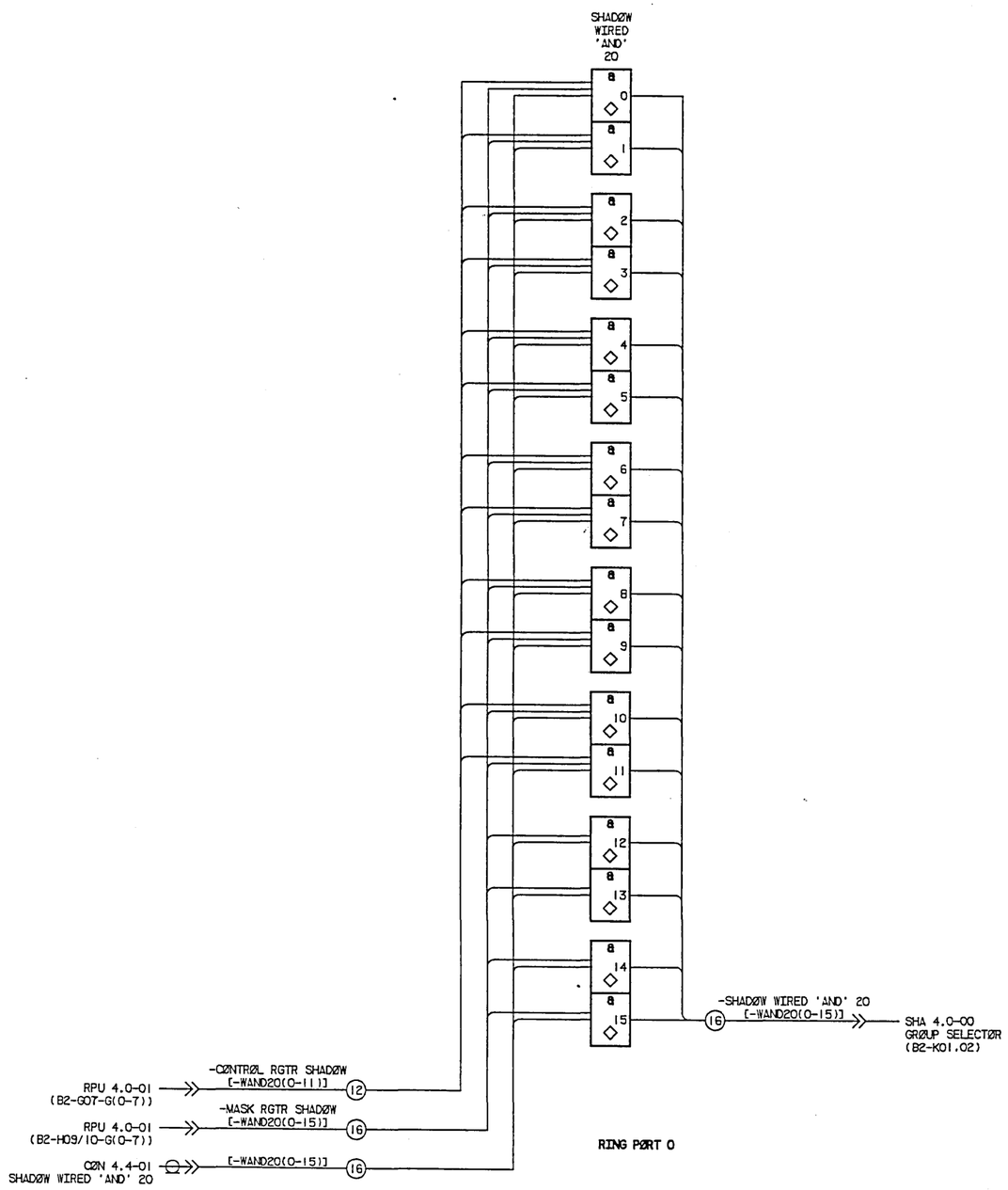
BIT	IN	ØUT	
	D	T	F
4,10	2	3	4
5,11	1	6	5
6,12	20	8	7
7,13	19	12	11
8,14	18	14	13
9,15	17	16	15

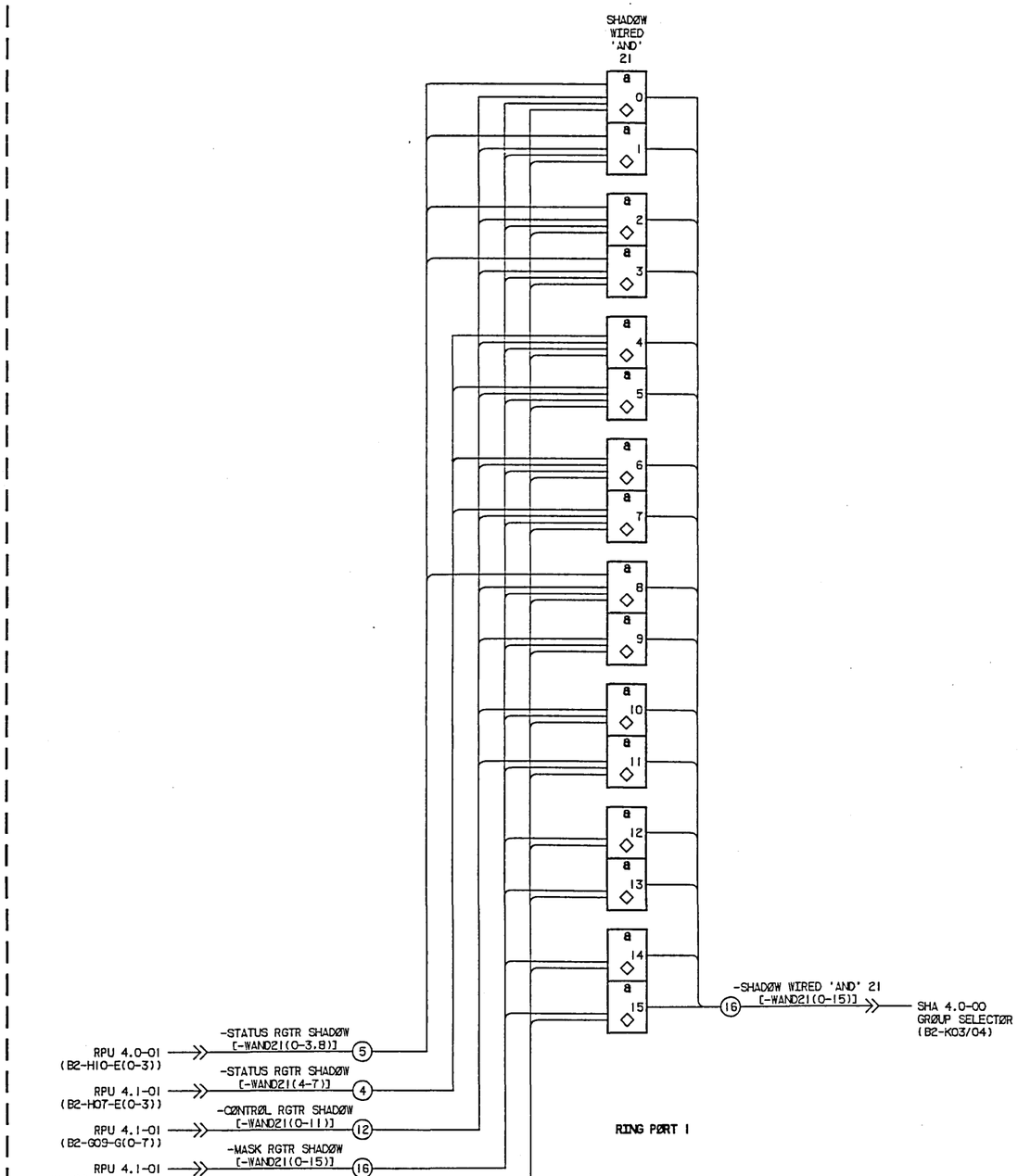
6 ALL ØUTPUTS MUST MUST STAY WITHIN A RANGE ØF 2.5 INCHES - 4.5 INCHES.

7 MUST STAY WITHIN A RANGE ØF 6 INCHES - 8 INCHES.

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM RPI ØPERATIØN TABLE	SIZE IDENT DWG NO 60461830	REV A
DEVELØPMENT DIVISIØN	DB-B2RPD:B2/F1	SHEET RPU 4.2-11	PAGE IV-7-59


1
BIT | AUX | LSI
0 | 10-06 | B2-F11-06
1 | 10-04 | B2-F11-04
2 | 10-01 | B2-F11-01
3 | 10-03 | B2-F11-03
3
BIT | AUX | LSI
0 | 10-07 | B2-F11-07
1 | 10-16 | B2-F11-16
2 | 10-17 | B2-F11-17
3 | 10-15 | B2-F11-15
RPU 4.0-00 (B2-H11)
[-STATSO(0-3)]
RPU 4.2-11 (B2/F1-D07-16)
[-A02C.T1]
[-STATAO(0-3)/STATA(0-3)]
RPU 4.0-20 (B2/J1-B12,A12)
12112 E13/A00
RPØ ØPERATIØN TABLE
12145 A13/B16 BITS 0-3
12145 B13/B17 4-7
12145 C13/B18 8-11
12143 D13/B19 BITS 12-15
TP120
TP117
TP118
TP119
RPU 4.2-10 (B2/F1-A14→C14)
RPU 4.2-11 (B2/F1-E08-12)
[-C10.T5]
RPU 4.0-00 (B2-K10)
[-ATWD(0-15)]
RPU 4.2-10 (B2/F1-A12→C12)
2
BIT | AUX | LSI
0 | 12-25 | B2-F13-25
1 | 12-26 | B2-F13-26
2 | 11-01 | B2-F12-01
3 | 11-04 | B2-F12-04
4 | 11-09 | B2-F12-09
5 | 11-10 | B2-F12-10
6 | 11-16 | B2-F12-16
7 | 11-15 | B2-F12-15
8 | 11-17 | B2-F12-17
9 | 11-19 | B2-F12-19
10 | 11-20 | B2-F12-20
11 | 11-21 | B2-F12-21
12 | 11-25 | B2-F12-25
13 | 11-24 | B2-F12-24
14 | 11-26 | B2-F12-26
15 | 10-08 | B2-F11-08
12102 D14/A03A-A/D
12102 D14/A03B-B/D
[-RINGØ] (12-2) (B2-F13-02)
XMA 4.10-01 (D2/E1-C11/B.C.E.B11/A)
-CØNTRØL SELECT
[-NRINGØ] (12-18) (B2-F13-18)
XMA 4.0-00 (D2-C12.D11-49,48)
[-XMGØ] (11-18) (B2-F12-18)
NU
4
BIT | AUX | LSI
0 | 06-15 | B2-F07-15
1 | 06-20 | B2-F07-20
2 | 05-20 | B2-F06-20
3 | 06-24 | B2-F07-24
12170 E12/A11
RPU 4.0-00 (B2-H11)
[-ENDWSO] (9-1) (B2-F10-01)
[-RPO(0-3)]
RPU 4.2-02 (B2/F2-B07.D07.E09.D07)
NU
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
RPØ ØPERATIØN TABLE
DB-B2RPD:B2/F1
CODE IDENT NO 60461830
REV A
SHEET RPU 4.2-12
PAGE IV-7-61





CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM RING PØRT UNIT 0 & 1 SHADØW WIRED 'AND' 20 & 21	CODE IDENT	DWG NO: 60461830 REV: A
DEVELØPMENT DIVISIØN	DB-B2RPU:B2	SHEET: RPU 4.3-00	PAGE: IV-7-63

8. SHIFT/BOOLEAN UNIT (SBU)

SYSTEM FUNCTION

The shift/Boolean functional unit, which is located in the base processor, performs shift and any of 16 bit-logical operations on operands taken from the crossbar and returns the results to the crossbar.

GENERAL DESCRIPTION

There are two shift/Boolean units in the base processor, each with four crossbar inputs and one crossbar output. Each unit performs shift operations on 16- or 32-bit operands during the first part of a clock cycle. During the last part of the clock cycle, the selected logical operation is performed. Therefore, the shift and Boolean operations can be performed serially in one clock cycle.

LOCATION

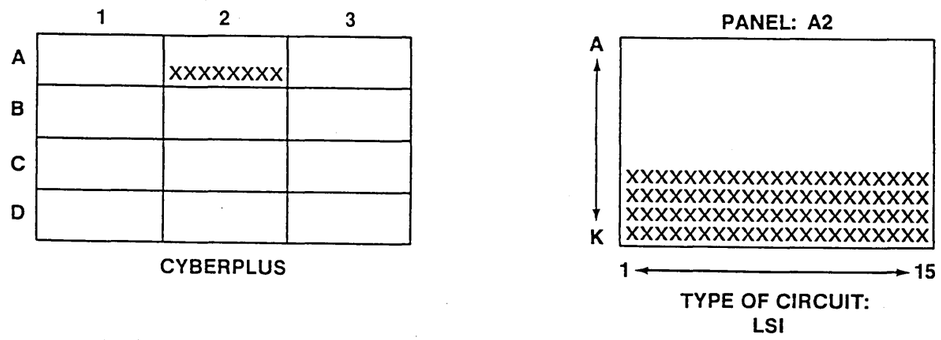


Figure IV-8-1. Location of Shift/Boolean Unit Logic Circuits

FUNCTIONAL DESCRIPTION

The discussion in the following paragraphs refers to the simplified block diagram of the shift/Boolean unit as shown in figure IV-8-2 and the level 2 diagrams SBU 2.0 and SBU 2.1. The control register receives the 12-bit operation code from the 16-bit dynamic control field of the instruction word. The bits of the operation code determine what function the shift/Boolean unit will perform.

The four input registers receive data from the crossbar when enabled by the A, B, C, or D clocks. The clocks are set by the program into the clock control field of the instruction word, bits 25 through 28 (clocks A, D, B, C, respectively) for S/B unit 0. Bits 29 through 32 are for S/B unit 1. Bit 25 (or 29), when set, gates data from crossbar output 13 for S/B 0, (17 for S/B 1) into the S register (primary shift operand). Bit 26 (or 30), when set, gates data from crossbar output 15 for S/B 0, (14 for S/B 1) into the D register (double-shift operand). Bit 27 (or 31), when set, gates data from crossbar output 16 for S/B 0, (3 for S/B 1) into the B register (Boolean operand) and the C register (compare). Bit 28 (or 32), when set, gates the four least significant bits from crossbar output 14 for S/B 0, (15 for S/B 1) into the SC register (4-bit shift count). The clock bits gate the data at time 0 of clock cycle one when they are set. If the clock bits are clear, the contents of the various registers are not changed. (Note the double usage of the lower 4-bits of crossbar outputs 14 and 15. It allows the simultaneous gating of a 32-bit word and the 4-bit shift count at the beginning of a double-shift operation -- but in one shift/Boolean unit only.)

The shift network performs 16- or 32-bit right shift operations during the first part of the second clock cycle with the shift count specifying the number of shifts. No left shifts are performed. The S register provides the data for the 16-bit shifts and the lower (primary) 16-bits for the double-shifts. The D register holds the upper 16-bits for a double-shift, only. Sixteen lines feed the results of the shift to the shift latch at clock cycle one plus one half. For a double-shift, that means that only the least significant 16-bits are used.

The Boolean network executes one of the 16 bit-logical operations during the last half of the second clock cycle. The data sources for the operations are the B register and the output of the shift network. Each Boolean operation uses a bit-by-bit examination of matching bits from the two 16-bit data sources to produce the logical results. All results from the Boolean network are available from the output register at time 0 of clock cycle two.

The Boolean network output is gated into the output register and then provided to the crossbar and the compare network. The other compare network input comes from the compare register. It can only be loaded with a new value at the same time that the control register is loaded with an operation code having the compare control bit set to a logical 1. Compares are made of the data in the output and compare registers on an 8-bit byte or 16-bit word basis, and the results are available at the start of clock cycle 0.

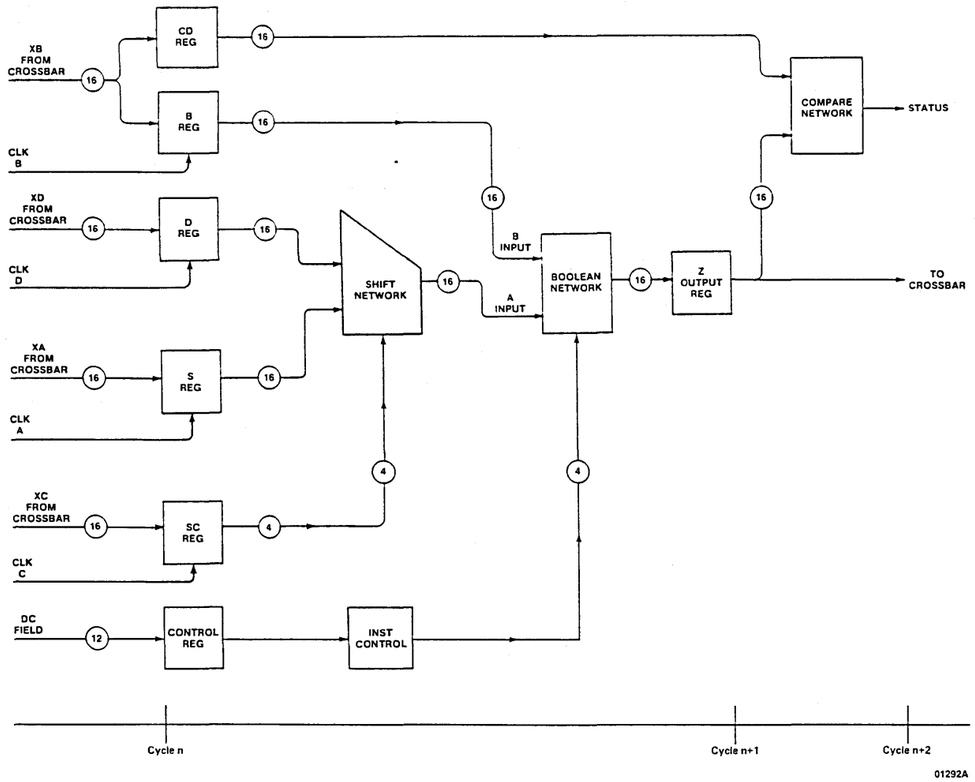


Figure IV-8-2. Shift/Boolean Unit Block Diagram

TIMING

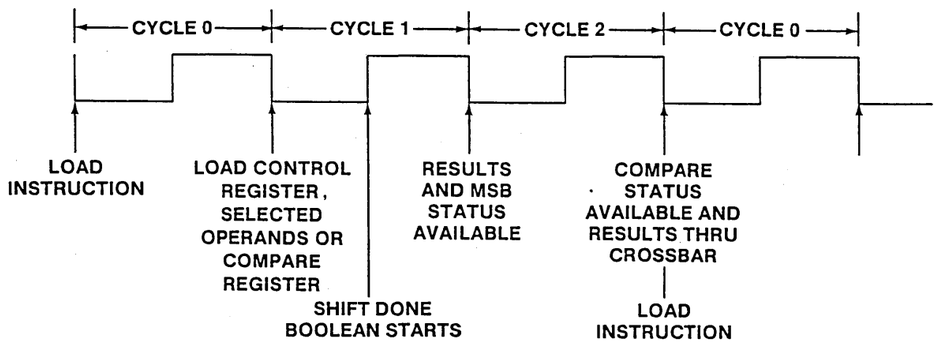


Figure IV-8-3. Shift/Boolean Instructions Timing

(C) COMPARE RGTR SBU 4.0-02

(B) BOOLEAN RGTR SBU 4.0-02

(D) DOUBLE SHIFT RGTR SBU 4.0-00

(A OR S) SHIFT OPERAND RGTR SBU 4.0-00

X BAR SHIFT COUNT RGTR SBU 4.0-03

CONTROL RGTR SBU 4.0-03

CON 2.0 DATA X BAR

CON 2.0 DATA X BAR

CON 2.0 X BAR FANOUT

CON 2.0 DC FIELDS FANOUT

CLK A

CLK B (PROG CLK D)

CLK C (PROG CLK B)

CLK D (PROG CLK C)

-SHADOW

SBU 2.1

SBU 2.1

SHIFT MATRIX SBU 4.0-00

SHIFT LATCH SHU 4.0-01

SHIFT COUNT SBU 4.0-03

-(0)

BOOLEAN FUNCTION SHU 4.0-01

MSB

OUTPUT RGTR SBU 4.0-02

SHADOW WIRED 'AND' IO SBU 4.2-00

CON 2.0

COMPARE NETWORK SBU 4.0-02

STATUS RGTR SBU 4.0-02

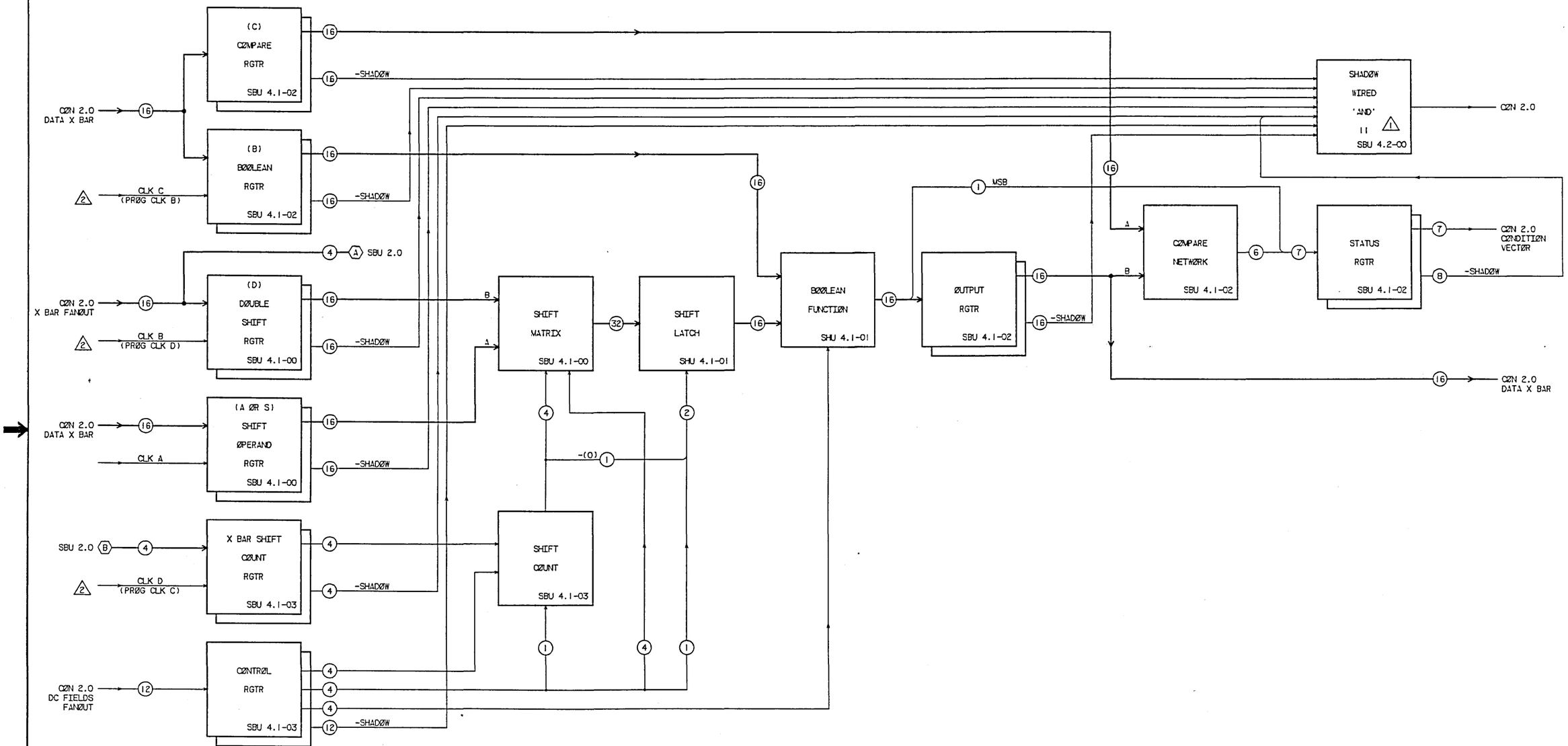
CON 2.0 CONDITION VECTOR

CON 2.0 DATA X BAR

NOTE:

1. SHADOW RGTR AND WIRED 'AND' DUPLICATED ON SHA 2.0.
2. PROGRAMMING DOCUMENTATION CLOCK LABELS.

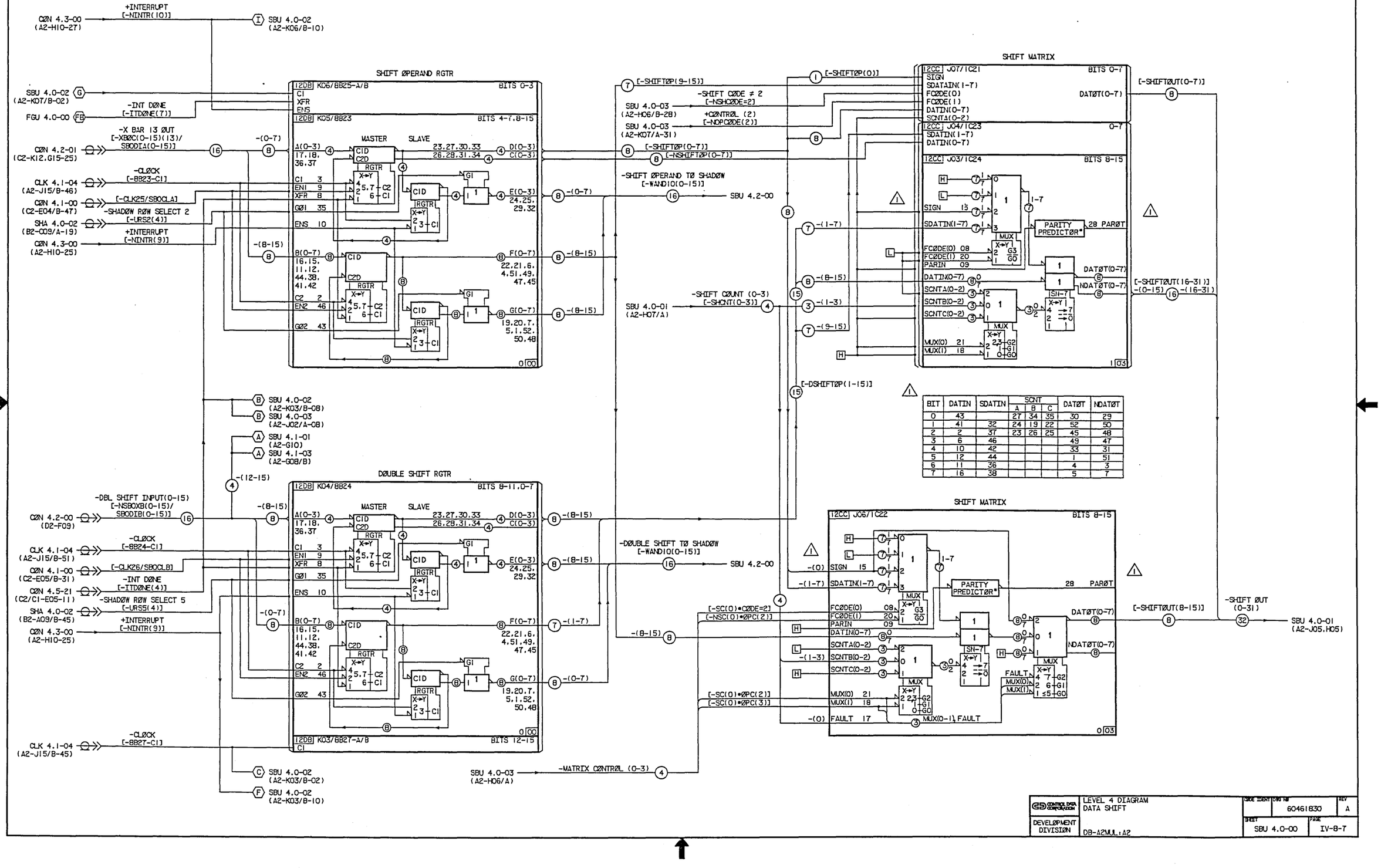
CONTROL DATA CORPORATION	LEVEL 2 DIAGRAM SHIFT BOOLEAN UNIT NO. 0	DRAWING IDENT	DWG NO 60461830 REV A
DEVELOPMENT DIVISION		SHEET SBU 2.0	SIZE IV-8-3

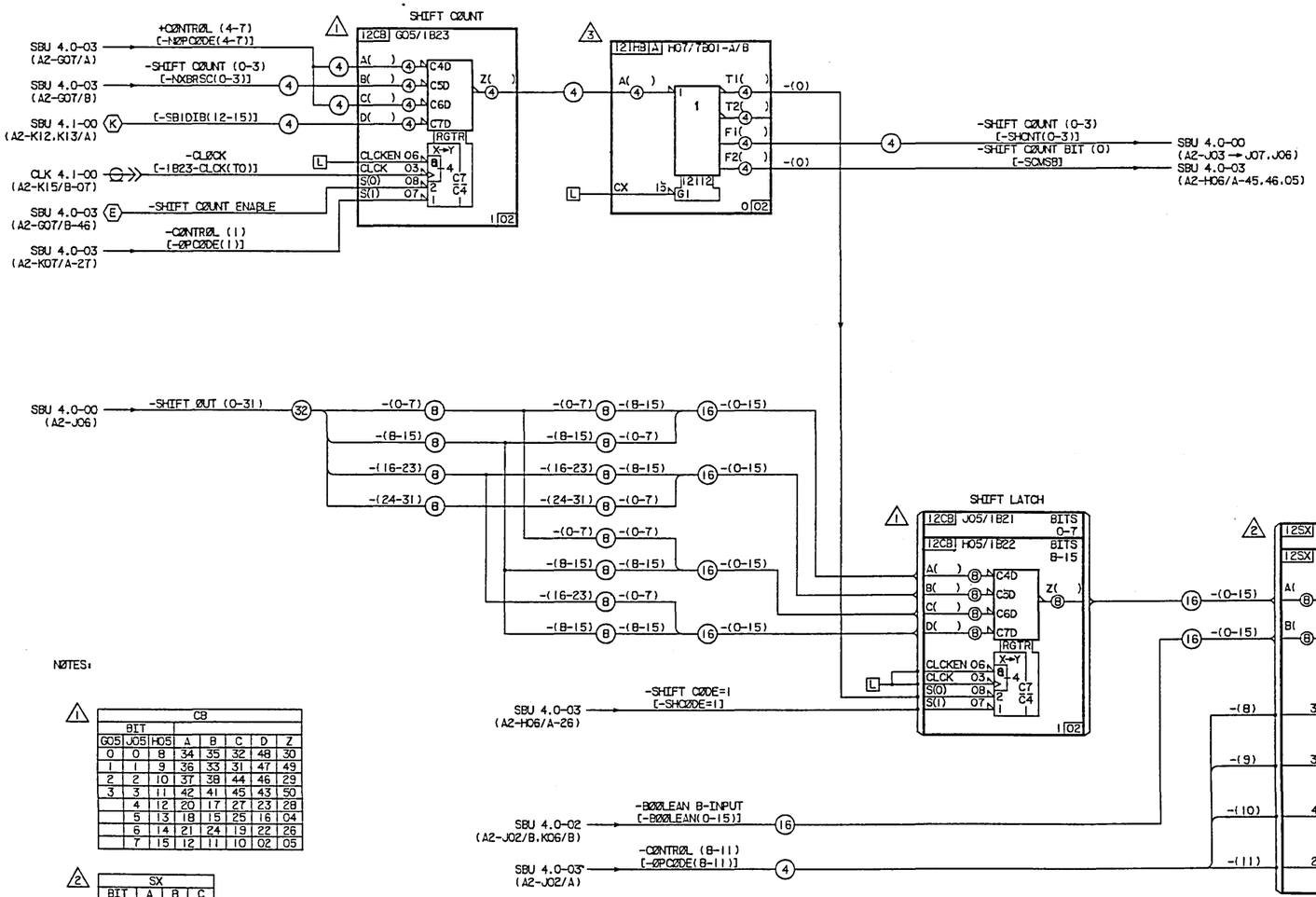


NOTE:

1. SHADOW RGTR AND WIRED 'AND' DUPLICATED ON SHA 2.0.
2. PROGRAMMING DOCUMENTATION CLOCK LABELS.

CONTROL DATA CORPORATION	LEVEL 2 DIAGRAM SHIFT BOOLEAN UNIT NO. 1	CODE IDENT	DWG NO 60461830 REV A
DEVELOPMENT DIVISION		SHEET SBU 2.1	SIZE IV-8-5


+INTERRUPT
[-NINTR(10)]
CØN 4.3-00
(A2-H10-27)
SBU 4.0-02
(A2-K06/B-10)
SHIFT ØPERAND RGTR
12DB K06/8B25-A/B
BITS 0-3
CI
XFR
ENS
12DB K05/8B23
BITS 4-7,8-15
MASTER
SLAVE
SBU 4.0-02
(A2-K07/B-02)
-INT DØNE
[-ITDØNE(7)]
FGU 4.0-00
-X BAR 13 ØUT
[-XBØC(0-15)(13)/
SBODIA(0-15)]
CØN 4.2-01
(C2-K12,G15-25)
-(0-7)
-CLØCK
[-8B23-CI]
CLK 4.1-04
(A2-J15/B-46)
[-CLK25/SBOCLA]
CØN 4.1-00
(C2-E04/B-47)
-SHADØW RØW SELECT 2
[-URS2(4)]
SHA 4.0-02
(B2-C09/A-19)
+INTERRUPT
[-NINTR(9)]
CØN 4.3-00
(A2-H10-25)
-(8-15)
-(8-15)
-(0-7)
-(8-15)
-(8-15)
-(0-7)
[-SHIFTØP(9-15)]
[-SHIFTØP(0)]
-SHIFT CØDE ≠ 2
[-NSHCØDE=2]
SBU 4.0-03
(A2-H06/B-28)
+CØNTRØL (2)
[-NOPCØDE(2)]
SBU 4.0-03
(A2-K07/A-31)
[-SHIFTØP(0-7)]
[-NSHIFTØP(0-7)]
-SHIFT ØPERAND TØ SHADØW
[-WANDIO(0-15)]
SBU 4.2-00
SBU 4.0-01
(A2-H07/A)
-SHIFT CØUNT (0-3)
[-SHCNT(0-3)]
-(1-7)
-(1-3)
-(9-15)
[-DSHIFTØP(1-15)]
SHIFT MATRIX
12CC J07/1C21
BITS 0-7
SIGN
SDATAIN(1-7)
FCØDE(0)
FCØDE(1)
DATIN(0-7)
SCNTA(0-2)
DATØT(0-7)
[-SHIFTØUT(0-7)]
12CC J04/1C23
0-7
SDATIN(1-7)
DATIN(0-7)
12CC J03/1C24
BITS 8-15
SIGN 15
SDATIN(1-7)
FCØDE(0) 08
FCØDE(1) 20
PARIN 09
DATIN(0-7)
SCNTA(0-2)
SCNTB(0-2)
SCNTC(0-2)
MUX(0) 21
MUX(1) 18
PARITY PREDICTØR*
28 PARØT
NDATØT(0-7)
[-SHIFTØUT(16-31)]
-(0-15)
-(16-31)
1 03
BIT
DATIN
SDATIN
SCNT A
SCNT B
SCNT C
DATØT
NDATØT
0 43 27 34 35 30 29
1 41 32 24 19 22 52 50
2 2 37 23 26 25 45 48
3 6 46 49 47
4 10 42 33 31
5 12 44 1 51
6 11 36 4 3
7 16 38 5 7
DØUBLE SHIFT RGTR
12DB K04/8B24
BITS 8-11,0-7
-(12-15)
-DBL SHIFT INPUT(0-15)
[-NSBOXB(0-15)/
SBODIB(0-15)]
CØN 4.2-00
(D2-F09)
-CLØCK
[-8B24-CI]
CLK 4.1-04
(A2-J15/B-51)
[-CLK26/SBOCLB]
CØN 4.1-00
(C2-E05/B-31)
-INT DØNE
[-ITDØNE(4)]
CØN 4.5-21
(C2/C1-E05-11)
-SHADØW RØW SELECT 5
[-URS5(4)]
SHA 4.0-02
(B2-A09/B-45)
+INTERRUPT
[-NINTR(9)]
CØN 4.3-00
(A2-H10-25)
-(0-7)
-(8-15)
-(1-7)
-(0-7)
-DØUBLE SHIFT TØ SHADØW
[-WANDIO(0-15)]
SBU 4.2-00
[-SC(0)•CØDE=2]
[-NSC(0)•ØPC(2)]
[-SC(0)•ØPC(2)]
[-SC(0)•ØPC(3)]
SHIFT MATRIX
12CC J06/1C22
BITS 8-15
SIGN 15
SDATIN(1-7)
FCØDE(0) 08
FCØDE(1) 20
PARIN 09
DATIN(0-7)
SCNTA(0-2)
SCNTB(0-2)
SCNTC(0-2)
MUX(0) 21
MUX(1) 18
FAULT 17
PARITY PREDICTØR*
28 PARØT
NDATØT(0-7)
FAULT
MUX(0)
MUX(1)
MUX(0-1) FAULT
0 03
[-SHIFTØUT(8-15)]
-SHIFT ØUT
(0-31)
SBU 4.0-01
(A2-J05.H05)
SBU 4.0-02
(A2-K03/B-08)
SBU 4.0-03
(A2-J02/A-08)
SBU 4.1-01
(A2-G10)
SBU 4.1-03
(A2-G08/B)
-CLØCK
[-8B27-CI]
CLK 4.1-04
(A2-J15/B-45)
12DB K03/8B27-A/B
BITS 12-15
SBU 4.0-02
(A2-K03/B-02)
SBU 4.0-02
(A2-K03/B-10)
SBU 4.0-03
(A2-H06/A)
-MATRIX CØNTRØL (0-3)
CONTROL DATA CORPORATION
DEVELØPMENT DIVISIØN
LEVEL 4 DIAGRAM
DATA SHIFT
DB-A2MUL,A2
60461830
A
SBU 4.0-00
IV-8-7



NOTES:

1.

C8							
BIT							
G05	J05	H05	A	B	C	D	Z
0	0	8	34	35	32	48	30
1	1	9	36	33	31	47	49
2	2	10	37	38	44	46	29
3	3	11	42	41	45	43	50
	4	12	20	17	27	23	28
	5	13	18	15	25	16	04
	6	14	21	24	19	22	26
	7	15	12	11	10	02	05

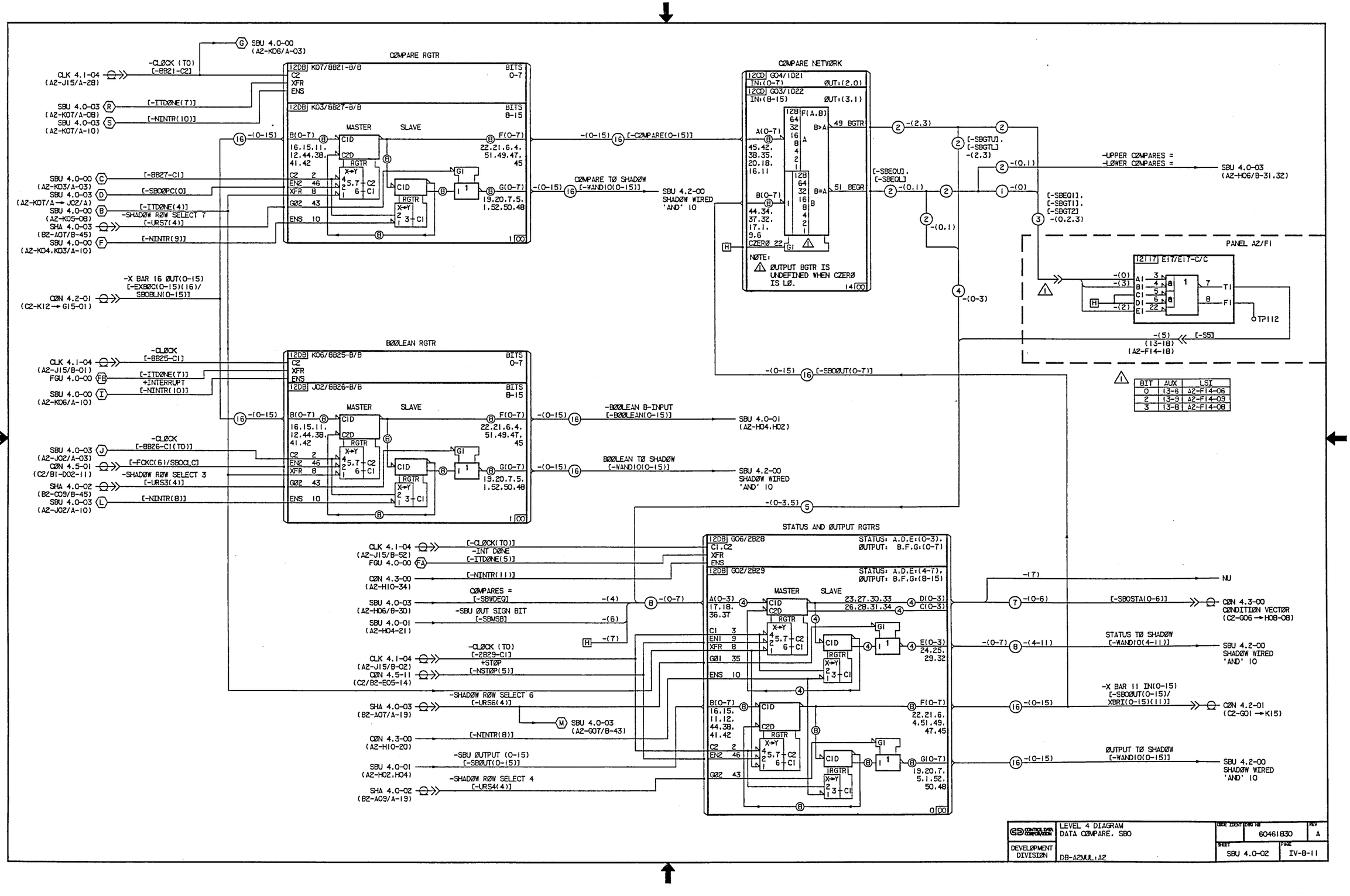
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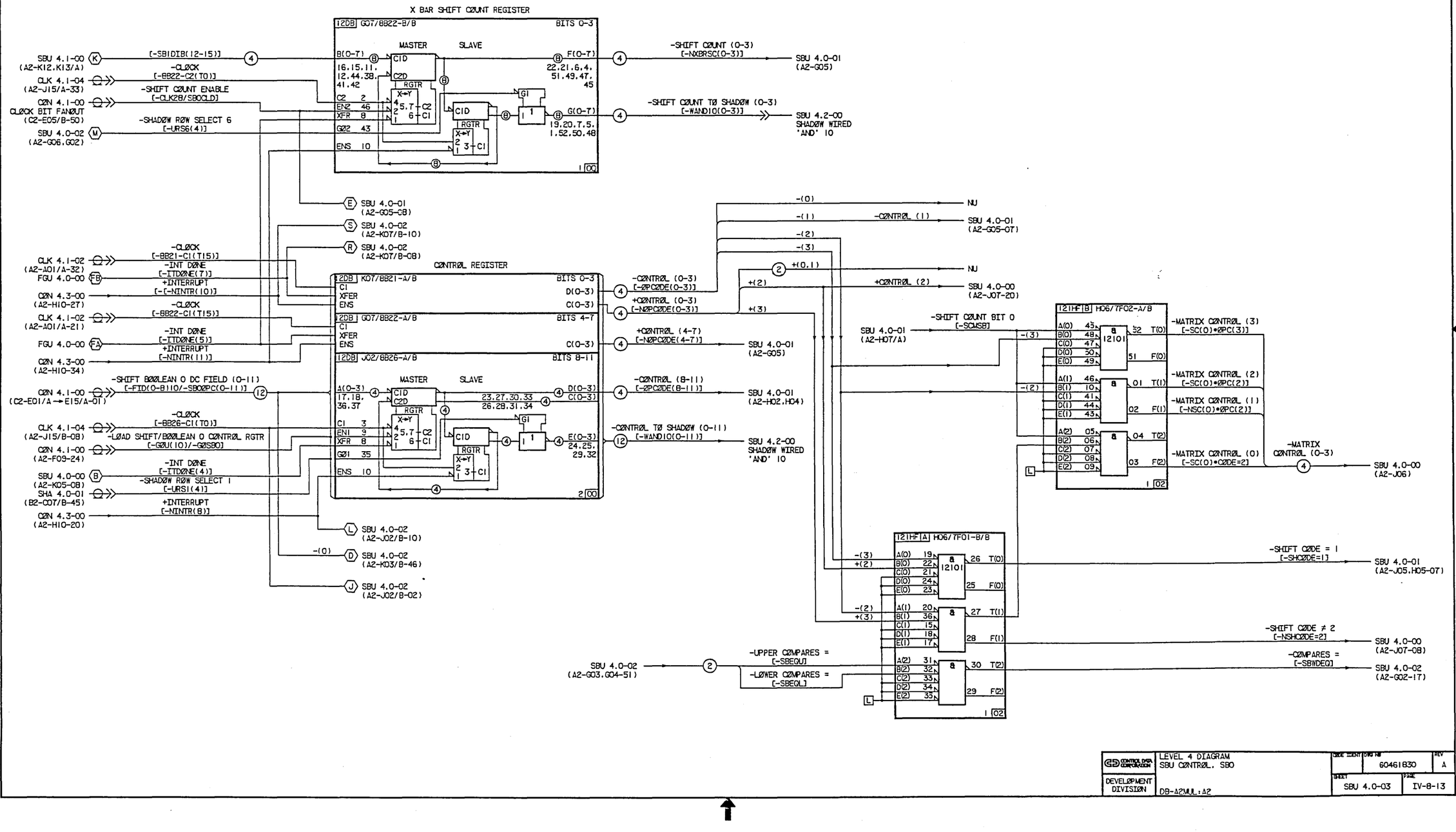
SX			
BIT	A	B	C
0,8	19	22	21
1,9	17	20	24
2,10	31	30	28
3,11	34	33	29
4,12	07	06	05
5,13	03	08	04
6,14	50	47	52
7,15	46	45	49

3.

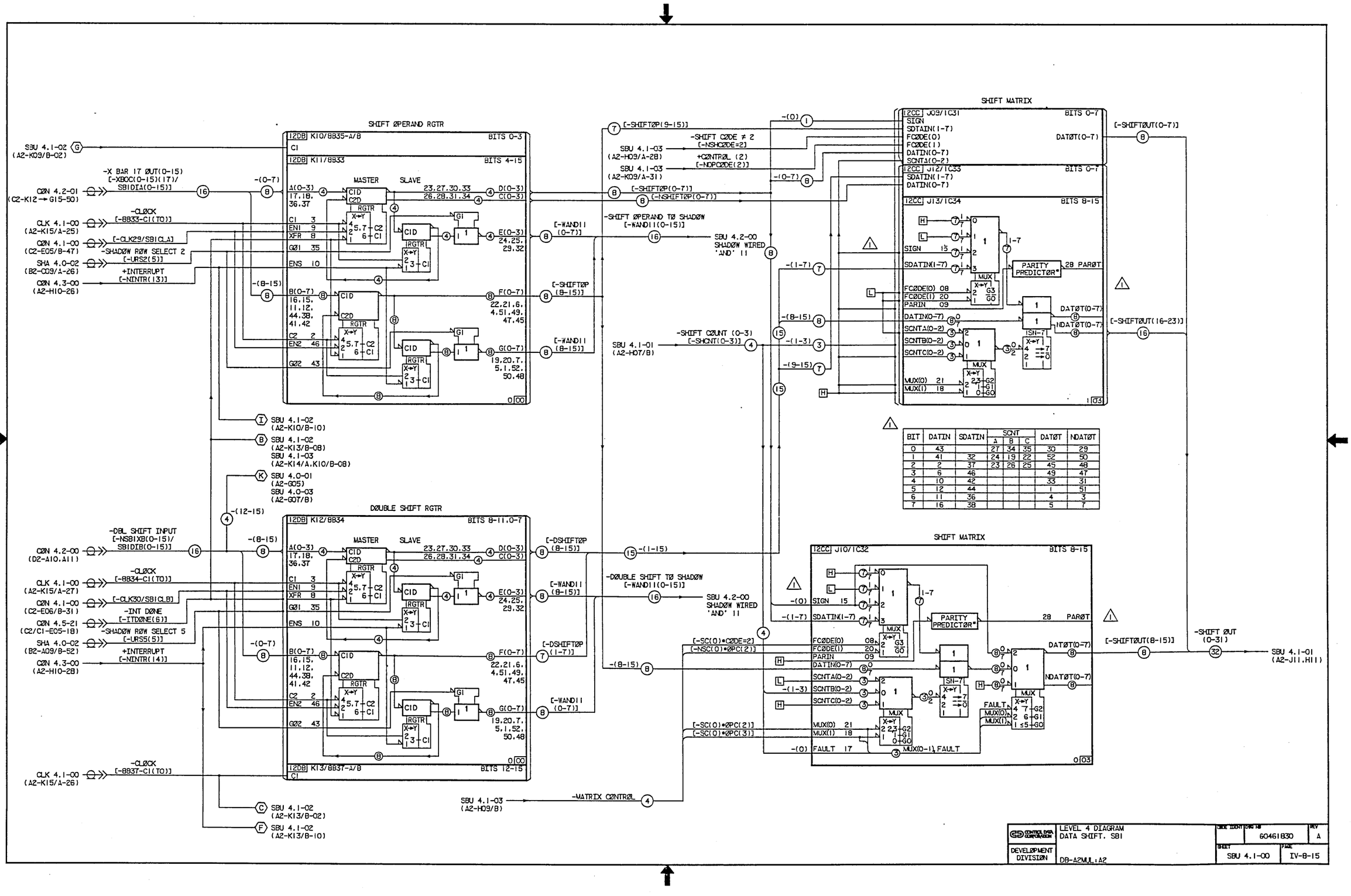
HB					
BIT	A	T1	T2	F1	F2
0	17	20	19	22	21
1	18	25	26	23	24
2	36	27	28	29	30
3	35	34	33	32	31

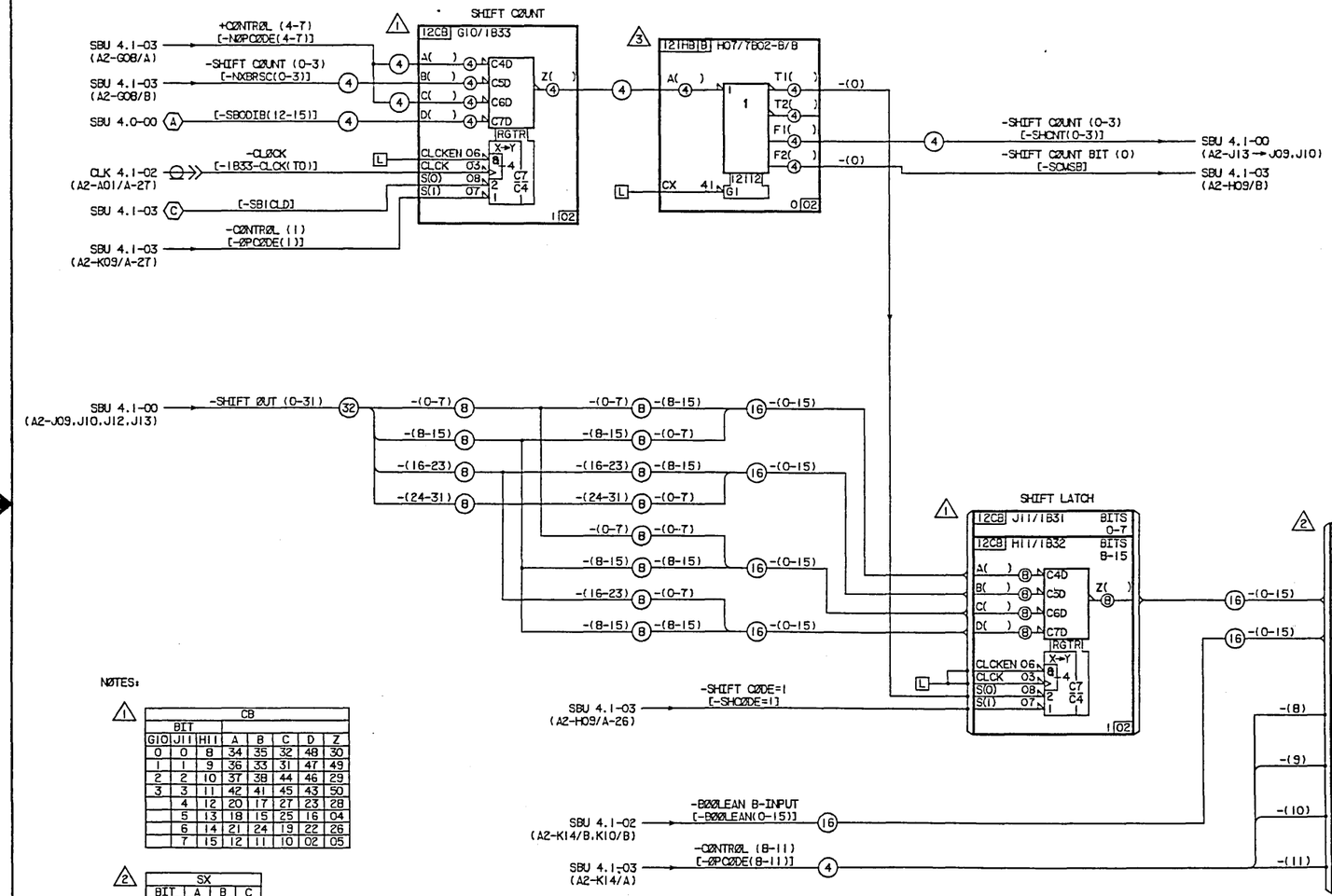
CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM BOOLEAN FUNCTIONS	DRAWING IDENT / DRAWING NO.	60461830 REV A
DEVELOPMENT DIVISION	DB-A2MUL:A2	SHEET SBU 4.0-01	PAGE IV-8-9


COMPARE RGTR
BOOLEAN RGTR
COMPARE NETWORK
STATUS AND OUTPUT RGTRS
MASTER
SLAVE
CLK 4.1-04 (A2-J15/A-28)
-CLOCK (TO) [-BB21-C2]
SBU 4.0-00 (A2-K06/A-03)
SBU 4.0-03 (A2-K07/A-08)
SBU 4.0-03 (A2-K07/A-10)
[-ITDONE(7)]
[-NINTR(10)]
SBU 4.0-00 (A2-K03/A-03)
SBU 4.0-03 (A2-K07/A→J02/A)
SBU 4.0-00 (A2-K05-08)
SHA 4.0-03 (B2-A07/B-45)
SBU 4.0-00 (A2-K04,K03/A-10)
[-BB27-CI]
[-SBOOPC(0)]
[-ITDONE(4)]
-SHADOW ROW SELECT 7
[-URS7(4)]
[-NINTR(9)]
-X BAR 16 OUT(0-15) [-EXBOC(0-15)(16)/ SBOBLN(0-15)]
C2N 4.2-01 (C2-K12→G15-01)
CLK 4.1-04 (A2-J15/B-01)
FGU 4.0-00
SBU 4.0-00 (A2-K06/A-10)
-CLOCK [-BB25-CI]
[-ITDONE(7)]
+INTERRUPT
[-NINTR(10)]
SBU 4.0-03 (A2-J02/A-03)
C2N 4.5-01 (C2/B1-D02-11)
SHA 4.0-02 (B2-C09/B-45)
SBU 4.0-03 (A2-J02/A-10)
-CLOCK [-BB26-CI(TO)]
[-FCKC(6)/SBOCLC]
-SHADOW ROW SELECT 3
[-URS3(4)]
[-NINTR(8)]
-(0-15) [-COMPARE(0-15)]
COMPARE TO SHADOW [-WANDIO(0-15)]
SBU 4.2-00 SHADOW WIRED 'AND' IO
-BOOLEAN B-INPUT [-BOOLEAN(0-15)]
SBU 4.0-01 (A2-H04,H02)
BOOLEAN TO SHADOW [-WANDIO(0-15)]
-(0-15) [-SBOOUT(0-7)]
-(0-3.5)
-(2.3)
[-SBEQU], [-SBEQL]
[-SBGTU], [-SBGTL] -(2.3)
-(0.1)
-(0)
-(0-3)
-UPPER COMPARES =
-LOWER COMPARES =
SBU 4.0-03 (A2-H06/B-31,32)
[-SBEQI], [-SBGTI], [-SBGTZ] -(0.2.3)
PANEL A2/F1
12117 E17/E17-C/C
TP112
-(5) [-S5]
(13-18) (A2-F14-18)
BIT | AUX | LSI
0 | 13-6 | A2-F14-06
2 | 13-9 | A2-F14-09
3 | 13-8 | A2-F14-08
CLK 4.1-04 (A2-J15/B-02)
C2N 4.5-11 (C2/B2-E05-14)
FGU 4.0-00
-INT DONE [-ITDONE(5)]
C2N 4.3-00 (A2-H10-34)
COMPARES = [-SBWDEQ]
SBU 4.0-03 (A2-H06/B-30)
-SBU OUT SIGN BIT [-SBMSB]
SBU 4.0-01 (A2-H04-21)
-CLOCK (TO) [-2B29-CI]
+STOP [-NSTOP(5)]
-SHADOW ROW SELECT 6 [-URS6(4)]
SHA 4.0-03 (B2-A07/A-19)
SBU 4.0-03 (A2-G07/B-43)
-SBU OUTPUT (0-15) [-SBOUT(0-15)]
-SHADOW ROW SELECT 4 [-URS4(4)]
SHA 4.0-02 (B2-A09/A-19)
-(7) NU
-(6) [-SBOSTA(0-6)] C2N 4.3-00 CONDITION VECTOR (C2-G06→H08-08)
-(4-11) STATUS TO SHADOW [-WANDIO(4-11)] SBU 4.2-00 SHADOW WIRED 'AND' IO
-X BAR 11 IN(0-15) [-SBOOUT(0-15)/ XBRI(0-15)(11)] C2N 4.2-01 (C2-G01→K15)
OUTPUT TO SHADOW [-WANDIO(0-15)] SBU 4.2-00 SHADOW WIRED 'AND' IO
NOTE: ⚠ OUTPUT BGTR IS UNDEFINED WHEN CZERO IS LO.
LEVEL 4 DIAGRAM
DATA COMPARE, SBO
DEVELOPMENT DIVISION
DB-A2MUL:A2
60461830
REV A
SHEET SBU 4.0-02
PAGE IV-B-11



CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM SBU CØNTRØL, SBO	CODE IDENT	DWG NO 60461830 REV A
DEVELOPMENT DIVISION	DB-A2MUL:A2	SHEET SBU 4.0-03	PAGE IV-8-13


SHIFT ØPERAND RGTR
SHIFT MATRIX
DØUBLE SHIFT RGTR
SHIFT MATRIX
SBU 4.1-02 (A2-K09/B-02)
-X BAR 17 ØUT(0-15) [-XBOC(0-15)(17)/ SBIDIA(0-15)]
CØN 4.2-01 (C2-K12→G15-50)
-CLØCK [-BB33-CI(TO)]
CLK 4.1-00 (A2-K15/A-25)
CØN 4.1-00 (C2-E05/B-47)
-SHADØW RØW SELECT 2 [-URS2(5)]
SHA 4.0-02 (B2-C09/A-26)
+INTERRUPT [-NINTR(13)]
CØN 4.3-00 (A2-H10-26)
12DB K10/BB35-A/B
BITS 0-3
CI
12DB K11/BB33
BITS 4-15
MASTER
SLAVE
A(0-3) 17,18, 36,37
CI 3
EN1 9
XFR 8
GØ1 35
EN3 10
B(0-7) 16,15, 11,12, 44,38, 41,42
C2 2
EN2 46
GØ2 43
23,27,30,33
26,28,31,34
D(0-3)
C(0-3)
E(0-3) 24,25, 29,32
F(0-7) 22,21,6, 4,51,49, 47,45
G(0-7) 19,20,7, 5,1,52, 50,48
0 00
[-WANDII (0-7)]
[-SHIFTØP (8-15)]
[-WANDII (8-15)]
-SHIFT ØPERAND TØ SHADØW [-WANDII(0-15)]
SBU 4.2-00 SHADØW WIRED 'AND' 11
[-SHIFTØP(9-15)]
-SHIFT CØDE ≠ 2 [-NSHCØDE=2]
SBU 4.1-03 (A2-H09/A-28)
+CØNTRØL (2) [-NOPCØDE(2)]
SBU 4.1-03 (A2-K09/A-31)
[-SHIFTØP(0-7)]
[-NSHIFTØP(0-7)]
SBU 4.1-01 (A2-H07/B)
-SHIFT CØUNT (0-3) [-SHCNT(0-3)]
12CC J09/1C31
BITS 0-7
SIGN
SDTAIN(1-7)
FCØDE(0)
FCØDE(1)
DATIN(0-7)
SCNTA(0-2)
DATØT(0-7)
12CC J12/1C33
BITS 0-7
SDTAIN(1-7)
DATIN(0-7)
12CC J13/1C34
BITS 8-15
SIGN 15
SDATIN(1-7)
FCØDE(0) 08
FCØDE(1) 20
PARIN 09
DATIN(0-7)
SCNTA(0-2)
SCNTB(0-2)
SCNTC(0-2)
MUX(0) 21
MUX(1) 18
PARITY PREDICTØR*
28 PARØT
MUX
SH-7
NDATØT(0-7)
[-SHIFTØUT(0-7)]
[-SHIFTØUT(16-23)]
1 03
BIT | DATIN | SDATIN | SCNT A | SCNT B | SCNT C | DATØT | NDATØT
0 | 43 | | 27 | 34 | 35 | 30 | 29
1 | 41 | 32 | 24 | 19 | 22 | 52 | 50
2 | 2 | 37 | 23 | 26 | 25 | 45 | 48
3 | 6 | 46 | | | | 49 | 47
4 | 10 | 42 | | | | 33 | 31
5 | 12 | 44 | | | | 1 | 51
6 | 11 | 36 | | | | 4 | 3
7 | 16 | 38 | | | | 5 | 7
-DBL SHIFT INPUT [-NSBIXB(0-15)/ SBIDIB(0-15)]
CØN 4.2-00 (D2-A10,A11)
-CLØCK [-BB34-CI(TO)]
CLK 4.1-00 (A2-K15/A-27)
CØN 4.1-00 (C2-E06/B-31)
-INT DØNE [-ITDØNE(6)]
CØN 4.5-21 (C2/C1-E05-18)
-SHADØW RØW SELECT 5 [-URS5(5)]
SHA 4.0-02 (B2-A09/B-52)
+INTERRUPT [-NINTR(14)]
CØN 4.3-00 (A2-H10-28)
-CLØCK [-BB37-CI(TO)]
CLK 4.1-00 (A2-K15/A-26)
12DB K12/BB34
BITS 8-11,0-7
12DB K13/BB37-A/B
BITS 12-15
[-DSHIFTØP (8-15)]
[-DSHIFTØP (0-7)]
-DØUBLE SHIFT TØ SHADØW [-WANDII(0-15)]
SBU 4.2-00 SHADØW WIRED 'AND' 11
[-SC(0)•CØDE=2]
[-NSC(0)•ØPC(2)]
[-SC(0)•ØPC(2)]
[-SC(0)•ØPC(3)]
-MATRIX CØNTRØL
SBU 4.1-03 (A2-H09/B)
12CC J10/1C32
BITS 8-15
SIGN 15
SDATIN(1-7)
FCØDE(0) 08
FCØDE(1) 20
PARIN 09
DATIN(0-7)
SCNTA(0-2)
SCNTB(0-2)
SCNTC(0-2)
MUX(0) 21
MUX(1) 18
FAULT 17
MUX(0-1) FAULT
PARITY PREDICTØR*
28 PARØT
DATØT(0-7)
NDATØT(0-7)
FAULT
[-SHIFTØUT(8-15)]
-SHIFT ØUT (0-31)
SBU 4.1-01 (A2-J11,H11)
0 03
SBU 4.1-02 (A2-K10/B-10)
SBU 4.1-02 (A2-K13/B-08)
SBU 4.1-03 (A2-K14/A,K10/B-08)
SBU 4.0-01 (A2-G05)
SBU 4.0-03 (A2-G07/B)
SBU 4.1-02 (A2-K13/B-02)
SBU 4.1-02 (A2-K13/B-10)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
DATA SHIFT. SB1
DB-A2MUL:A2
CODE IDENT 60461830
REV A
SHEET SBU 4.1-00
PAGE IV-B-15



NOTES:

1

BIT			CB				
G10	J11	H11	A	B	C	D	Z
0	0	8	34	35	32	48	30
1	1	9	36	33	31	47	49
2	2	10	37	38	44	46	29
3	3	11	42	41	45	43	50
	4	12	20	17	27	23	28
	5	13	18	15	25	16	04
	6	14	21	24	19	22	26
	7	15	12	11	10	02	05

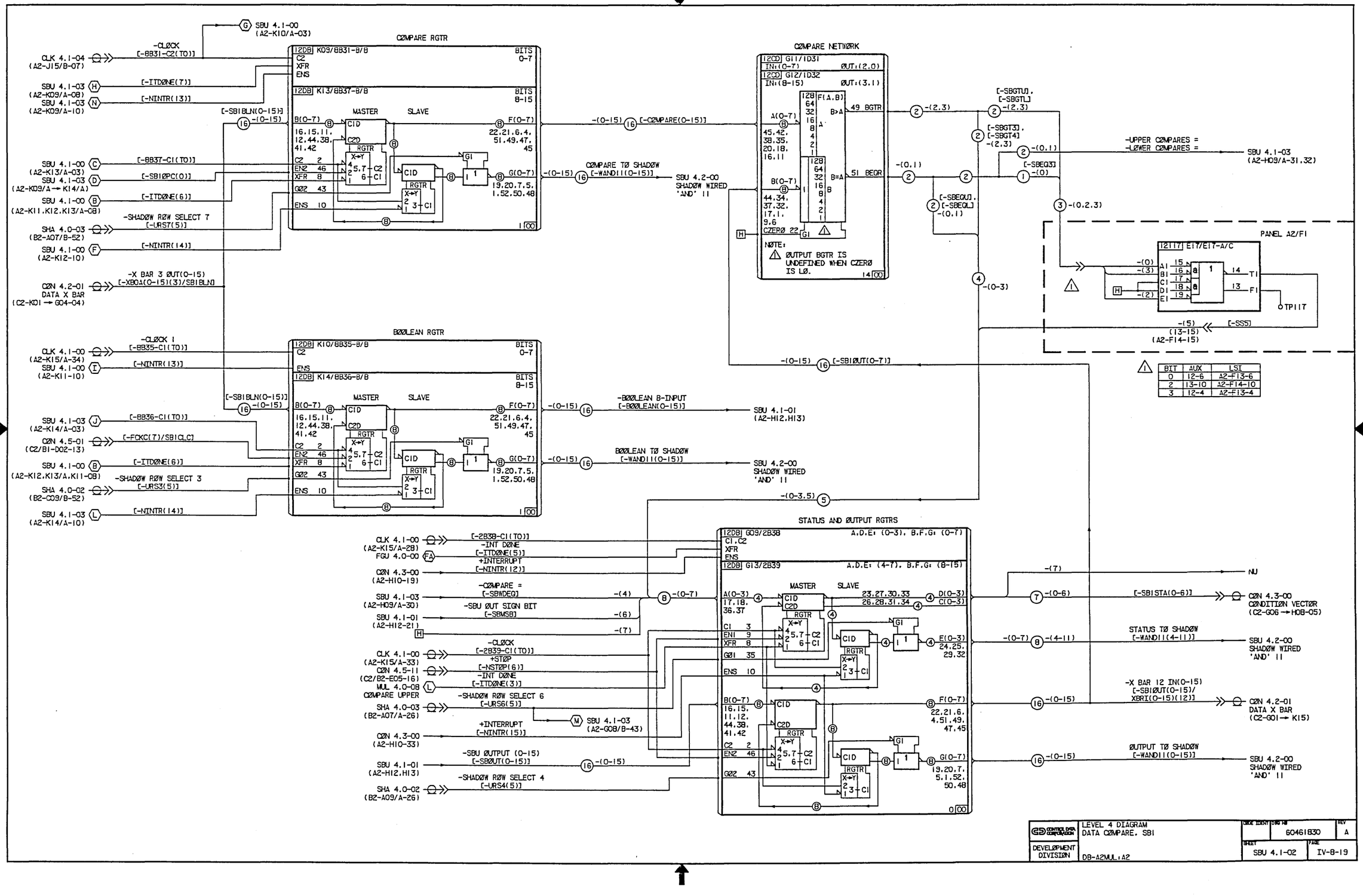
2

SX			
BIT	A	B	C
0.8	19	22	21
1.9	17	20	24
2.10	31	30	28
3.11	34	33	29
4.12	07	06	05
5.13	03	08	04
6.14	50	47	52
7.15	46	45	49

3

HB					
BIT	A	T1	T2	F1	F2
0	43	46	45	48	47
1	44	51	52	49	50
2	10	01	02	03	04
3	09	08	07	06	05

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM BOOLEAN FUNCTIONS, SBI	CODE IDENT	DWG NO 60461830 REV A
DEVELOPMENT DIVISION	DB-A2MUL:A2	SHEET SBU 4.1-01	PAGE IV-B-17


COMPARE RGTR
BØØLEAN RGTR
COMPARE NETWØRK
STATUS AND ØUTPUT RGTRS
PANEL A2/F1
-CLØCK
[-BB31-C2(TO)]
CLK 4.1-04
(A2-J15/B-07)
SBU 4.1-03
(A2-K09/A-08)
SBU 4.1-03
(A2-K09/A-10)
[-ITDØNE(7)]
[-NINTR(13)]
[-SBIBLN(0-15)]
SBU 4.1-00
(A2-K10/A-03)
[-BB37-C1(TO)]
[-SBI0PC(0)]
[-ITDØNE(6)]
-SHADØW RØW SELECT 7
[-URS7(5)]
SHA 4.0-03
(B2-A07/B-52)
SBU 4.1-00
(A2-K12-10)
[-NINTR(14)]
-X BAR 3 ØUT(0-15)
[-XB0A(0-15)(3)/SBIBLN]
C2N 4.2-01
DATA X BAR
(C2-K01 → G04-04)
-CLØCK 1
[-BB35-C1(TO)]
CLK 4.1-00
(A2-K15/A-34)
SBU 4.1-00
(A2-K11-10)
[-NINTR(13)]
[-SBIBLN(0-15)]
[-BB36-C1(TO)]
SBU 4.1-03
(A2-K14/A-03)
C2N 4.5-01
(C2/B1-D02-13)
[-FCKC(7)/SBICLC]
SBU 4.1-00
(A2-K12,K13/A,K11-08)
[-ITDØNE(6)]
-SHADØW RØW SELECT 3
[-URS3(5)]
SHA 4.0-02
(B2-C09/B-52)
SBU 4.1-03
(A2-K14/A-10)
[-NINTR(14)]
[-C0MPARE(0-15)]
C0MPARE TØ SHADØW
[-WAND11(0-15)]
SBU 4.2-00
SHADØW WIRED
'AND' 11
[-SBGTU],
[-SBGTL]
[-SBGT3],
[-SBGT4]
-UPPER C0MPARES =
-LØWER C0MPARES =
SBU 4.1-03
(A2-H09/A-31,32)
[-SBEQ3]
[-SBEQU],
[-SBEQL]
-(0-3)
-(0,2,3)
[-SS5]
(13-15)
(A2-F14-15)
-(0-3.5)
-(7)
NU
[-SBISTA(0-6)]
C2N 4.3-00
CØNDITIØN VECTØR
(C2-G06 → H08-05)
STATUS TØ SHADØW
[-WAND11(4-11)]
SBU 4.2-00
SHADØW WIRED
'AND' 11
-X BAR 12 IN(0-15)
[-SBIØUT(0-15)/
XBRI(0-15)(12)]
C2N 4.2-01
DATA X BAR
(C2-G01 → K15)
ØUTPUT TØ SHADØW
[-WAND11(0-15)]
SBU 4.2-00
SHADØW WIRED
'AND' 11
-BØØLEAN B-INPUT
[-BØØLEAN(0-15)]
SBU 4.1-01
(A2-H12,H13)
BØØLEAN TØ SHADØW
[-WAND11(0-15)]
SBU 4.2-00
SHADØW WIRED
'AND' 11
[-SBIØUT(0-7)]
-CLØCK
[-2B38-C1(TO)]
CLK 4.1-00
(A2-K15/A-28)
-INT DØNE
[-ITDØNE(5)]
FGU 4.0-00
+INTERRUPT
[-NINTR(12)]
C2N 4.3-00
(A2-H10-19)
-C0MPARE =
[-SBWDEQ]
SBU 4.1-03
(A2-H09/A-30)
-SBU ØUT SIGN BIT
[-SBMSB]
SBU 4.1-01
(A2-H12-21)
-CLØCK
[-2B39-C1(TO)]
CLK 4.1-00
(A2-K15/A-33)
+STØP
[-NSTØP(6)]
C2N 4.5-11
(C2/B2-E05-16)
-INT DØNE
[-ITDØNE(3)]
MUL 4.0-08
C0MPARE UPPER
-SHADØW RØW SELECT 6
[-URS6(5)]
SHA 4.0-03
(B2-A07/A-26)
SBU 4.1-03
(A2-G08/B-43)
+INTERRUPT
[-NINTR(15)]
C2N 4.3-00
(A2-H10-33)
-SBU ØUTPUT (0-15)
[-SBØUT(0-15)]
SBU 4.1-01
(A2-H12,H13)
-SHADØW RØW SELECT 4
[-URS4(5)]
SHA 4.0-02
(B2-A09/A-26)
NØTE:
⚠ ØUTPUT BGTR IS UNDEFINED WHEN CZERØ IS LØ.
BIT | AUX | LSI
0 | 12-6 | A2-F13-6
2 | 13-10 | A2-F14-10
3 | 12-4 | A2-F13-4
LEVEL 4 DIAGRAM
DATA C0MPARE, SBI
DEVELØPMENT DIVISIØN
DB-A2MUL:A2
60461830
A
SBU 4.1-02
IV-8-19

X BAR SHIFT CØUNT REGISTER

12DB GØ8/8832-B/B — BITS 0-3

SBU 4.0-00 (A2-K04,K03/A) — +SHIFT CØUNT [-SBCDIB(12-15)] — -(0-3)

CLK 4.1-00 (A2-K15/A-20) — -CLØCK [-8832-C2(T0)]

CØN 4.1-00 CLØCK BITS FANØUT (C2-E06/B-50) — -SHIFT CØUNT ENABLE [-CLK32/-SB1CLD]

SBU 4.1-02 (A2-G09,G13-35) — -SHADØW RØW SELECT 6 [-URS6(5)]

MASTER / SLAVE

B(0-7) 16,15,11,12,44,38,41,42 — CID, C2D, RGTR, X→Y, 4,5,7→C2, 2,6→CI

C2 2 · EN2 46 · XFR 8 · GØ2 43 · ENS 10

GI — 1 1

F(0-7) 22,21,6,4,51,49,47,45 — -SHIFT CØUNT (0-3) [-NXBRSC(0-3)] — SBU 4.1-01 (A2-G10)

G(0-7) 19,20,7,5,1,52,50,48 — -SHIFT CØUNT TØ SHADØW [-WAND11(0-3)] — SBU 4.2-00 SHADØW WIRED 'AND' 11

1 00

SBU 4.1-01 (A2-G10-08)

SBU 4.1-02 (A2-K09/B-10)

SBU 4.1-02 (A2-K09/B-08)

CØNTRØL REGISTER

CLK 4.1-02 (A2-A01/A-24) — -CLØCK [-8831-C1(T15)]

FGU 4.0-00 — -INT DØNE [-ITDØNE(7)]

CØN 4.3-00 (A2-H10-26) — +INTERRUPT [-NINTR(13)]

CLK 4.1-02 (A2-A01/A-30) — -CLØCK [-8832-C1(T15)]

FGU 4.0-00 — [-ITDØNE(5)]

CØN 4.3-00 (A2-H10-34) — +INTERRUPT [-NINTR(11)]

12DB K09/8831-A/B — BITS 0-3

CI · XFR · ENS

D(0-3) — -CØNTRØL (0-3) [-ØPCØDE(0-3)]

C(0-3) — +CØNTRØL (0-3) [-NØPCØDE(0-3)]

12DB GØ8/8832-A/B — BITS 4-7

CI · XFR · ENS

C(0-3) — +CØNTRØL (4-7) [-NØPCØDE(4-7)] — SBU 4.1-01 (A2-G10)

12DB K14/8836-A/B — BITS 8-11

MASTER / SLAVE

A(0-3) 17,18,36,37 — CID, C2D, RGTR, X→Y, 4,5,7→C2, 2,6→CI

CI 3 · ENI 9 · XFR 8 · GØI 35 · ENS 10

23,27,30,33 26,28,31,34 — GI — 1 1

D(0-3) — C(0-3)

E(0-3) 24,25,29,32 — -CØNTRØL TØ SHADØW [-WAND11(0-11)] — SBU 4.2-00 SHADØW WIRED 'AND' 11

2 00

-CØNTRØL (8-11) [-ØPCØDE(8-11)] — SBU 4.1-01 (A2-H12,H13)

-SHIFT/BØØLEAN 1 DC FIELD (0-11) [-FID(0-8)11/-SB1ØPC(0-11)] — CØN 4.1-00 (C2-E01/A→E15/A-02)

-CLØCK [-8836-C1(T0)] — CLK 4.1-00 (A2-K15/A-19)

-LØAD SHIFT/BØØLEAN 1 CØNTRØL RGTR [-GØU(11)/-GØSB1] — CØN 4.1-00 (C2-F09-02)

[-ITDØNE(6)] — SBU 4.1-00 (A2-K11,K12,K13/B-08)

-SHADØW RØW SELECT 1 [-URS1(5)] — SHA 4.0-01 (B2-C07/B-52)

+INTERRUPT [-NINTR(14)] — CØN 4.3-00 (A2-H10-28)

SBU 4.1-02 (A2-K14/B-10)

SBU 4.1-02 (A2-K14/B-02)

-(0) — SBU 4.1-02 (A2-K09/B,K13/B-46)

-(0) — NU

-(1) — -CØNTRØL (1) — SBU 4.1-01 (A2-G10-07)

-(2)

-(3)

+(0.1) — NU

+(2) — +CØNTRØL (2) — SBU 4.1-00 (A2-J09-20)

+(3)

-SHIFT CØUNT BIT 0 [-SCMSB] — SBU 4.1-01 (A2-H07/B)

12IHF B H09/7F04-B/B

-(3) · -(2)

A(0) 45, B(0) 48, C(0) 47, D(0) 50, E(0) 49 — 12101 — 52 T(0), 51 F(0)

A(1) 46, B(1) 10, C(1) 41, D(1) 44, E(1) 43 — 12101 — 01 T(1), 02 F(1)

A(2) 05, B(2) 06, C(2) 07, D(2) 08, E(2) 09 — 12101 — 04 T(2), 03 F(2)

L

1 02

-MATRIX CØNTRØL (3) [-SC(0)•ØPC(3)]

-MATRIX CØNTRØL (2) [-SC(0)•ØPC(2)]

-MATRIX CØNTRØL (1) [-NSC(0)•ØPC(2)]

-MATRIX CØNTRØL (0) [-SC(0)•CØDE=2]

-MATRIX CØNTRØL (0-3) — SBU 4.1-00 (A2-J10)

12IHF A H09/7F03-A/B

-(3) · +(2)

A(0) 19, B(0) 22, C(0) 21, D(0) 24, E(0) 23 — 12101 — 26 T(0), 25 F(0)

-SHIFT CØDE = 1 [-SHCØDE=1] — SBU 4.1-01 (A2-J11,H11-07)

-(2) · +(3)

A(1) 20, B(1) 36, C(1) 15, D(1) 18, E(1) 17 — 12101 — 27 T(1), 28 F(1)

-SHIFT CØDE ≠ 2 [-NSHCØDE=2] — SBU 4.1-00 (A2-J09-08)

SBU 4.1-02 (A2-G11,G12-51) — -UPPER CØMPARES = [-SBEQU] · -LØWER CØMPARES = [-SBEQL]

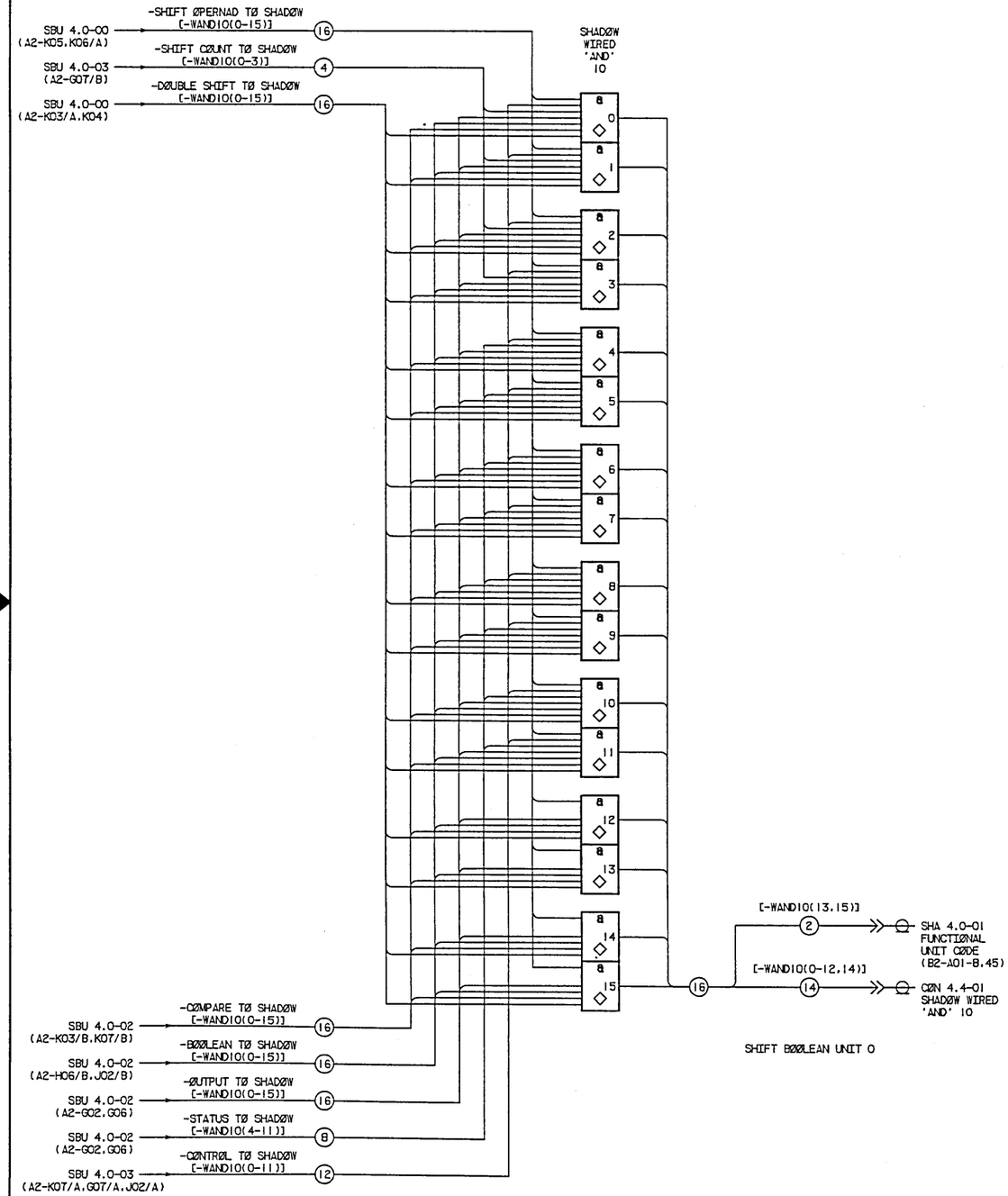
A(2) 31, B(2) 32, C(2) 33, D(2) 34, E(2) 35 — 12101 — 30 T(2), 29 F(2)

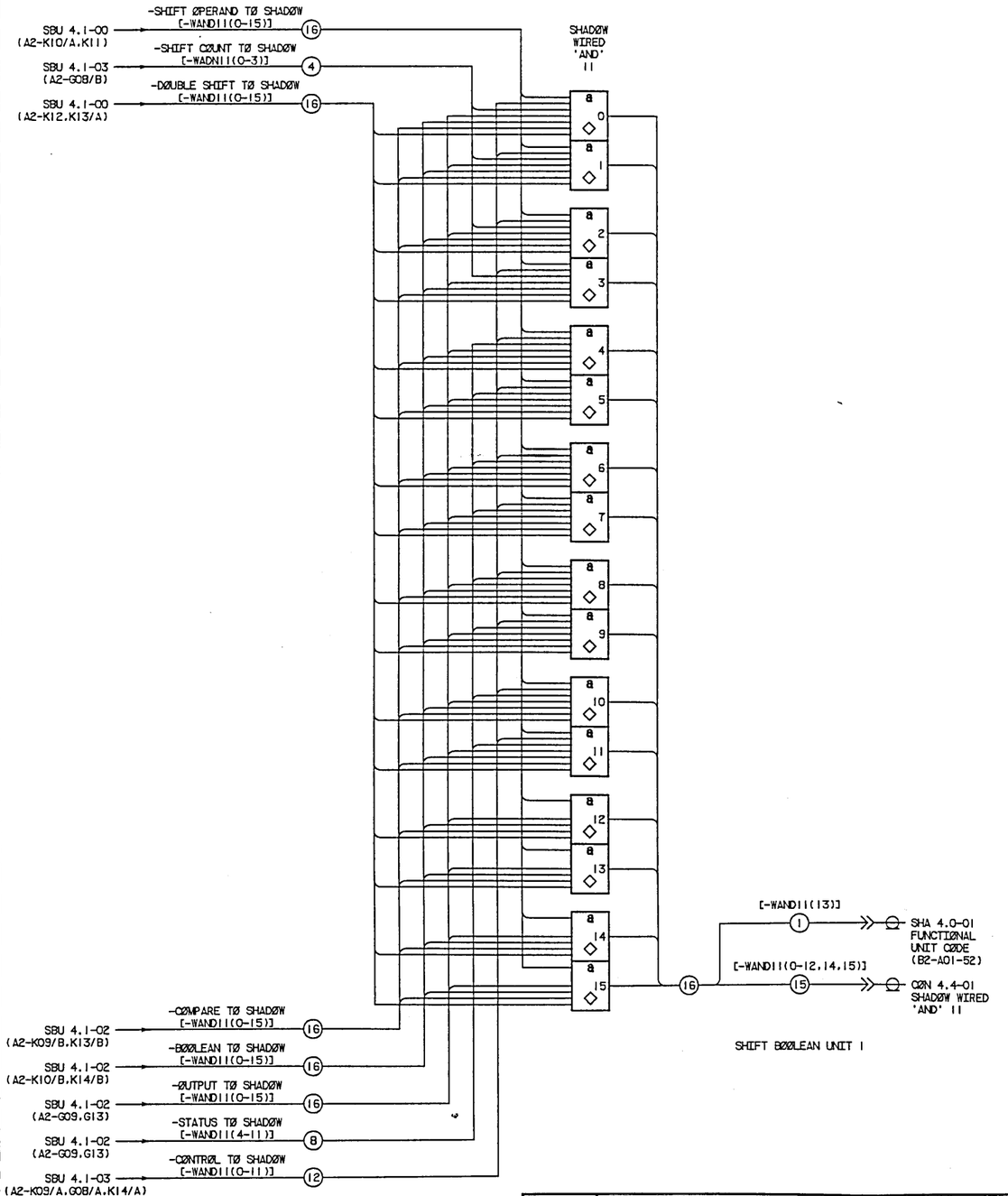
-CØMPARE = [-SBWDEQ] — SBU 4.1-02 (A2-G13-17)

L

1 02

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM SBU CØNTRØL, SB1	CODE IDENT 60461830	REV A
DEVELØPMENT DIVISIØN	DB-A2MUL:A2	SHEET SBU 4.1-03	PAGE IV-8-21





CONTROL DATA CORPORATION
DEVELØPMENT DIVISION

LEVEL 4 DIAGRAM
SHIFT BØØLEAN UNIT
SHADØW WIRED 'AND'
DB-A2MUL:A2

CODE IDENT | DWG NO: 60461830 | REV: A
SHEET: SBU 4.2-00 | PAGE: IV-8-23

9. SHADOW MATRIX UNIT (SHA)

SYSTEM FUNCTION

The shadow matrix, which is part of ring port 0, provides the means by which the contents of the registers in the base processor can be read and displayed. The shadow registers also provide the means to trap and store the state of the registers of the base processor when an interrupt occurs. Thereby providing a means to return to normal processing at the very same place in the program that was reached before the interruption.

GENERAL DESCRIPTION

The shadow matrix is a logical array of wired AND gates 8 rows deep by 16 columns wide. Each parcel in the matrix is wired to a 16-bit portion of a register in the processor. Each parcel can be addressed by specifying the hexidecimal values for the row and column in which it resides. Once selected, the data in the 16-bit parcel is gated along with the data from three other parcels to the external memory access unit 0, or, 16 bits at a time, to the output register of ring port 0.

LOCATION

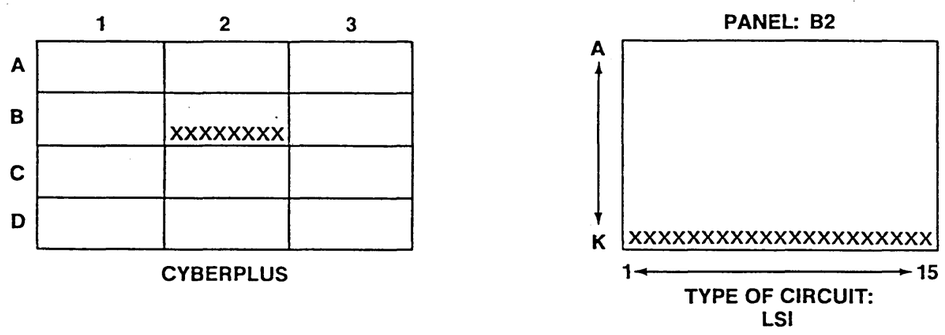
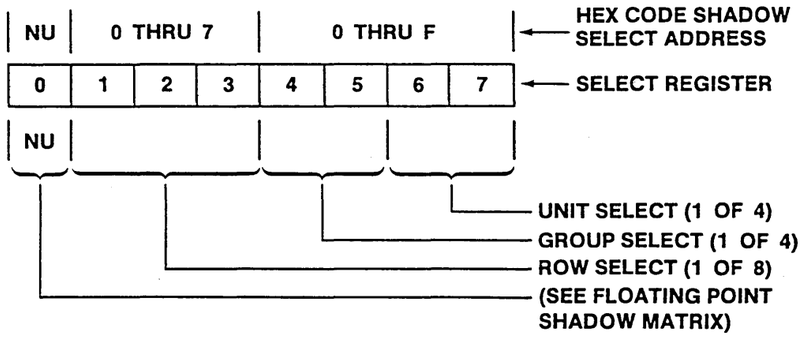


Figure IV-9-1. Location of Shadow Matrix Logic Circuits

FUNCTIONAL DESCRIPTION

Most registers within the base processor all have duplicate registers called shadow registers. These registers continually receive the same data as the operating registers, except during interrupt processing when they store the data as it existed when the interrupt occurred. To function as duplicate registers, which are read via the shadow matrix, each bit in a register is connected through a gate to a wired AND so that each separate bit position in each sixteen (or fewer) bits of the eight rows in a shadow matrix column is ANDed together.

The selection of the data to be read from the shadow matrix begins when the shadow select register is loaded from either the ring input register or the crossbar register of ring port 0. (The loading of the shadow select register is inhibited, if the lockout flipflop in ring port 0 is set.) The complete decoding of the shadow select matrix address occurs simultaneously. However, for ease of understanding, the enabling of the wired ANDs by the row decoder and row select circuits and the wired AND's logical operation is discussed first.



The row decoder decodes the three bit binary code (bits 1-3) resulting in the selection of one of a possible eight outputs. That output is fanned out to all of the register bits identified in one row of the shadow matrix. The purpose of this row select signal is to enable each bit in that row for gating through the wired ANDs to the group selector.

The condition of all logical 1 inputs to the wired AND produces a logical 1 output. When at least one of the inputs is a logical 0, a logical 0 is the resulting output. The eight inputs (one for each row) to the wired AND circuit of a matrix column are held at a logical 1 when they are disabled. Only one of the eight row inputs to each wired AND is enabled at a time, therefore the data held in the registers of that row is the only data which reaches the group selector network. However, since there are sixteen columns and each column has 16 bits, 256 bits of data reach the the group selector network when a row is selected.

The group selector decodes the two-bit binary code (bits 4,5) resulting in the selection of one group (4 columns) out of the possible four (16 columns). The selected group then gates 64 of the 256 bits of data from the matrix into the group select register. From there, the 64 selected bits go either to the unit selector for further division, or to XMAU 0 as a 64-bit word.

The unit selector decodes the last two binary bits (6 and 7), which results in the selection of a unit (one 16-bit column) out of the possible four. Fifteen bits of the selected unit are then available to the ring output register of ring port 0. The sixteenth bit, the LSB, is gated by the shadow lockout flipflop of ring port 0 to the ring output register. If the lockout flipflop is set the bit is always a logical zero.

SHADØW MATRIX

	GS0			
	US0	US1	US2	US3
-RØW 0	00 INST RGTR (0-15) CØN 4.4-00	01 INST RGTR (16-31) CØN 4.4-00	02 INST RGTR 32-47) CØN 4.4-00	03 INST RGTR (48-63) CØN 4.4-00
-RØW 1 +RØW 1	10 DMØ CØNTRØL RGTR (1) (0-11) (12-15)=2 DMU 4.0-00	11 DMI CØNTRØL RGTR (1) (0-11) (12-15)=3 DMU 4.1-00	12 DM2 CØNTRØL RGTR (1) (0-11) (12-15)=4 DMU 4.2-00	13 DM3 CØNTRØL RGTR (1) (0-11) (12-15)=5 DMU 4.3-00
-RØW 2	20 INPUT DATA RGTR (0-15) DMU 4.0-01	21 INPUT DATA RGTR (0-15) DMU 4.1-01	22 INPUT DATA RGTR (0-15) DMU 4.2-01	23 INPUT DATA RGTR (0-15) DMU 4.3-01
-RØW 3	30 INPUT ADRS RGTR (0-11) DMU 4.0-00	31 INPUT ADRS RGTR (0-11) DMU 4.1-00	32 INPUT ADRS RGTR (0-11) DMU 4.2-00	33 INPUT ADRS RGTR (0-11) DMU 4.3-00
-RØW 4	40 ØUTPUT DATA RGTR (0-15) DMU 4.0-01	41 ØUTPUT DATA RGTR (0-15) DMU 4.1-01	42 ØUTPUT DATA RGTR (0-15) DMU 4.2-01	43 ØUTPUT DATA RGTR (0-15) DMU 4.3-01
-RØW 5	50 ADRS CØMPARE RGTR/ 4 STATUS (0-11/12-15) DMU 4.0-00/01	51 ADRS CØMPARE RGTR/ 4 STATUS (0-11/12-15) DMU 4.1-00/01	52 ADRS CØMPARE RGTR/ 4 STATUS (0-11/12-15) DMU 4.2-00/01	53 ADRS CØMPARE RGTR/ 4 STATUS (0-11/12-15) DMU 4.3-00/01
-RØW 6	60 INCREMENT RGTR/ 4 STATUS (0-11/12-15) DMU 4.0-00/01	61 INCREMENT RGTR/ 4 STATUS (0-11/12-15) DMU 4.1-00/01	62 INCREMENT RGTR/ 4 STATUS (0-11/12-15) DMU 4.2-00/01	63 INCREMENT RGTR/ 4 STATUS (0-11/12-15) DMU 4.3-00/01
-RØW 7	70 DATA CØMPARE RGTR (0-15) DMU 4.0-01	71 DATA CØMPARE RGTR (0-15) DMU 4.1-01	72 DATA CØMPARE RGTR (0-15) DMU 4.2-01	73 DATA CØMPARE RGTR (0-15) DMU 4.3-01

	GS1			
	US0	US1	US2	US3
	04 INST RGTR (64-79) CØN 4.4-00	05 INST RGTR (80-95) CØN 4.4-00	06 INST RGTR (96-111) CØN 4.4-00	07 INST RGTR (112-127) CØN 4.4-00
	14 SBU 0 CØNTRØL RGTR (1) (0-11) (12-15)=A SBU 4.0-03	15 SBU 1 CØNTRØL RGTR (1) (0-11) (12-15)=B SBU 4.1-03	16 FILE UNIT CØNTRØL RGTR (1) (0-11) (12-15)=8 FGU 4.0-00	17 MULT CØNTRØL RGTR (1) (0-11) (12-15)=1 MUL 4.0-07
	24 SHIFT ØPERAND RGTR A (0-15) SBU 4.0-00	25 SHIFT ØPERAND RGTR A (0-15) SBU 4.1-00	26 INPUT DATA RGTR F (0-15) FGU 4.0-00	27 A ØPERAND RGTR (0-15) MUL 4.0-07
	34 BØØLEAN RGTR B (0-15) SBU 4.0-02	35 BØØLEAN RGTR B (0-15) SBU 4.1-02	36 INPUT DATA RGTR G (0-15) FGU 4.0-00	37 B ØPERAND RGTR (0-15) MUL 4.0-07
	44 ØUTPUT DATA RGTR (0-15) SBU 4.0-02	45 ØUTPUT DATA RGTR (0-15) SBU 4.1-02	46 ØUTPUT DATA RGTR F (0-15) FGU 4.0-01	47 ØUTPUT RGTR UPPER (0-15) MUL 4.0-08
	54 DØUBLE SHIFT INPUT RGTR (6) (0-15) SBU 4.0-02	55 DØUBLE SHIFT INPUT RGTR (6) (0-15) SBU 4.1-00	56 ØUTPUT DATA RGTR G (0-15) FGU 4.0-01	57 ØUTPUT RGTR LØWER (0-15) MUL 4.0-08
	64 X BAR SHIFT CØUNT/ STATUS (0-3/4-10) (6) SBU 4.0-02/03	65 X BAR SHIFT CØUNT/ STATUS (0-3/4-10) (6) SBU 4.1-02/03	66 CØNTRØL X BAR INPUT RGTR (0-15) CØN 4.0-01	67 DATA CØMPARE UPPER (0-15) MUL 4.0-08
	74 DATA CØMPARE RGTR (0-15) SBU 4.0-02	75 DATA CØMPARE RGTR (0-15) SBU 4.0-02	76 FILE UNIT UPPER/LØWER ADDR BIT (0) (1-15) NØT USED FGU 4.0-01	77 DATA CØMPARE LØWER (0-15) MUL 4.0-08

	GS2			
	US0	US1	US2	US3
	08 INST RGTR (128-143) CØN 4.4-00	09 INST RGTR (144-159) CØN 4.4-00	0A INST RGTR (160-175) CØN 4.4-00	0B INST RGTR (176-191) CØN 4.4-00
	18 RING PØRT 0 CØNTRØL RGTR (1) (0-11) (12-15)=E RPU 4.0-01	19 RING PØRT 1 CØNTRØL RGTR (1) (0-11 (12-15)=F RPU 4.X-XX	1A ADD 0 CØNTRØL RGTR (1) (0-11) (12-15)=6 ADD 4.0-02	1B ADD 1 CØNTRØL RGTR (1) (0-11) (12-15)=7 ADD 4.1-02
	28 RING PØRT 0 MASK RGTR (0-15) RPU 4.0-01	29 RING PØRT 1 MASK RGTR (0-15) RPU 4.1-01	2A INPUT DATA RGTR A (0-15) ADD 4.0-00	2B INPUT DATA RGTR A (0-15) ADD 4.1-00
	38 INTERMED/ CARRY (0-7/8-15) MUL 4.0-06	39 RING PØRT 0/1 STATUS (0-8) RPU 4.0-01/ RPU 4.1-01	3A INPUT DATA RGTR B (0-15) ADD 4.0-00	3B INPUT DATA RGTR B (0-15) ADD 4.1-00
	48 INTERMED/ CARRY (0-7/8-15) MUL 4.0-06	49 NØT USED	4A ØUTPUT DATA RGTR (0-15) ADD 4.1-00	4B ØUTPUT DATA RGTR (0-15) ADD 4.1-00
	58 INTERMED/ CARRY (0-7/8-15) MUL 4.0-06	59 NØT USED	5A STATUS RGTR (0-11) ADD 4.0-02	5B STATUS RGTR (0-11) ADD 4.1-02
	68 INTERMED/ CARRY (0-7/8-15) MUL 4.0-06	69 NØT USED	6A NØT USED	6B NØT USED
	78 STATUS RGTR (0-5) MUL 4.0-08	79 NØT USED	7A DATA CØMPARE RGTR (0-15) ADD 4.0-01	7B DATA CØMPARE RGTR (0-15) ADD 4.1-01

	GS3			
	US0	US1	US2	US3
	0C INST RGTR (192-199)/ (2) +STØP/INTR CØN 4.4-00	0D XMAU 0/1 CØNDITIØN RGTR (0-5/6-11) XMA 4.0-03	0E NØT USED	0F P RGTR/ CØNTRØL (0-11/12-15) (3) CØN 4.0-00
	1C NØT USED (0-7) (10-15) / +STØP (8) INTR (9) (2)	1D XMAU 0 CØNTRØL RGTR (0-11) (12-15)=C (1) XMA 4.0-00	1E XMAU 1 CØNTRØL RGTR (0-11) (12-15)=D (1) XMA 4.1-00	1F P RGTR/ CØNTRØL (0-11/12-15) (3) CØN 4.0-00
	2C NØT USED (0-7) (10-15) / +STØP (8) INTR (9) (2)	2D ADDRESS RGTR 1 (0-15) XMA 4.0-03	2E ADDRESS RGTR 1 (0-15) XMA 4.1-03	2F P RGTR/ CØNTRØL (0-11/12-15) (3) CØN 4.0-00
	3C NØT USED (0-7) (10-15) / +STØP (8) INTR (9) (2)	3D ADDRESS RGTR 2 (0-15) XMA 4.0-03	3E ADDRESS RGTR 2 (0-15) XMA 4.1-03	3F P RGTR/ CØNTRØL (0-11/12-15) (3) CØN 4.0-00
	4C NØT USED (0-7) (10-15) / +STØP (8) INTR (9) (2)	4D SEGMENT RGTR 1/2 (0-7/8-15) XMA 4.0-03	4E SEGMENT RGTR 1/2 (0-7/8-15) XMA 4.1-03	4F P RGTR/ CØNTRØL (0-11/12-15) (3) CØN 4.0-00
	5C NØT USED (0-7) (10-15) / +STØP (8) INTR (9) (2)	5D XMAU 0 STATUS (0-7) XMA 4.10-03	5E XMAU 1 STATUS (0-7) XMA 4.11-03	5F P RGTR/ CØNTRØL (0-11/12-15) (3) CØN 4.0-00
	6C NØT USED (0-7) (10-15) / +STØP (8) INTR (9) (2)	6D SEGMENT CØMPARE RGTR (0-7) XMA 4.0-01	6E SEGMENT CØMPARE RGTR (0-7) XMA 4.1-01	6F P RGTR/ CØNTRØL (0-11/12-15) (3) CØN 4.0-00
	7C NØT USED (0-7) (10-15) / +STØP (8) INTR (9) (2)	7D ADDRESS CØMPARE RGTR (0-15) XMA 4.0-01	7E ADDRESS CØMPARE RGTR (0-15) XMA 4.1-01	7F P RGTR/ CØNTRØL (0-11/12-15) (3) CØN 4.0-00

DMU 2.0 -SHADØW WIRED 'AND' 00 / -SHADØW WIRED 'AND' 01 / -SHADØW WIRED 'AND' 02 / -SHADØW WIRED 'AND' 03

CØN 2.0 -SHADØW WIRED 'AND' 10 / -SHADØW WIRED 'AND' 11 / -SHADØW WIRED 'AND' 12 / -SHADØW WIRED 'AND' 13

RPU 2.0 -SHADØW WIRED 'AND' 20 / RPU 2.1 -SHADØW WIRED 'AND' 21 / CØN 2.0 -SHADØW WIRED 'AND' 22 / CØN 2.0 -SHADØW WIRED 'AND' 23

CØN 2.0 -SHADØW WIRED 'AND' 30 / XMA 2.0 -SHADØW WIRED 'AND' 31 / XMA 2.0 -SHADØW WIRED 'AND' 32 / CØN 2.0 RPU 2.0 -SHADØW WIRED 'AND' 33

SHADØW MATRIX IS A GRAPHICAL REPRESENTATIØN ØF SHADØW RGTRS AND WIRED 'AND'S EXISTING THRØUGHØUT BASE PRØCESSØR ØN ALL LEVEL 2 PRINTS.

256 / 26 / 102

GRØUP SELECTØR (SHA 4.0-00) → 64 → UNIT SELECTØR (SHA 4.0-00) → 16 → (5) SHA 2.1 ØR RPU 2.0 RING ØUTPUT RGTR

64 → (5) SHA 2.1 ØR XMA 2.0 ASSEMBLY/DISASEMBLY DATA RGTR

-GRØUP SELECT (4.5) → (5) SHA 2.1

-UNIT SELECT (6.7) → (5) SHA 2.1

-SSR(0) → RPU 2.0

SHADØW RØW DECØDER (SHA 4.0-00) → 8 → SHADØW RØW SELECT FANØUT (SHA 4.0-01, SHA 4.0-02, SHA 4.0-03) → 1 → FØRCE FUNCTIØNAL UNIT CØDE (SHA 4.0-01)

RPU 2.0 RING INPUT RGTR → 8 → SHADØW SELECT RGTR (SHA 4.0-00) → 3 → SHADØW RØW SELECT (2.3) → SHA 2.1 (5)

RPU 2.0 CRØSS BAR RGTR → 8 → SHADØW SELECT RGTR → 2 → SHADØW RØW SELECT (2.3) → SHA 2.1 (5)

SHADØW SELECT RGTR → 2 → SHADØW RØW SELECT (2.3) → SHA 2.1 (5)

NØTES:

1. +RØW 1 IS FANNED ØUT TØ EACH WIRED 'AND', TØ FØRCE BITS 12-15 ØF RGTRS 10-1F EXCEPT 1C AND 1F TØ THE FUNCTIØNAL UNIT CØDE SHA 4.0-01.
2. +STØP BIT 8 CØN 4.5-11, INTR BIT 9 CØN 4.5-31.
3. CØNTRØL-BITS 12-14, RUN, BREAKPØINT ENABLE, PRØCESSØR INTERRUPT ENABLE, RPU 4.0-22, BIT 15, RING PØRT LØCKØUT, RPU 4.0-20.
4. SHADØW WIRED 'AND'S SHØWN IN MØRE DETAIL, SEE SHEETS SHA 3.1.3.2.
5. ØUTPUT TØ FLØATING PØINT UNIT ØPTIØN IF INSTALLED.
6. RGTR 54,55 BITS 0-15, RGTR 64,65 BITS 0-3 CØMPLEMENT DATA.

CONTROL DATA CORPORATION	LEVEL 2 DIAGRAM SHADØW MATRIX DECØDING	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN		SHEET SHA 2.0	PAGE IV-9-3

FLØATING PØINT SHADØW MATRIX

	GS0 US0	GS0 US1	GS0 US2	GS0 US3
–RØW 8	80 INST RGTR (200-215) FPC 4.0-00	81 INST RGTR (216-231) FPC 4.0-00	82 INST RGTR (232-239) FPC 4.0-00	83 CØNT RGTR (0-13) FPC 4.0-00
–RØW 9	90 FILE INPUT RGTR (0-15) FPC 4.0-04	91 FILE INPUT RGTR (16-31) FPC 4.0-04	92 FILE INPUT RGTR (32-47) FPC 4.0-04	93 FILE INPUT RGTR (48-63) FPC 4.0-04
–RØW A	A0 UNUSED	A1 UNUSED	A2 UNUSED	A3 UNUSED
–RØW B	B0 FILE ØUTPUT RGTR (0-15) FPC 4.0-05	B1 FILE ØUTPUT RGTR (16-31) FPC 4.0-05	B2 FILE ØUTPUT RGTR (32-47) FPC 4.0-05	B3 FILE ØUTPUT RGTR (48-63) FPC 4.0-05

	GS1 US0	GS1 US1	GS1 US2	GS1 US3
	84 ADDER STATUS RGTR (0-15) FPA 4.0-10	85 UNUSED	86 UNUSED	87 UNUSED
	94 ADDER A ØPERAND (0-15) FPA 4.0-01	95 ADDER A ØPERAND (16-31) FPA 4.0-01	96 ADDER A ØPERAND (32-47) FPA 4.0-01	97 ADDER A ØPERAND (48-63) FPA 4.0-01
	A4 ADDER B ØPERAND (0-15) FPA 4.0-01	A5 ADDER B ØPERAND (16-31) FPA 4.0-01	A6 ADDER B ØPERAND (32-47) FPA 4.0-01	A7 ADDER B ØPERAND (48-63) FPA 4.0-01
	B4 ADDER RESULTS RGTR (0-15) FPA 4.0-11	B5 ADDER RESULTS RGTR (16-31) FPA 4.0-11	B6 ADDER RESULTS RGTR (32-47) FPA 4.0-11	B7 ADDER RESULTS RGTR (48-63) FPA 4.0-11

	GS2 US0	GS2 US1	GS2 US2	GS2 US3
	88 MULT STATUS RGTR (0-14) FPM 4.0-	89 UNUSED	8A UNUSED	8B UNUSED
	98 MULT A ØPERAND (0-15) FPM 4.0-00	99 MULT A ØPERAND (16-31) FPM 4.0-00	9A MULT A ØPERAND (32-47) FPM 4.0-00	9B MULT A ØPERAND (48-63) FPM 4.0-00
	A8 MULT B ØPERAND (0-15) FPM 4.0-01	A9 MULT B ØPERAND (16-31) FPM 4.0-01	AA MULT B ØPERAND (32-47) FPM 4.0-01	AB MULT B ØPERAND (48-63) FPM 4.0-01
	B8 MULT RESULTS RGTR (0-15) FPM 4.	B9 MULT RESULTS RGTR (16-31) FPM 4.	BA MULT RESULTS RGTR (32-47) FPM 4.	BB MULT RESULTS RGTR (48-63) FPM 4.

	GS3 US0	GS3 US1	GS3 US2	GS3 US3
	8C DIV/SQR STATUS RGTR (0-14) FPD 4.1-04	8D UNUSED	8E UNUSED	8F UNUSED
	9C DIV/SQR A ØPERAND (0-15) FPD	9D DIV/SQR A ØPERAND (16-31)	9E DIV/SQR A ØPERAND (32-47)	9F DIV/SQR A ØPERAND (48-63)
	AC DIV/SQR B ØPERAND (0-15) FPD	AD DIV/SQR B ØPERAND (16-31)	AE DIV/SQR B ØPERAND (32-47)	AF DIV/SQR B ØPERAND (48-63)
	BC DIV/SQR RESULTS RGTR (0-15) FPD	BD DIV/SQR RESULTS RGTR (16-31)	BE DIV/SQR RESULTS RGTR (32-47)	BF DIV/SQR RESULTS RGTR (48-63)

FPC 2.0 — (16) –SHADØW WIRED 'AND' 00 / (16) –SHADØW WIRED 'AND' 01 / (16) –SHADØW WIRED 'AND' 02 / (16) –SHADØW WIRED 'AND' 03

FPA 2.0 — (16) –SHADØW WIRED 'AND' 10 / (16) –SHADØW WIRED 'AND' 11 / (16) –SHADØW WIRED 'AND' 12 / (16) –SHADØW WIRED 'AND' 13

(16) –SHADØW WIRED 'AND' 20 / (16) –SHADØW WIRED 'AND' 21 / (16) –SHADØW WIRED 'AND' 22 / (16) –SHADØW WIRED 'AND' 23 → (64) → FPM 2.0

FPD 2.0 — (16) –SHADØW WIRED 'AND' 30 / (16) –SHADØW WIRED 'AND' 31 / (16) –SHADØW WIRED 'AND' 32 / (16) –SHADØW WIRED 'AND' 33

(52) (64) (64) (64) (64)

THE FLØATING PØINT SHADØW MATRIX IS A GRAPHICAL REPRESENTATIØN ØF SHADØW REGISTERS AND WIRED 'AND'S EXISTING THRØUGHØUT THE FLØATING PØINT PRØCESSØR ØN MØST LEVEL 2 PRINTS.

(1) SHA 2.0 — –SHADØW RØW SELECT (BITS 2.3) — (2) → FP SHADØW RØW SELECT FANØUT SHA 4.1-01

SHA 2.0 — –HPP SHADØW (0-15) — (16)

SHA 2.0 — –UNIT SELECT (BITS 6.7) — (2)

(256)

(1) SHA 2.0 — –GRØUP SELECT (BITS 4.5) — (2)

(64) –CØNT SHADØW (0-63)

(64) –ADDER SHADØW (0-63)

(64) –MULT SHADØW (0-63)

(64) –DIV SHADØW (0-63)

→ FP GRØUP SELECTØR SHA 4.1-00 → FP SHADØW DATA

FP SHADØW DATA → –(0-15) / –(16-31) / –(32-47) / –(48-63) → FP UNIT SELECTØR SHA 4.1-00 → SHADØW SELECTØR SHA 4.1-00 → (16) INTEGER/FPU SHADØW DATA (0-15) → RPU 2.0

FPC 2.0 — –XBAR ØUTPUT — (64)

SHA 2.0 — –HPP SHADØW (0-63) — (64)

(1) SHA 2.0 — –SHADØW SELECT (BIT 0) — (1)

FP SHADØW DATA → –(0-63) → (0-63) → XMAU 0 SELECTØR SHA 4.1-00 → (64) XMAU 0 DATA ØUT (0-63) → XMA 2.0

FP SHADØW DATA → –(0-31) → (32-63) → XMAU 0 SELECTØR SHA 4.1-00

(0-63) → XMAU 0 SELECTØR SHA 4.1-00

(0-31) → XMAU 1 SELECTØR SHA 4.1-00 → (64) XMAU 1 DATA ØUT (0-63) → XMA 2.0

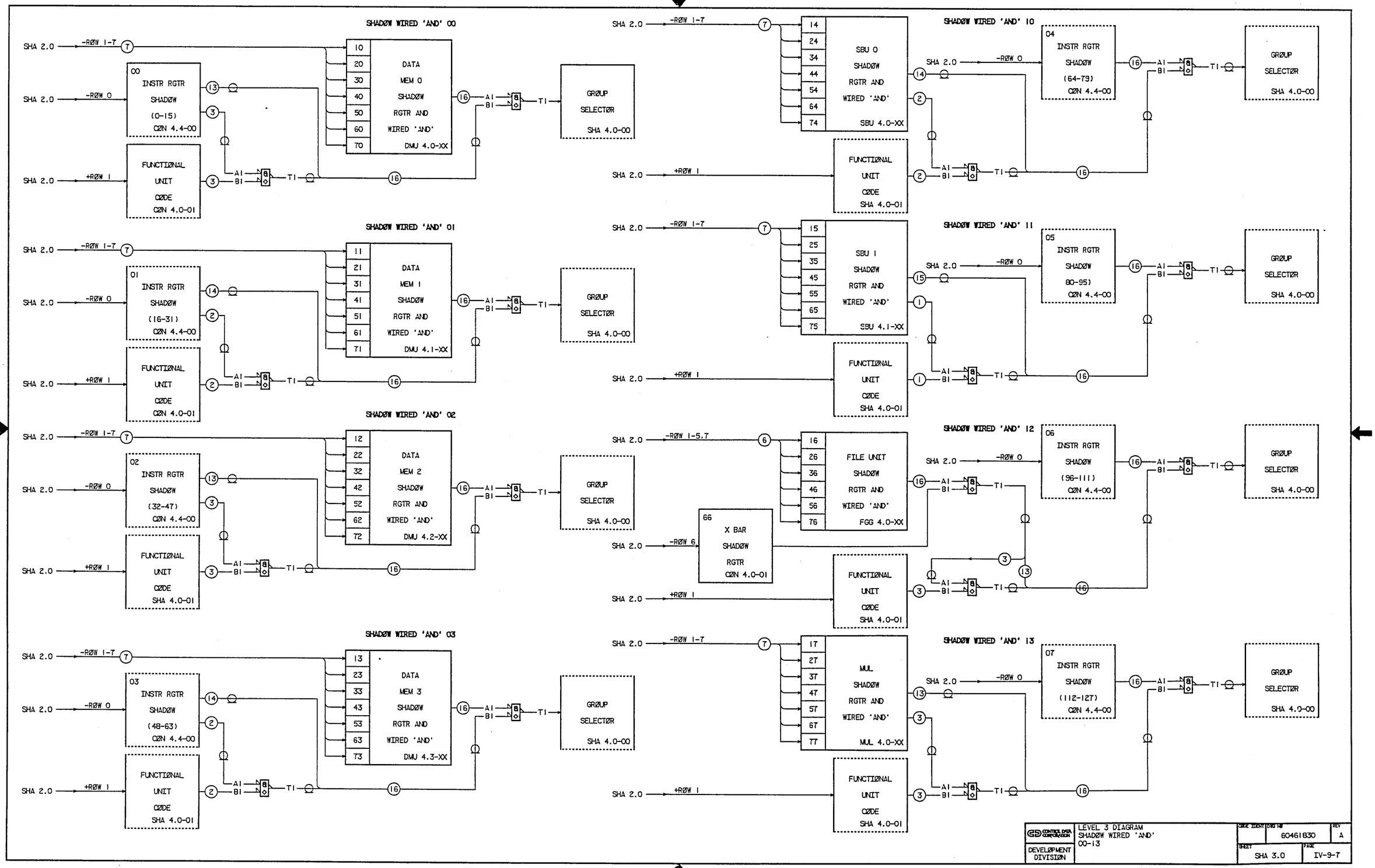
(0-31) → XMAU 1 SELECTØR SHA 4.1-00

(32-63) → XMAU 1 SELECTØR SHA 4.1-00

NØTE:

(1) SHADØW SELECT BITS 0,2,3,4,5, ØRIGINATE ØN SHA BUT GØES THRU A GATE ØN RPU.

CONTROL DATA CORPORATION	LEVEL 2 DIAGRAM FLØATING PØINT SHADØW MATRIX DECØDING	CODE IDENT / DWG NO: 60461830	REV: A
DEVELØPMENT DIVISIØN		SHEET: SHA 2.1	PAGE: IV-9-5


SHADØW WIRED 'AND' 00
SHA 2.0 -RØW 1-7
SHA 2.0 -RØW 0
SHA 2.0 +RØW 1
00 INSTR RGTR SHADØW (0-15) CØN 4.4-00
FUNCTIØNAL UNIT CØDE CØN 4.0-01
10 20 30 40 50 60 70
DATA MEM 0 SHADØW RGTR AND WIRED 'AND' DMU 4.0-XX
AI BI TI
GRØUP SELECTØR SHA 4.0-00
SHADØW WIRED 'AND' 01
01 INSTR RGTR SHADØW (16-31) CØN 4.4-00
11 21 31 41 51 61 71
DATA MEM 1 SHADØW RGTR AND WIRED 'AND' DMU 4.1-XX
SHADØW WIRED 'AND' 02
02 INSTR RGTR SHADØW (32-47) CØN 4.4-00
12 22 32 42 52 62 72
DATA MEM 2 SHADØW RGTR AND WIRED 'AND' DMU 4.2-XX
SHADØW WIRED 'AND' 03
03 INSTR RGTR SHADØW (48-63) CØN 4.4-00
13 23 33 43 53 63 73
DATA MEM 3 SHADØW RGTR AND WIRED 'AND' DMU 4.3-XX
SHADØW WIRED 'AND' 10
04 INSTR RGTR SHADØW (64-79) CØN 4.4-00
14 24 34 44 54 64 74
SBU 0 SHADØW RGTR AND WIRED 'AND' SBU 4.0-XX
SHADØW WIRED 'AND' 11
05 INSTR RGTR SHADØW 80-95) CØN 4.4-00
15 25 35 45 55 65 75
SBU 1 SHADØW RGTR AND WIRED 'AND' SBU 4.1-XX
SHADØW WIRED 'AND' 12
06 INSTR RGTR SHADØW (96-111) CØN 4.4-00
16 26 36 46 56 66 76
FILE UNIT SHADØW RGTR AND WIRED 'AND' FGG 4.0-XX
66 X BAR SHADØW RGTR CØN 4.0-01
SHA 2.0 -RØW 1-5.7
SHA 2.0 -RØW 6
SHADØW WIRED 'AND' 13
07 INSTR RGTR SHADØW (112-127) CØN 4.4-00
17 27 37 47 57 67 77
MUL SHADØW RGTR AND WIRED 'AND' MUL 4.0-XX
FUNCTIØNAL UNIT CØDE SHA 4.0-01
GRØUP SELECTØR SHA 4.0-00
CONTROL DATA CORPORATION
DEVELOPMENT DIVISIØN
LEVEL 3 DIAGRAM
SHADØW WIRED 'AND'
00-13
CODE IDENT
DWG NO
60461830
REV
A
SHEET
SHA 3.0
SIZE
IV-9-7

SHADØW WIRED 'AND' 20

SHA 2.0 -RØW 1,2 (2)
SHA 2.0 -RØW 3-7 (5)
SHA 2.0 -RØW 0
SHA 2.0 +RØW 1

38 48 58 68 78 — MUL SHADØW RGTR AND WIRED 'AND' — MUL 4.0-06

18 28 — RING 0 SHADØW RGTR AND WIRED 'AND' — RPU 4.0-XX

08 INSTR RGTR SHADØW (128-143) CØN 4.4-00

FUNCTIØNAL UNIT CØDE — SHA 4.0-01

A I / B I / T I

GRØUP SELECTØR — SHA 4.0-00

SHADØW WIRED 21

SHA 2.0 -RØW 1-3 (3)
SHA 2.0 -RØW 0
SHA 2.0 +RØW 1

19 29 39 — RING PØRT 1 SHADØW RGTR AND WIRED 'AND' — RPU 4.1-XX

09 INSTR RGTR SHADØW (144-159) CØN 4.0-00

FUNCTIØNAL UNIT CØDE — SHA 4.0-01

GRØUP SELECTØR — SHA 4.0-00

SHADØW WIRED 'AND' 22

SHA 2.0 -RØW 0
SHA 2.0 -RØW 1-5,7 (6)
SHA 2.0 +RØW 1

1A 2A 3A 4A 5A 7A — ADD 0 SHADØW RGTR AND WIRED 'AND' — ADD 4.0-XX

0A INSTR RGTR SHADØW (160-175) CØN 4.0-00

FUNCTIØNAL UNIT CØDE — SHA 4.0-01

GRØUP SELECTØR — SHA 4.0-00

SHADØW WIRED 'AND' 23

SHA 2.0 -RØW 0
SHA 2.0 -RØW 1-5,7 (6)
SHA 2.0 +RØW 1

1B 2B 3B 4B 5B 7B — ADD 1 SHADØW RGTR AND WIRED 'AND' — ADD 4.1-XX

0B INSTR RGTR SHADØW (176-191) CØN 4.0-00

FUNCTIØNAL UNIT CØDE — SHA 4.0-01

GRØUP SELECTØR — SHA 4.0-00

SHADØW WIRED 'AND' 30

OC INSTR RGTR SHADØW (192-199) CØN 4.0-00
OC-7C +STØP CØN 4.5-11
OC-7C INTP CØN 4.5-31

GRØUP SELECTØR — SHA 4.0-00

SHADØW WIRED 'AND' 31

SHA 2.0 -RØW 0-7 (8)
SHA 2.0 +RØW 2

00 10 20 30 40 50 60 70 — X MAU 0 SHADØW RGTR AND WIRED 'AND' — XMA 4.0-XX

FUNCTIØNAL UNIT CØDE — SHA 4.0-01

GRØUP SELECTØR — SHA 4.0-00

SHADØW WIRED 'AND' 32

SHA 2.0 -RØW 1-7 (5)
SHA 2.0 +RØW 2

1E 2E 3E 4E 5E 6E 7E — X MAU 1 SHADØW RGTR AND WIRED 'AND' — XMA 4.1-XX

FUNCTIØNAL UNIT CØDE — SHA 4.0-01

GRØUP SELECTØR — SHA 4.0-00

SHADØW WIRED 'AND' 33

OF-7F P RGTR CØN 4.0-00
OF-7F RUN BREAK PØINT ENABLE PRØCESSØR INSR ENABLE — RPU 4.0-22

GRØUP SELECTØR — SHA 4.0-00

CONTROL DATA CORPORATION
DEVELOPMENT DIVISIØN

LEVEL 3 DIAGRAM
SHADØW WIRED 'AND'
20-33

CHGE LEVEL | DWG NO 60461830 | REV A
SHEET SHA 3.1 | PAGE IV-9-9

RØW DECØDER

12170 E16/D17

DEMUX

[-RSR(1)]
[-RSR(2)]
[-RSR(3)]

-RØW 7 [-GRØUP(7)] → SHA 4.0-03 (B2-A07/B-41)
-RØW 6 (13-20) (J02-46) [-GRØUP(6)] → SHA 4.0-03 (B2-A07/A-15)
-RØW 5 (12-21) (J03-47) [-GRØUP(5)] → SHA 4.0-02 (B2-A09/B-41)
-RØW 4 (13-24) (J02-50) [-GRØUP(4)] → SHA 4.0-02 (B2-A09/A-15)
-RØW 3 (13-26) (J02-52) [-GRØUP(3)] → SHA 4.0-02 (B2-C09/B-41)
-RØW 2 (13-25) (J02-51) [-GRØUP(2)] → SHA 4.0-02 (B2-C09/A-15)
-RØW 1 (12-04) (J03-30) [-GRØUP(1)] → SHA 4.0-01 (B2-C07/B-41)
-RØW 0 (12-01) (J03-27) [-GRØUP(0)] → SHA 4.0-01 (B2-C07/A-15)
(13-20) (J02-47) [-RSR(1-3)] (1-3)

BIAS LØ=3.4 HI=17

-RGTR SEL RGTR BIT 1 [-RSR(1.2)] → M RPU 4.1-13 (B2/J2-C11-23,15)
-RGTR SEL RGTR BIT 2 [-RSR(3)] → N RPU 4.1-20 (B2/J2-C13-19)

DUPLICATED ØN RPU 4.1-22 AUX BØARD B2/J2

RSR	AUX	LSI
1	(1-42)	(J02-42)
2	(1-43)	(J02-43)
3	(1-45)	(J02-45)

SHADØW SELECT RGTR AND CØUNTER

12CD G08/1D08

256 CNTR WITH PARITY TØGGLE

-RING RGTR SEL [-RID(12-19)] ← RPU 4.0-10 (B2/J1-C04,C05)
-X BAR RGTR SEL [-XBREGØ(8-15)] ← RPU 4.0-01 (B2-H08)
-CLØCK [-SYSCLK(6)] ← CLK 4.1-01 (A2-B02-04)
-ENA RGTR SEL [-ENRS] ← RPU 4.0-22 (B2/J1-A02-07,15)
[-NPRRS]
+RGTR SEL LØCKØUT [-PRRS] ← RPU 4.0-12 (B2/J1-C17-12)
-INCREMENT [-INCRS] ← RPU 4.0-22 (B2/J1-A01-14)

PARA 48 A(0-7)
PARB 43 B(0-7)
C1D
C2D
CLCK
EN
SEL(0)
SEL(1)
CINA
CINB
CINC
CIND
PMIL
DECR
CZERØ

27 CØUT
29 PARZ
Z(0-7)
-(0-7)
[-RSR(1-3)]
[-RSR(0)] → RPU 4.2-11 (B2/F1-D07,D14/C-19)
[-RSR(4.5)]
[-SRSELØ(6,7)/-SRSELI(6,7)]
[-SRSEL(6,7)] → FPC 4.0-03

49 BGTR
50 BGTRL
51 BEQR
47 BEQRL

NØTES:
1. EACH DATA TRUNK CØNTAINS 8 DATA BITS AND 1 PARITY BIT. DURING CØUNT ØPERATIØNS THE PARITY BIT TØGGLES WHEN AN ØDD NUMBER ØF DATA BITS TØGGLE.
2. ØUTPUTS BGTR AND BGTRL ARE UNDEFINED WHEN CZERØ IS LØ.

105

NØTES:
1. ØUTPUTS TØ FLØATING PØINT UNIT ØPTIØN IF INSTALLED.
2.

CD ARRAY

BIT	A	B	Z
0	45	44	31
1	42	34	26
2	38	37	23
3	35	32	25
4	20	17	24
5	18	01	21
6	16	09	05
7	11	06	04

3.

CB ARRAY

BIT	A	B	C	D	Z
0	34	35	32	48	30
1	36	33	31	47	49
2	37	38	44	46	29
3	42	41	45	43	50
4	20	17	27	23	28
5	18	15	25	16	04
6	21	24	19	22	26
7	12	11	10	02	05

4. DUAL DRIVE ØUTPUT (6.7).

DUPLICATED ØN RPU 4.2-11 AUX BØARD B2/F1

12102 D07/A02-E/E

[-RSR(4)] (4-17) (F05-17) → -(4)
[-STASEL(1)] (3-3) (F04-03) → RPU 4.0-20 (B2/J1-D15-19)
[-NSTAS(1)] (3-1) (F04-01) → RPU 4.2-11 (B2/F1-D14/D-23)

12112 E14/D15-A/D

[-NSTAS(1)] (12-9) (J03-35)
[-CBRSØ(0)] (11-16) (J04-42)
[-CBRSØ(1)] (11-15) (J04-41)
TP119

DUPLICATED ØN RPU 4.1-22 AUX BØARD B2/J2

12112 E14/D15-B/D

[-RSR(5)] (12-20) (J03-46) → -(5)
[-CBRSI(0)] (11-19) (J04-45)
[-CBRSI(1)] (11-21) (J04-47)
RPU 4.1-22 (B2/J2-E14-19)
TP108

-(6.7)

CØNTRØL LØGIC

DMU 4.0-00 DATA MEMØRY 0 INS RGTR (0-15)
DMU 4.4-00 DATA MEMØRY 1 INS RGTR (16-31)
DMU 4.4-01 DATA MEMØRY 2 INS RGTR (32-47)
DMU 4.4-01 DATA MEMØRY 3 INS RGTR (48-63)
CØN 4.4-01 INS RGTR (64-79) SHIFT BØØLEAN 0
CØN 4.4-01 INS RGTR (80-95) SHIFT BØØLEAN 1
CØN 4.4-01 INS RGTR (96-111) FILE UNIT
CØN 4.4-01 INS RGTR (112-127) MULTIPLY
RPU 4.3-00 RING PØRT 0 INS RGTR (128-143)
RPU 4.3-00 RING PØRT 1 INS RGTR (144-159)
CØN 4.4-01 INS RGTR (160-171,173,174) ADD UNIT 0
CØN 4.4-01 INS RGTR (176-187,189-191) ADD UNIT 1
CØN 4.4-01 INS RGTR (192-199)
CØN 4.5-11 (C2/B2-E13-06) CØN 4.5-31 (C2/C2-E05-18)
NU
XMA 4.0-04 XMAU 0
XMA 4.0-04 XMAU 1
SHA 4.0-01 FUNCTIØNAL UNIT CØDE
CØN 4.0-00 P+1 ADDER (C2-F01,02)
RPU 4.0-22 CØNT RGTR (B2/J1-A07-7,11,14)
NU
CLK 4.1-06 (A2-H10-46,45,51,52,01)

-SHADØW WIRED 'AND' 00 [-WANDØØ(0-15)]
-SHADØW WIRED 'AND' 01 [-WANDØ1(0-15)]
-SHADØW WIRED 'AND' 02 [-WANDØ2(0-15)]
-SHADØW WIRED 'AND' 03 [-WANDØ3(0-15)]
-SHADØW WIRED 'AND' 10 [-WAND10(0-15)]
-SHADØW WIRED 'AND' 11 [-WAND11(0-15)]
-SHADØW WIRED 'AND' 12 [-WAND12(0-15)]
-SHADØW WIRED 'AND' 13 [-WAND13(0-15)]
-SHADØW WIRED 'AND' 20 [-WAND20(0-15)]
-SHADØW WIRED 'AND' 21 [-WAND21(0-15)]
-SHADØW WIRED 'AND' 22 [-WAND22(0-11,13,14)]
-SHADØW WIRED 'AND' 23 [-WAND23(0-11,13-15)]
-SHADØW WIRED 'AND' 30 [-WAND30(0-7)]
+STØP, INTERRUPT [-NSTØP(10).INTR(6)]
-SHADØW WIRED 'AND' 30 [-WAND30(10-15)]
-SHADØW WIRED 'AND' 31 [-WAND31(0-13)]
-SHADØW WIRED 'AND' 32 [-WAND32(0-13,15)]
-WIRED 'AND' 22 [-WAND22(12,15)]
-WIRED 'AND' 23 [-WAND23(12)]
-WIRED 'AND' 31 [-WAND31(14,15)]
-WIRED 'AND' 32 [-WAND32(14)]
-P+1 (4-15) [-P(4-15)/-WAND33(0-11)]
-RUN [-RUN1/-WAND33(12)]
-BREAKPØINT ENABLE [-BKPEN1/-WAND33(13)]
-PRØC INTR ENABLE [-RPIL/-WAND33(14)]
[-WAND33(15)]
-CLØCK [-ØFFCLK(47-51)]
-GRØUP SELECT (0,1)

GRØUP SELECTØR

12CB K01/1B15 BITS 0-7
12CB K02/1B16 BITS 8-15
12CB K03/1B17 BITS IN:0-7 16-23
12CB K04/1B18 BITS IN:8-15 24-31
12CB H12/1B19 BITS 3 IN:0-7 32-39
12CB K13/1B20 BITS IN:8-15 40-47
12CB K14/1B21 BITS IN:0-7 48-55
12CB K15/1B22 BITS IN:8-15 56-63

-WIRED 'AND' 00
-WIRED 'AND' 10
-WIRED 'AND' 20
-WIRED 'AND' 30
-WIRED 'AND' 01
-WIRED 'AND' 11
-WIRED 'AND' 21
-WIRED 'AND' 31
-WIRED 'AND' 02
-WIRED 'AND' 12
-WIRED 'AND' 22
-WIRED 'AND' 32
-WIRED 'AND' 03
-WIRED 'AND' 13
-WIRED 'AND' 23
-WIRED 'AND' 33

[-ØFFCLK(50)] [-ØFFCLK(51)] [-ØFFCLK(48)] [-ØFFCLK(49)] [-ØFFCLK(47)]
[-CBRSØ(0)] [-CBRSØ(1)] [-CBRSI(0)] [-CBRSI(1)]

CLCKEN Ø6 CLCK Ø3 S(0) Ø8 S(1) Ø7 RGTR

-(0-15) -(16-31) -(32-47) -(48-63)

UNIT SELECTED

-(6) -(7)

-INTEGER SHADØW [-RGTR(0-63)] (2WØ14/2WØ15) → SHA 4.1-00 (HØG → JØ8) ØR XMA 4.0-01 ASSEMBLY/ DISASEMBLY DATA RGTR

[-SHREGØ(0-15)/-SHREGI(0-15)] (2WØ18) → SHA 4.1-00 (C3-F01,H01) ØR RPU 4.0-00 RING ØUTPUT RGTR

CØNTRØL DATA CØRPØRATIØN
DEVELØPMENT DIVISIØN

LEVEL 4 DIAGRAM
SHADØW WIRED 'AND'
DB-B2RPU:B2

CODE IDENT | DWG NO 60461830 | REV A
SHEET SHA 4.0-00 | PAGE IV-9-11

SHADØW RØW SELECT 0

SHA 4.0-00 RØW DECØDER (B2/J2-E16-05)

-RØW 0 [-GRØUP(0)]

CØN 4.4-00 INSTR RGTR

[-INSREG(12.13.15.28.29.44.46.47.60.62)]

-SHADØW RØW SELECT 0 [-URSO(0-8)]

CØN 4.4-00 INST RGTR

12|HB|A CØ7/7B01-A/B

12|HB|A AO6/7B09-A/C

XMA 4.0-03 XMAU O/I CØNDITIØN BITS (D2-G10-35,43)

SHADØW RØW SELECT 1

SHA 4.0-00 RØW DECØDER (B2/J2-E16-07)

-RØW 1 [-GRØUP(1)]

12|HB|B CØ7/7B02-B/B

DMU 4.0-00 DMO CØNT RGTR (B2-C13-35,43)

SBU 4.0-03 CØNTRØL RGTR (A2-J02/A-35)

DMU 4.1-00 DMI CØNT RGTR (B2-D15-35,43)

SBU 4.1-03 CØNT RGTR (A2-K14/A-35)

DMU 4.2-00 DM2 CØNT RGTR (B2-A05-35,43)

FGU 4.0-00 FILE CØNT RGTR (A2-H08/A-35)

DMU 4.3-00 DM3 CØNT RGTR (B2-D04-35,43)

MUL 4.0-07 CØNT RGTR (A2-E05/A → A06/A-35)

RPU 4.0-01 CØNT RGTR (B2-G07-35,43)

ADD 4.0-02 CØNT RGTR (D2-F04/B → G04/B-35)

12|HB|A AO6/7B09-B/C

12|HB|A AO6/7B09-C/C

RPU 4.1-01 CØNT RGTR (B2-G09-35,43)

ADD 4.1-02 CØNT RGTR (D2-F08/B → G08/B-35)

SHADØW RØW SELECT 1

ØN LSI BD D2

[-NURSI(0)]

12|HB|A D11/7B34-A/D

XMA 4.0-00 XMAUO CØNT RGTR (D2-D12-35,43)

XMA 4.1-00 XMAUI CØNT RGTR (D2-F11-35,43)

FUNCTIONAL UNIT CØDE

12|HB|A AO1/7B13-A/B

12|HB|B AO1/7B14-B/B

12|HB|A AO2/7B15-A/B

12|HB|B AO2/7B16-B/B

+RØW 1

XMA 4.0-04 SHADØW WIRED 'AND' 32 BIT (14)

SBU 4.2-00 SHADØW WIRED 'AND' 11 BIT (13)

SBU 4.2-00 SHADØW WIRED 'AND' 10 BITS (13,15)

FGU 4.0-02 SHADØW WIRED 'AND' 12 BITS (13-15)

MUL 4.0-09 SHADØW WIRED 'AND' 20 BIT (15)

CØN 4.4-00 SHADØW WIRED 'AND' 22 BITS (12,15)

MUL 4.0-09 SHADØW WIRED 'AND' 13 BITS (12-14)

CØN 4.4-00 SHADØW WIRED 'AND' 23 BIT (12)

XMA 4.0-04 SHADØW WIRED 'AND' 31 BITS (14,15)

NU

SHA 4.0-00 GRØUP SELECTØR VIA DMU 4.4-00 SHADØW WIRED 'AND' 00 BITS (12,13,15)

SHA 4.0-00 GRØUP SELECTØR VIA DMU 4.4-00 SHADØW WIRED 'AND' 01 BITS (12,13)

SHA 4.0-00 GRØUP SELECTØR VIA DMU 4.4-01 SHADØW WIRED 'AND' 02 BITS (12,14,15)

SHA 4.0-00 GRØUP SELECTØR VIA DMU 4.4-01 SHADØW WIRED 'AND' 03 BITS (12,14)

CØN 4.4-01 INS RGTR

SHA 4.0-00 GRØUP SELECTØR

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM SHADØW-RØW SELECT CØDES 0.1	CODE IDENTIFICATION NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-B2RPU:B2 DB-D2XMU:D2	SHEET SHA 4.0-01 PAGE IV-9-13



SHADØW RØW SELECT 2

121HB|A| DI177834-B/D

[-NURS2(0)] → ØN LSI BD D2

A(1) 18 → 12112 → 25 T1(1), 26 T2(1), 23 F1(1), 24 F2(1) → 2|01

[-URS2(13)] → XMA 4.0-03 ADRS RGTR 1 (D2-B11-35,43)

[-URS2(14)] → XMA 4.1-03 ADRS RGTR 1 (D2-F15,F14/A-35)

SHADØW RØW SELECT 3

121HB|A| DI177834-C/D

[-NURS3(0)] → ØN LSI BD D2

A(2) 36 → 12112 → 27 T1(2), 28 T2(2), 29 F1(2), 30 F2(2) → 2|01

[-URS3(13)] → XMA 4.0-03 ADRS RGTR 2 (D2-B10/B,A09/A-43)

[-URS3(14)] → XMA 4.1-03 ADRS RGTR 2 (D2-F14,G13-43)

SHA 4.0-00 RØW DECØDER (B2/J2-E16-08)

-RØW 2 [-GRØUP(2)]

SHADØW RØW SELECT 2

121HB|A| C09/7B03-A/B

CX 15 → 12112 → 20 T1(0), 19 T2(0), 22 F1(0), 21 F2(0), 25 T1(1), 26 T2(1), 23 F1(1), 24 F2(1), 27 T1(2), 28 T2(2), 29 F1(2), 30 F2(2), 34 T1(3), 33 T2(3), 32 F1(3), 31 F2(3) → 1|02

A(0) 17

A(1) 18

A(2) 36

L

A(3) 35

[-URS2(0)] → DMU 4.0-01 INPUT DATA (B2-C12/B,C11/B-43)

[-URS2(4)] → SBU 4.0-00 INPUT DATA A (A2-K05-35)

[-NURS2(0)]

[-URS2(1)] → DMU 4.1-01 INPUT DATA (B2-D12/B,D11/B-43)

[-URS2(5)] → SBU 4.1-00 INPUT DATA A (A2-K11-35)

[-URS2(2)] → DMU 4.2-01 INPUT DATA (B2-A04/B,A05/B)

[-URS2(6)] → FGU 4.0-00 F DATA RGTR (A2-J08/B-43)

[-URS2(3)] → DMU 4.3-01 INPUT DATA (B2-D05/B,D06/B-43)

[-URS2(7)] → MUL 4.0-00 A ØPERAND (A2-E04/B → E09/B-43)

121HB|B| A06/7B10-A/D

A(0) 43 → 12112 → 46 T1(0), 45 T2(0), 48 F1(0), 47 F2(0) → 2|01

[-URS2(8)] → RPU 4.0-01 MASKS RGTR (B2-H10,H09-43)

[-URS2(10)] → ADD 4.0-00 A ØPERAND (D2-F04/A,F01/A-43)

121HB|B| A06/7B10-B/D

A(1) 44 → 12112 → 51 T1(1), 52 T2(1), 49 F1(1), 50 F2(1) → 2|01

[-URS2(9)] → RPU 4.1-01 MASK RGTR (B2-H07,H06-43)

[-URS2(11)] → ADD 4.1-00 A ØPERAND (D2-F06/A,F05/A-43)

[-URS3(0)] → DMU 4.0-00 INPUT ADRS (B2-C08-35,43)

SHADØW RØW SELECT 3

121HB|B| C09/7B34-B/B

-RØW 3 [-GRØUP(3)]

SHA 4.0-00 RØW DECØDER (B2/J2-E16-06)

CX 41 → 12112 → 46 T1(0), 45 T2(0), 48 F1(0), 47 F2(0), 51 T1(1), 52 T2(1), 49 F1(1), 50 F2(1), 01 T1(2), 02 T2(2), 03 F1(2), 04 F2(2), 08 T1(3), 07 T2(3), 06 F1(3), 05 F2(3) → 1|02

A(0) 43

A(1) 44

A(2) 10

L

A(3) 09

[-URS3(4)] → SBU 4.0-02 INPUT DATA B (A2-K06/B,J02/B-43)

[-NURS3(0)]

[-URS3(1)] → DMU 4.1-00 INPUT ADRS (B2-D09-35,42)

[-URS3(5)] → SBU 4.1-02 INPUT DATA B (A2-K10/B,K14/B-43)

[-URS3(2)] → DMU 4.2-00 INPUT ADRS (B2-A08-35,43)

[-URS3(6)] → FGU 4.0-00 G DATA RGTR (A2-J14/B-43)

[-URS3(3)] → DMU 4.3-00 INPUT ADRS (B2-D08-35,43)

[-URS3(7)] → MUL 4.0-00 B ØPERAND (A2-E07/B → E08/B-43)

121HB|B| A06/7B10-C/D

A(2) 10 → 12112 → 01 T1(2), 02 T2(2), 03 F1(2), 04 F2(2) → 2|01

[-URS3(8)] → MUL 4.0-06 INTER/CARRY (A2-A13,A11/A-35)

[-URS3(10)] → ADD 4.0-00 B ØPERAND (D2-G04/A,G01/A-43)

121HB|B| A06/7B10-D/D

A(3) 09 → 12112 → 08 T1(3), 07 T2(3), 06 F1(3), 05 F2(3) → 2|01

[-URS3(9)] → RPU 4.0-01 RPØ/1 STATUS (B2-H10,H09-35)

[-URS3(11)] → ADD 4.1-00 B ØPERAND (D2-G08/A,G05/A-43)

SHADØW RØW SELECT 4

SHA 4.0-00 RØW DECØDER (B2/J2-E16-11)

-RØW 4 [-GRØUP(4)]

121HB|A| A09/7B05-A/B

CX 15 → 12112 → 20 T1(0), 19 T2(0), 22 F1(0), 21 F2(0), 25 T1(1), 26 T2(1), 23 F1(1), 24 F2(1), 27 T1(2), 28 T2(2), 29 F1(2), 30 F2(2), 34 T1(3), 33 T2(3), 32 F1(3), 31 F2(3) → 1|02

A(0) 17

A(1) 18

A(2) 36

L

A(3) 35

[-URS4(0)] → DMU 4.0-01 ØUTPUT DATA RGTR (B2-C03/B,C02/B-43)

[-URS4(4)] → SBU 4.0-02 ØUTPUT DATA RGTR (B2-G02,G06-43)

[-URS4(1)] → DMU 4.1-01 ØUTPUT DATA RGTR (B2-D03/B,D02/B-43)

[-URS4(5)] → SBU 4.1-02 ØUTPUT DATA RGTR (A2-G09,G13-43)

[-URS4(2)] → DMU 4.2-01 ØUTPUT DATA RGTR (B2-A13/B,A14/B-43)

[-URS4(6)] → FGU 4.0-01 F FILE DATA ØUTPUT RGTR (A2-G15/A,K08-35)

[-URS4(3)] → DMU 4.3-01 ØUTPUT DATA RGTR (B2-D13/B,D14/B-43)

[-URS4(7)] → MUL 4.0-08 ØUTPUT RGTR UPPER (A2-A15/B,E15/B-43)

121HB|A| A10/7B11-A/D

A(0) 17 → 12112 → 20 T1(0), 19 T2(0), 22 F1(0), 21 F2(0) → 2|01

[-URS4(8)] → MUL 4.0-06 INTER/CARRY (A2-A11/B-43)

[-URS4(10)] → ADD 4.0-00 ØUTPUT DATA RGTR (D2-H02/A,H03/A-43)

121HB|A| A10/7B11-B/D

A(1) 18 → 12112 → 25 T1(1), 26 T2(1), 23 F1(1), 24 F2(1) → 2|01

[-USR4(9)] → NU

[-URS4(11)] → ADD 4.1-00 ØUTPUT DATA RGTR (D2-H06/A,H07/A-43)

[-NURS4(0)] → ØN LSI BD D2

121HB|A| DI177834-D/D

A(3) 35 → 12112 → 34 T1(3), 33 T2(3), 32 F1(3), 31 F2(3) → 2|01

[-URS4(13)] → XMA 4.0-03 SEGMENT RGTR (D2-A08-43,35)

[-URS4(14)] → XMA 4.1-03 SEGMENT RGTR (D2-G13,F13-35,43)

SHADØW RØW SELECT 5

SHA 4.0-00 RØW DECØDER (B2/J2-E16-13)

-RØW 5 [-GRØUP(5)]

121HB|B| A09/7B06-B/B

CX 41 → 12112 → 46 T1(0), 45 T2(0), 48 F1(0), 47 F2(0), 51 T1(1), 52 T2(1), 49 F1(1), 50 F2(1), 01 T1(2), 02 T2(2), 03 F1(2), 04 F2(2), 08 T1(3), 07 T2(3), 06 F1(3), 05 F2(3) → 1|02

A(0) 43

A(1) 44

A(2) 10

L

A(3) 09

[-URS5(0)] → DMU 4.0-00 ADRS CØMPARE RGTR (B2-C04/A,C05/B,C01/A)

[-URS5(4)] → SBU 4.0-00 DØUBLE SHIFT INPUT (A2-K04,K03/A-35)

[-URS5(1)] → DMU 4.1-00 ADRS CØMPARE RGTR (B2-C06/A,D07/B,D01/A)

[-URS5(5)] → SBU 4.1-00 DØUBLE SHIFT INPUT (A2-K12,K13/A-35)

[-URS5(2)] → DMU 4.2-00 ADRS CØMPARE RGTR (B2-A12/A,A11/B,A13/A)

[-URS5(6)] → FGU 4.0-01 G FILE DATA ØUTPUT RGTR (A2-H15/B-43)

[-URS5(3)] → DMU 4.3-00 ADRS CØMPARE RGTR (B2-D10/A,C10/B,D13/A)

[-URS5(7)] → MUL 4.0-08 ØUTPUT RGTR LØWER (A2-A06/B,E05/B-43)

121HB|A| A10/7B11-C/D

A(2) 36 → 12112 → 27 T1(2), 28 T2(2), 29 F1(2), 30 F2(2) → 2|01

[-URS5(8)] → MUL 4.0-06 INTER/CARRY (A2-B05-43,35)

[-URS5(10)] → ADD 4.0-02 STATUS RGTR (D2-H02/B → F01/B-35)

121HB|A| A10/7B11-D/D

A(3) 35 → 12112 → 34 T1(3), 33 T2(3), 32 F1(3), 31 F2(3) → 2|01

[-URS5(9)] → NU

[-URS5(11)] → ADD 4.1-02 STATUS RGTR (D2.H06/B → F05/B-35)

[-NURS5(0)] → ØN LSI BD D2

121HB|B| J09/7B50-C/D

A(2) 10 → 12112 → 01 T1(2), 02 T2(2), 03 F1(2), 04 F2(2) → 2|01

[-URS5(13)] → XMA 4.10-03 STATUS (D2/E1-E07-22)

[-URS5(14)] → XMA 4.11-03 STATUS (D2/E2-E03-22)

CONTROL DATA CORPORATION

DEVELØPMENT DIVISIØN

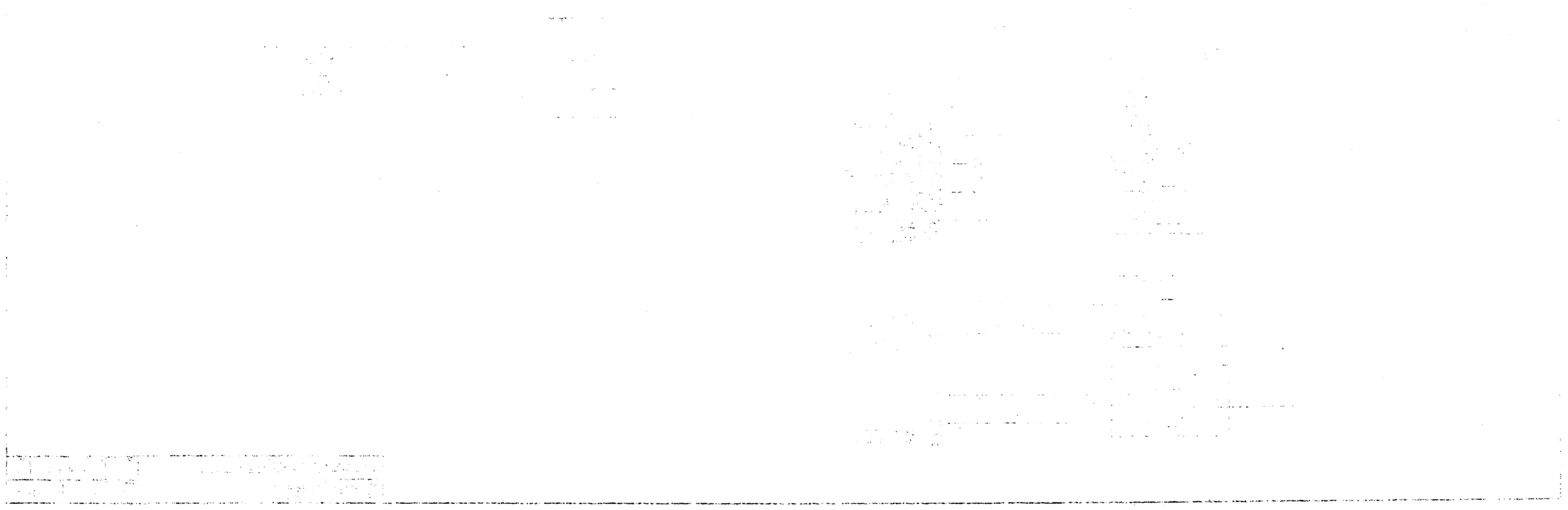
LEVEL 4 DIAGRAM
SHADØW RØW SELECT CØDES 2-5
B2-D2
DB-B2APU:B2
DB-D2XMU:D2

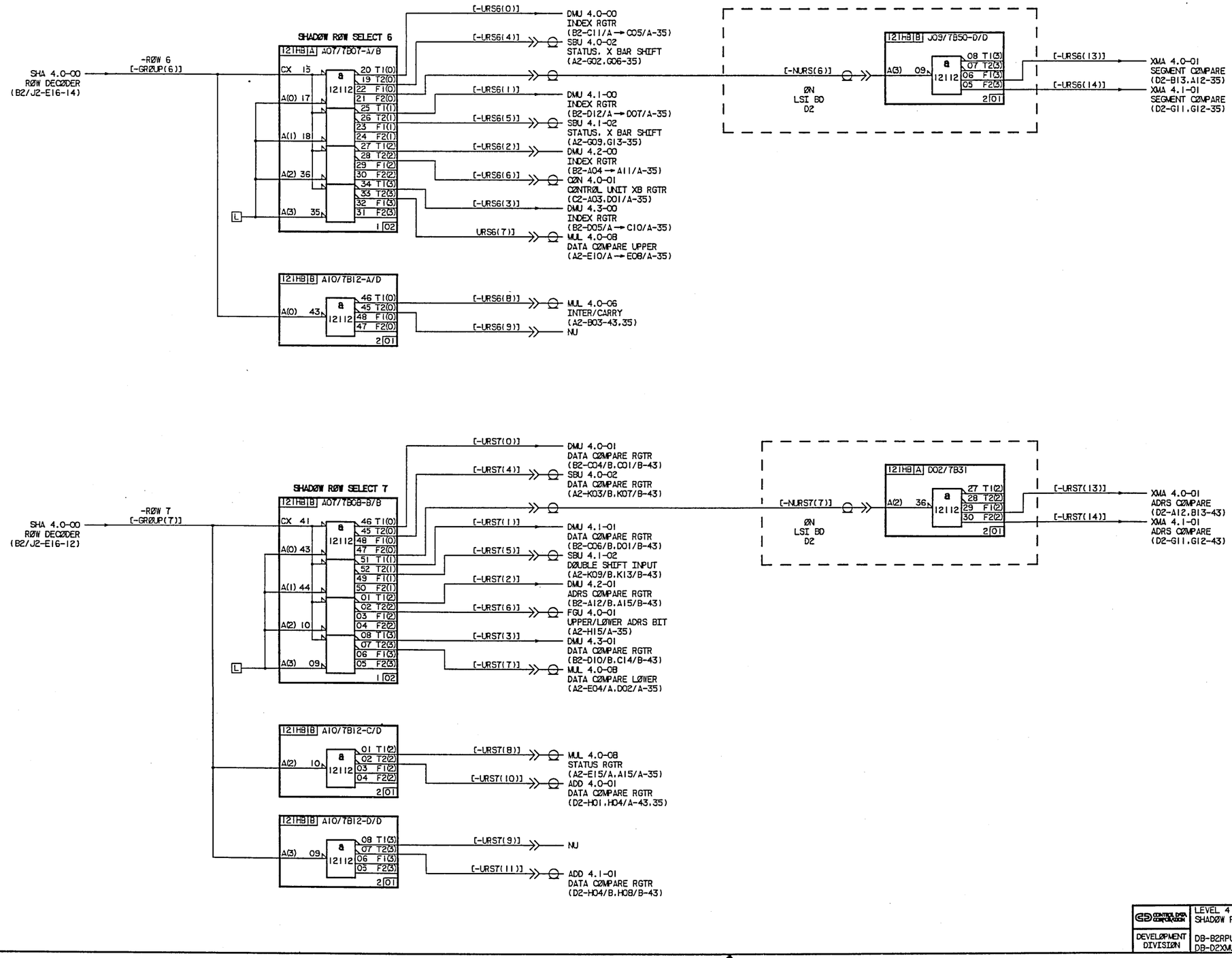
DRG NØ 60461830

REV A

SHEET SHA 4.0-02

PAGE IV-9-15



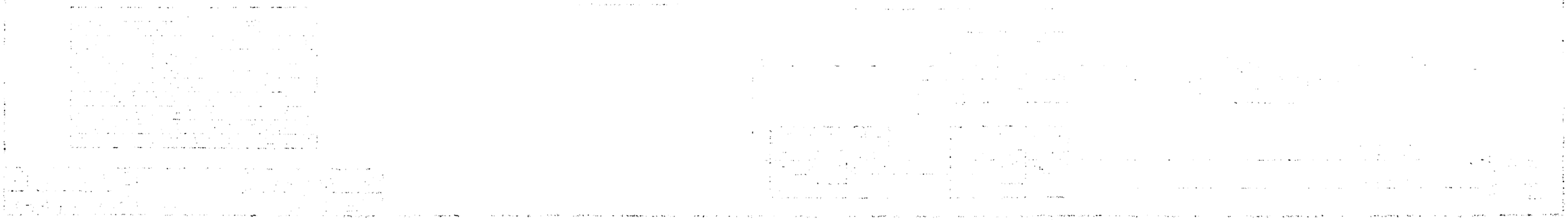


CONTROL DATA CORPORATION
DEVELØPMENT DIVISION

LEVEL 4 DIAGRAM
SHADØW RØW SELECT CØDES 6-7

DB-B2RPU:B2
DB-D2XMU:D2

CODE IDENT
DWG NO 60461830
REV A
SHEET SHA 4.0-03
PAGE IV-9-17



SHA 4.0-00 (B2-K01 → K15)
FPC 4.0-01 (C3-F02 → D12)
FPC 4.0-02 (C3-F03 → D13)
-INTEGER SHADØW RGTR (0-63) [-RGTR(0-63)]
-XMAU DATA (0-31)
-XMAU DATA (32-63)
XMA 4.10-03 (D2/E1-C07-14)
-READ SHADØW [-RDSHAD]
CLK 4.3-03 (C3-C01/B-01)
-CLKTØ (20) [-1B21-CLCK]
FPD 4.0-01 SHADØW WIRED 'AND' 30-33
-DIVIDE UNIT SHADØW (0-63) [-DSHAD(0-63)]
FPM 4.0-01 SHADØW WIRED 'AND' 20-23
-MULTIPLY UNIT SHADØW (0-63) [-MSHAD(0-63)]
FPA 4.0-12 WIRED 'AND' 10-13
-ADD UNIT SHADØW (0-63) [-ASHAD(0-63)]
FPC 4.0-00 (C3-D08)
-INSTRUCTIØN RGTR SHADØW (0-39) [-ISHAD(0-39)]
FPC 4.0-03 (C3-A15)
-MØDE RGTR SHADØW (0-13) [-MDSHAD(0-13)]
FPC 4.0-04 (C3-C15 → F14)
-FILE INPUT RGTR SHAD (0-63)
FPC 4.0-05 (C3-G15 → F14)
-FILE ØUTPUT RGTR SHAD (0-63)
CLK 4.3-03 (C3-C01/B-02)
-CLKTØ (21) [-1B23-CLCK]
CLK 4.3-03 (C3-C01/B-08)
-CLKTØ (22) [-1B25-CLCK]
CLK 4.3-03 (C3-C01/B-07)
-CLKTØ (23) [-1B27-CLCK]
RPU 4.2-11 (B2/F1-D14/D-12)
[-SRSEL(4)]
RPU 4.1-22 (B2/J2-E14-18)
[-SRSEL(5)]
FPC 4.0-00 (C3-F07 → D08)
+ØUT SELECT
RPU 4.2-11 (B2/F1-D14/C-13)
[-SRSEL(0)]
XMA 4.10-03 (D2/E1-C07-13)
+READ SHADØW [-NRDSH-01]
FPC 4.0-00 (C3-D08-27)
-ØUTPUT SELECT

SHA 4.0-00 (B2-G08)
[-SRSEL(6-7)]
SHA 4.0-00 (B2-K08.K09)
-INTEGER SHADØW DATA (0-15) [-SHREG(0-15)]

XMAUØ SELECTØR
XMAU1 SELECTØR
FP GRØUP SELECTØR
FP UNIT SELECTØR
SHADØW SELECTØR

-XMAU Ø DATA ØUT (0-63) [-XMØFPD(0-63)/RGTR(0-63)] → XMA 4.0-01 (D2-D10)
-XMAU 1 DATA ØUT (0-63) [-XM1FPD(0-63)] → XMA 4.1-01 (D2-K02 → K09)
-INTEGER/FPU SHADØW DATA (0-15) [-SHREGI(0-15)] → RPU 4.0-00 (B2-G04)

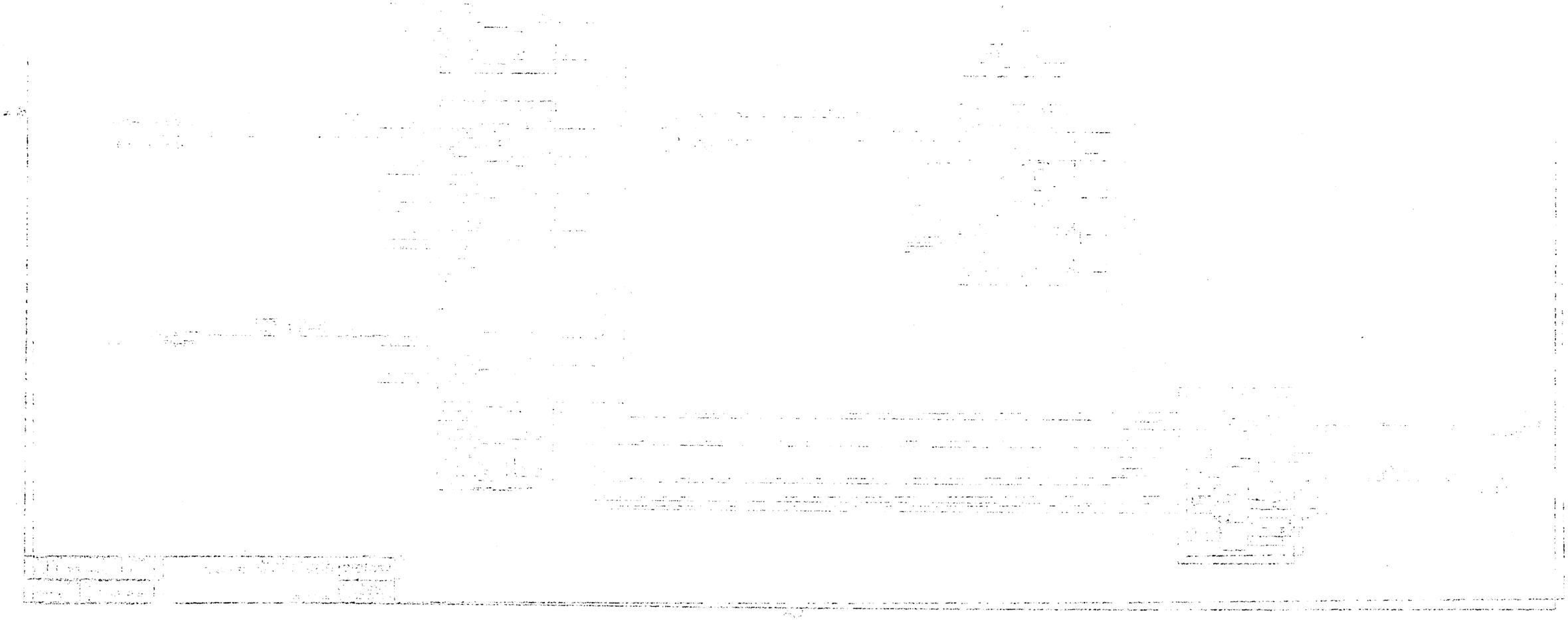
NØTE:
⚠1 ISHAD, MDSHAD, FILE INPUT RGTR SHAD, AND FILE ØUTPUT RGTR SHAD ARE 'WIRE ANDED' VIA FØIL ØN LSI PANAL.

CS/CB

BIT PØSITIØN							A	B	C	D	Z
0	8	16	24	32	40	48	56	34	35	32	48	30
1	9	17	25	33	41	49	57	36	33	31	47	49
2	10	18	26	34	42	50	58	37	38	44	46	29
3	11	19	27	35	43	51	59	42	41	45	43	50
4	12	20	28	36	44	52	60	20	17	27	23	28
5	13	21	29	37	45	53	61	18	15	25	16	4
6	14	22	30	38	46	54	62	21	24	19	22	26
7	15	23	31	39	47	55	63	12	11	10	2	5

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
LEVEL 4 DIAGRAM
F.P. SHADØW
XMAU Ø + 1 FANIN
DR-C3FPK:C3
05-20-86
60461830
REV H
SHEET SHA 4.1-00
PAGE IV-9-19

<50 60 70 80 90 FULL



RØW 8

121HB|B AO6/7B50-B/B

CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09

8 12112

46 T1(0) -(0)
45 T2(0)
48 F1(0)
47 F2(0)
51 T1(1) -(1)
52 T2(1)
49 F1(1)
50 F2(1)
01 T1(2) -(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)

1|02

(3) -EN INST RGTR SHAD (0-2) → FPC 4.0-00 (C3-F07)

[-FPURSO(0)] → FPA 4.0-10 (D3-A09-43,35)

[-FPURSO(4)] → FPM 4.0-06 (B3-J15/A-35)

[-FPURSO(8)] → FPD 4.1-04 (A3-D15/A,J15/A-35)

-EN MØDE RGTR SHAD → FPC 4.0-03 (C3-D15,A15)

[-FPURSO(12)] → NU

RØW 9

121HB|A AO7/7B51-A/B

CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35

8 12112

20 T1(0) -(0)
19 T2(0) -(2)
22 F1(0)
21 F2(0)
25 T1(1) -(1)
26 T2(1) -(3)
23 F1(1)
24 F2(1)
27 T1(2) -(0)
28 T2(2) -(2)
29 F1(2)
30 F2(2)
34 T1(3) -(1)
33 T2(3) -(3)
32 F1(3)
31 F2(3)

1|02

(4) -EN FILE INPUT RGTR SHAD (0-3) → FPC 4.0-04 (C3-C15→C14,F14/B)

(4) [-FPURS1(0-3)] → FPA 4.0-00 (D3-A01→A08)

RØW 9

121HB|B AO7/7B52-B/B

CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09

8 12112

46 T1(0) -(4)
45 T2(0) -(8)
48 F1(0)
47 F2(0)
51 T1(1) -(5)
52 T2(1) -(9)
49 F1(1)
50 F2(1)
01 T1(2) -(6)
02 T2(2) -(10)
03 F1(2)
04 F2(2)
08 T1(3) -(7)
07 T2(3) -(11)
06 F1(3)
05 F2(3)

1|02

(4) [-FPURS1(4-7)] → FPM 4.0-00 (B3-D01→F02)

(4) [-FPURS1(8-11)] → FPD 4.0-00 (A3-C01→K01)

RØW A

121HB|A AO8/7B53-A/B

CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35

8 12112

20 T1(0) -(0)
19 T2(0) -(4)
22 F1(0)
21 F2(0)
25 T1(1) -(1)
26 T2(1) -(5)
23 F1(1)
24 F2(1)
27 T1(2) -(2)
28 T2(2) -(6)
29 F1(2)
30 F2(2)
34 T1(3) -(3)
33 T2(3) -(7)
32 F1(3)
31 F2(3)

1|02

(4) [-FPURS2(0-3)] → FPA 4.0-00 (D3-B01→B08)

(4) [-FPURS2(4-7)] → FPM 4.0-01 (B3-A02→C02)

RØW A/B

121HB|B AO8/7B54-B/B

CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09

8 12112

46 T1(0) -(8)
45 T2(0) -(10)
48 F1(0)
47 F2(0)
51 T1(1) -(9)
52 T2(1) -(11)
49 F1(1)
50 F2(1)
01 T1(2) -(0)
02 T2(2) -(2)
03 F1(2)
04 F2(2)
08 T1(3) -(1)
07 T2(3) -(3)
06 F1(3)
05 F2(3)

1|02

(4) [-FPURS2(8-11)] → FPD 4.0-01 (A3-C02→K02)

(4) [-FPURS3(0-3)] → FPA 4.0-11 (D3-A13/B→B15/B,A14/A→D15/A)

RØW B

121HB|A AO9/7B55-A/B

CX 15
A(0) 17
A(1) 18
A(2) 36
A(3) 35

8 12112

20 T1(0) -(4)
19 T2(0) -(8)
22 F1(0)
21 F2(0)
25 T1(1) -(5)
26 T2(1) -(9)
23 F1(1)
24 F2(1)
27 T1(2) -(6)
28 T2(2) -(10)
29 F1(2)
30 F2(2)
34 T1(3) -(7)
33 T2(3) -(11)
32 F1(3)
31 F2(3)

1|02

(4) [-FPURS3(4-7)] → FPM 4.0-06 (B3-E15→K14-35,43)

(4) [-FPURS3(8-11)] → FPD 4.0-04 (A3-D15/B→J15/B)

RØW B

121HB|B AO9/7B56-B/B

CX 41
A(0) 43
A(1) 44
A(2) 10
A(3) 09

8 12112

46 T1(0) -(0)
45 T2(0) -(2)
48 F1(0)
47 F2(0)
51 T1(1) -(1)
52 T2(1) -(3)
49 F1(1)
50 F2(1)
01 T1(2)
02 T2(2)
03 F1(2)
04 F2(2)
08 T1(3)
07 T2(3)
06 F1(3)
05 F2(3)

1|02

(4) -EN FILE ØUTPUT RGTR SHAD (0-3) → FPC 4.0-05 (C3-G15→F15,F14/B)

121HE|A AO6/7E06-A/B

CX 15
A(0) 20
B(0) 19
A(1) 22
B(1) 21
A(2) 33
B(2) 34
A(3) 35
B(3) 36
A(4) 18
B(4) 17

8 12102

25 T(0)
26 F(0)
24 T(1)
23 F(1)
32 T(2)
31 F(2)
29 T(3)
30 F(3)
28 T(4)
27 F(4)

0|02

RPU 4.1-13 (B2/J2-C11-14) → [-SRSEL(2)]

RPU 4.1-20 (B2/J2-C13-13) → [-SRSEL(3)]

L

CONTROL DATA CORPORATION	LEVEL 4 DIAGRAM FP SHADØW RØW SELECT FANØUT	CODE IDENT	DWG NO 60461830 REV A
DEVELØPMENT DIVISIØN	DB-C3FPK:C3	SHEET SHA 4.1-01	PAGE IV-9-21